

TOSHIBA Field Effect Transistor Silicon N Channel Junction Type

TTK101MFV

For ECM

Application for compact ECM

Thin package: 0.5mm

Low capacitance: $C_{iss} = 1.8 \text{ pF (typ.) @ } V_{DS} = 2 \text{ V, } V_{GS} = 0, f = 1 \text{ MHz}$

Low noise: $V_N = 15 \text{ mV (typ.)}$

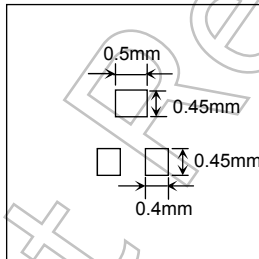
@ $V_{DD}=2 \text{ V, } R_K=1\text{k}\Omega, C_g=10\text{pF, } G_v=80\text{dB, A-Cuve Filter}$

Absolute Maximum Ratings (Ta=25°C)

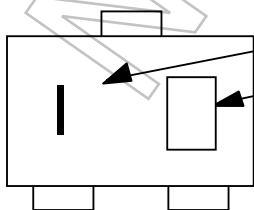
Characteristic	Symbol	Rating	Unit
Gate-drain voltage	V_{GDO}	-20	V
Gate current	I_G	10	mA
Drain power dissipation	P_D (Note 1)	150	mW
Junction temperature	T_j	125	°C
Storage temperature range	T_{stg}	-55 to 125	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Mounted on FR4 board (25.4 mm × 25.4 mm × 1.6 t)



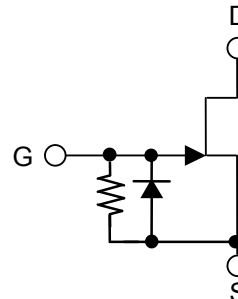
Marking



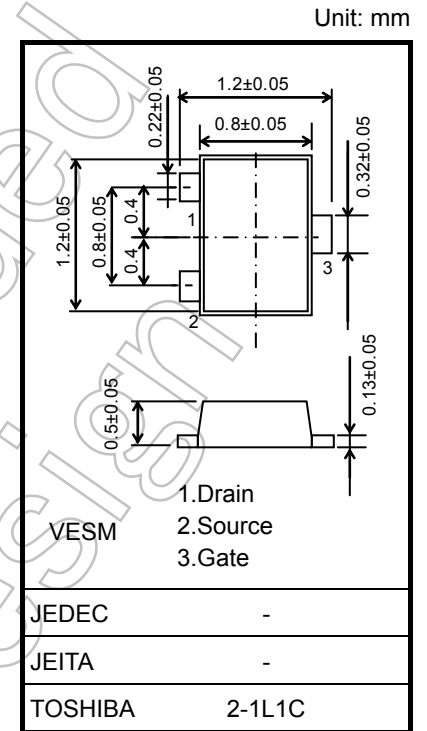
Type Name
 I_{DSS} Classification Symbol
 1: A-Rank
 2: B-Rank

I_{DSS} Classification
 A-Rank 140 to 240 μA
 B-Rank 210 to 340 μA

Equivalent Circuit



Start of commercial production
 2009-03



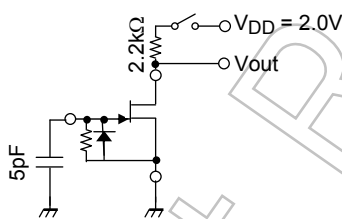
Weight: 1.5mg (typ.)

Electrical Characteristics (Ta=25°C)

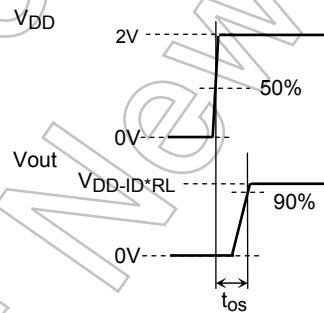
Characteristic	Symbol	Test Condition	Min	Typ.	Max	Unit	
Drain current	I _{DSS}	V _{DS} = 2 V, V _{GS} = 0	A	140	—	240	μA
			B	210	—	350	
Drain current	I _D	V _{DD} = 2 V, R _L = 2.2kΩ, C _g = 5pF	A	125	—	260	μA
			B	190	—	370	
Gate-source cut-off voltage	V _{GS(OFF)}	V _{DS} = 2 V, I _D = 1μA	-0.1	—	-1.0	V	
Forward transfer admittance	Y _{fs}	V _{DS} = 2 V, V _{GS} = 0V	0.65	0.9	—	mS	
Gate-drain breakdown voltage	V _{(BR)GDO}	I _G = -100 μA	-20	—	—	V	
Input capacitance	C _{iss}	V _{DS} = 2 V, V _{GS} = 0, f = 1 MHz	—	1.8	—	pF	
Voltage gain	G _v	V _{DD} = 2V, R _L = 2.2kΩ, C _g = 5pF, f = 1kHz, v _{in} = 100mV	A	-2.7	-1.3	—	dB
			B	-1.8	-0.6	—	
Delta voltage gain	DG _{v(f)}	V _{DD} = 2V, R _L = 2.2kΩ, C _g = 5pF, f = 1kHz to 100Hz, v _{in} = 100mV	—	0	-1.0	dB	
Delta voltage gain	DG _{v(V)}	V _{DD} = 2 V to 1.5 V, R _L = 2.2 kΩ, C _g = 5pF, f = 1kHz, v _{in} = 100mV	A	—	-0.7	-1.4	dB
			B	—	-1.4	-3.0	
Noise voltage	V _N	V _{DD} = 2 V, R _L = 1 kΩ, C _g = 10 pF, G _v = 80 dB, A-Curve Filter	—	15	30	mV	
Total harmonic distortion	THD	V _{DD} = 2 V, R _L = 2.2kΩ, C _g = 5 pF, f = 1kHz, v _{in} = 50mV	A	—	1.1	—	%
			B	—	0.6	—	
Time output stability	t _{os}	V _{DD} = 2 V, R _L = 2.2 kΩ, C _g = 5 pF	—	20	50	ms	

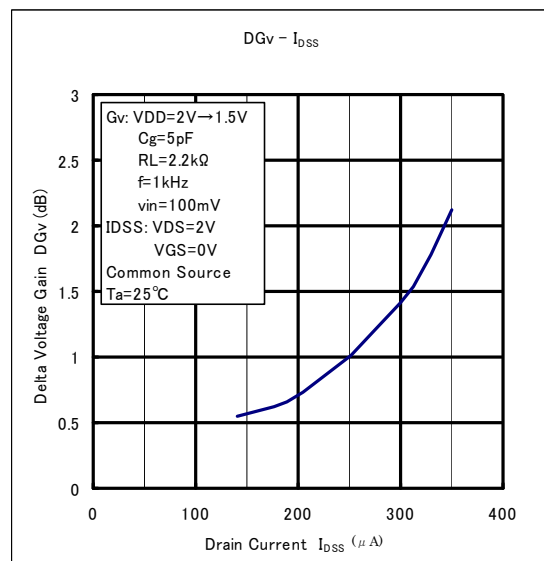
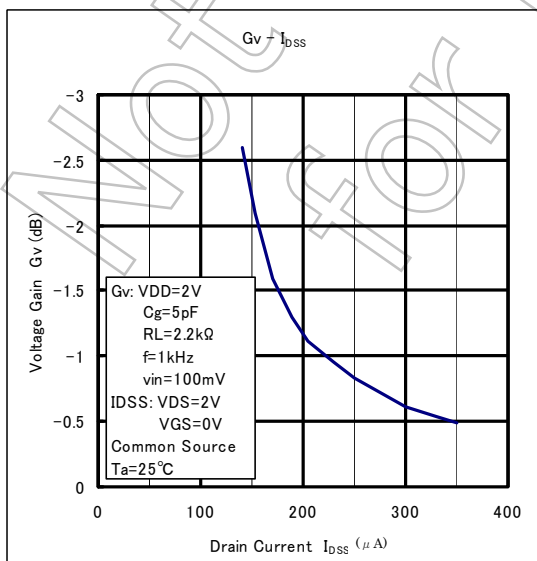
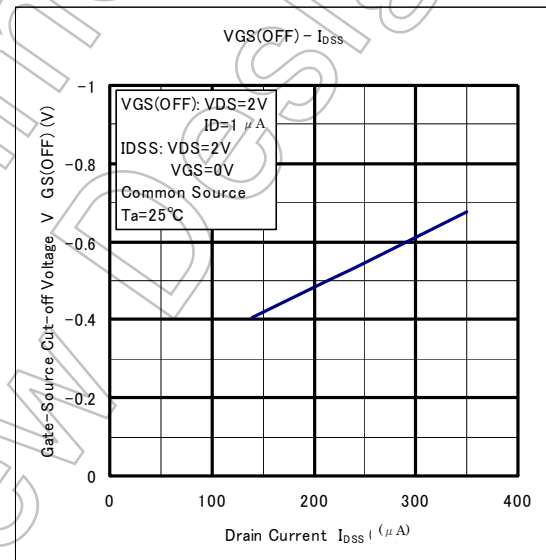
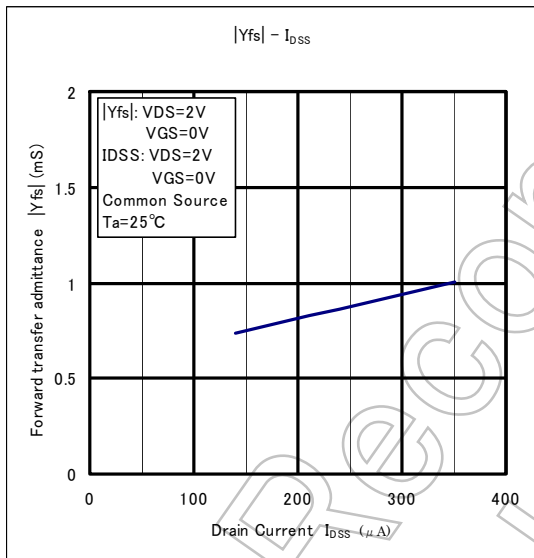
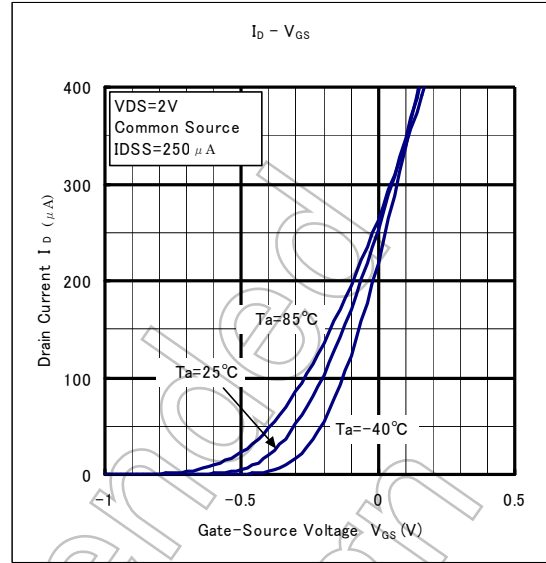
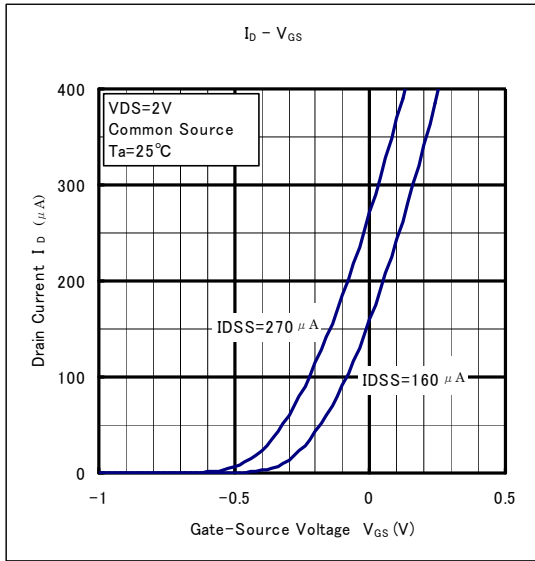
Time Output Stability Test Method

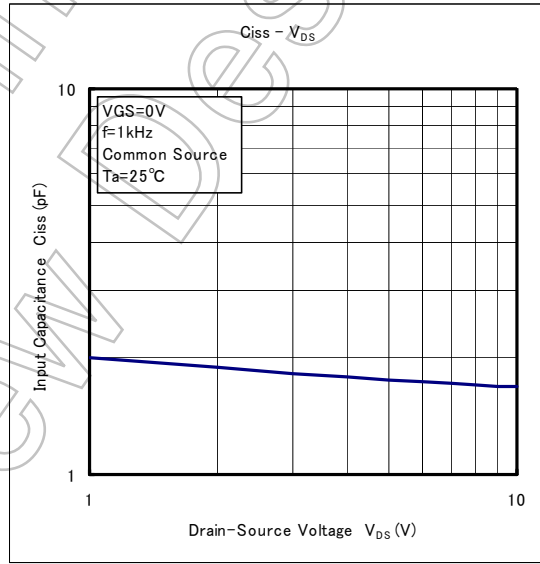
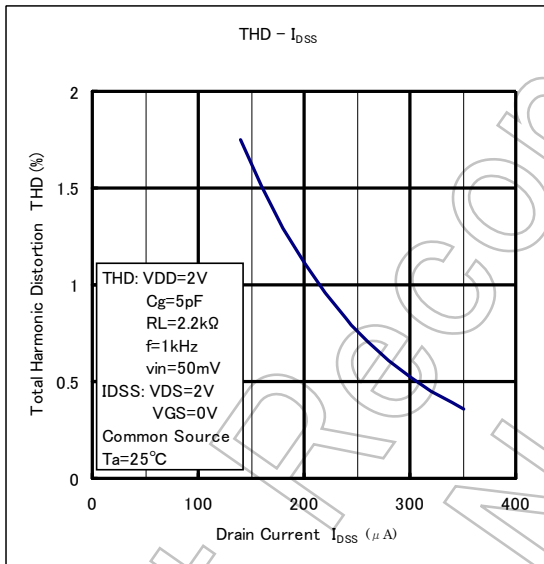
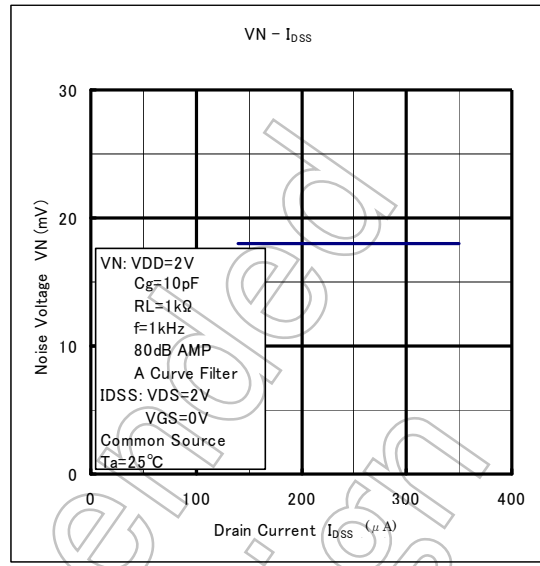
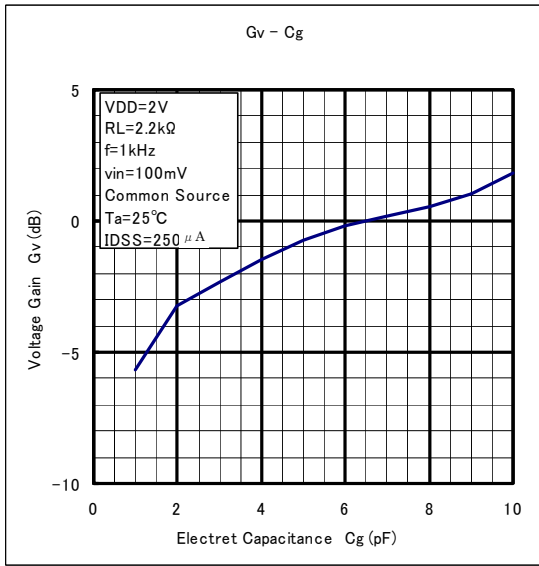
a) TEST CIRCUIT



b) TEST SIGNAL







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