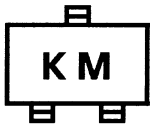


# 2SK2009

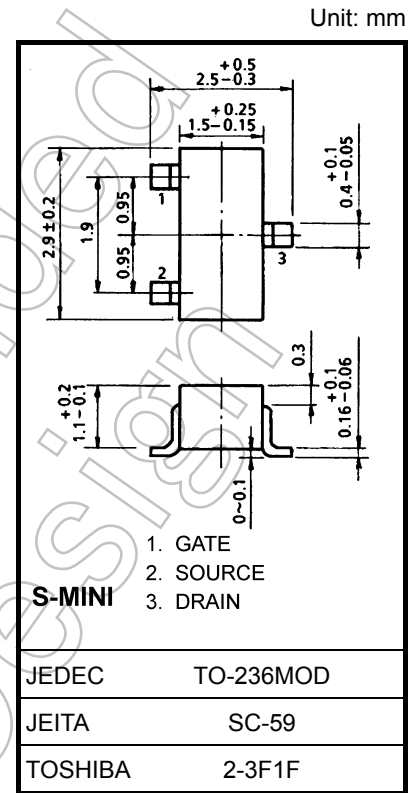
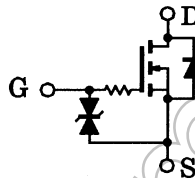
High Speed Switching Applications  
 Analog Switch Applications

- High input impedance.
- Low gate threshold voltage:  $V_{th} = 0.5$  to  $1.5$  V
- Excellent switching times:  $t_{on} = 0.06 \mu s$  (typ.)  
 $t_{off} = 0.12 \mu s$  (typ.)
- Low drain-source ON resistance:  $R_{DS(ON)} = 1.2 \Omega$  (typ.)
- Small package
- Enhancement-mode

**Marking**



**Equivalent Circuit**



Weight: 0.012 g (typ.)

**Absolute Maximum Ratings (Ta = 25°C)**

Characteristics	Symbol	Rating	Unit
Drain-source voltage	$V_{DS}$	30	V
Gate-source voltage	$V_{GSS}$	±20	V
DC drain current	$I_D$	200	mA
Drain power dissipation	$P_D$	200	mW
Channel temperature	$T_{ch}$	150	°C
Storage temperature range	$T_{stg}$	-55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

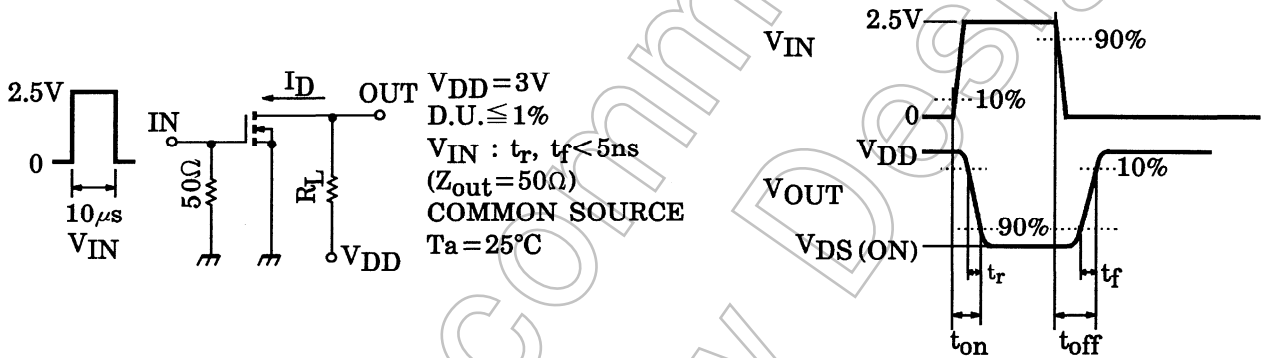
Note: This transistor is electrostatic sensitive device. Please handle with caution.

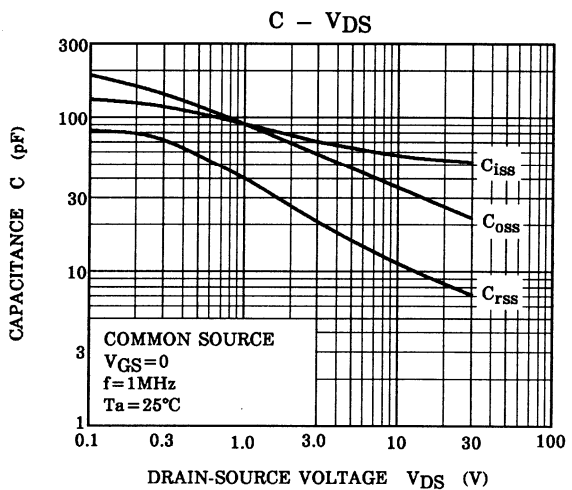
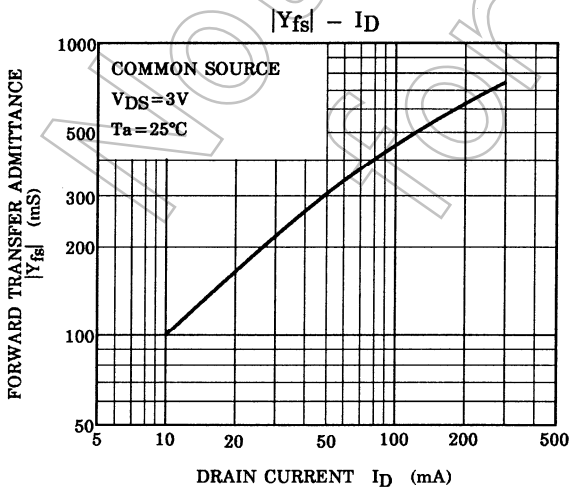
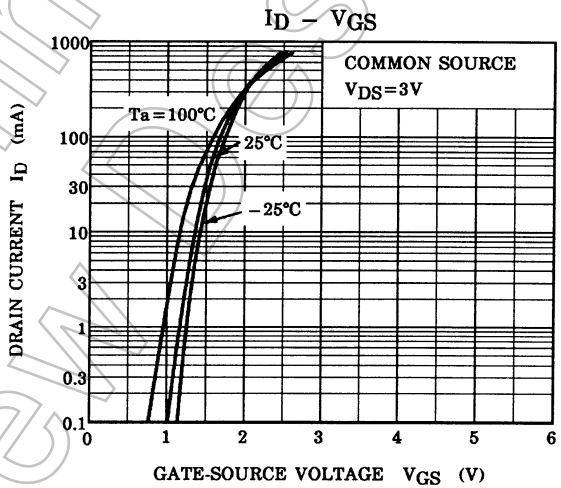
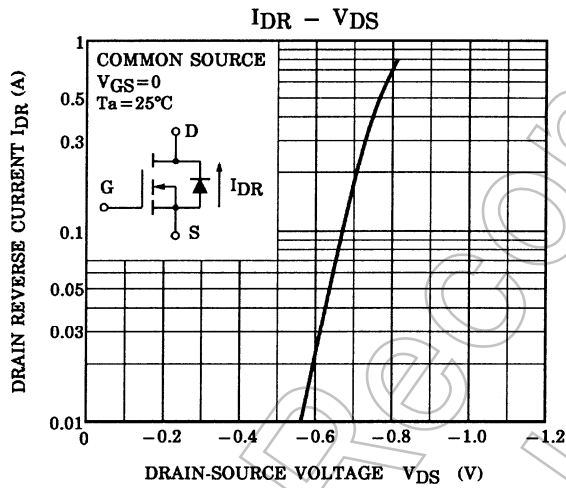
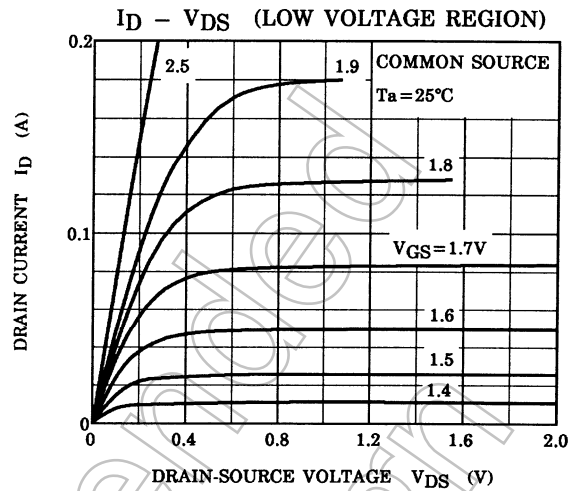
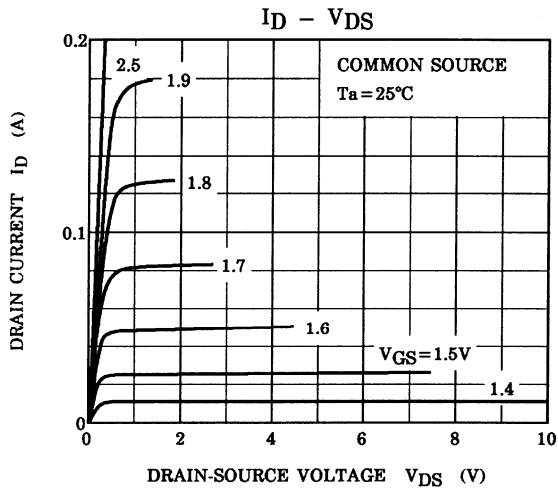
Start of commercial production  
 1992-04

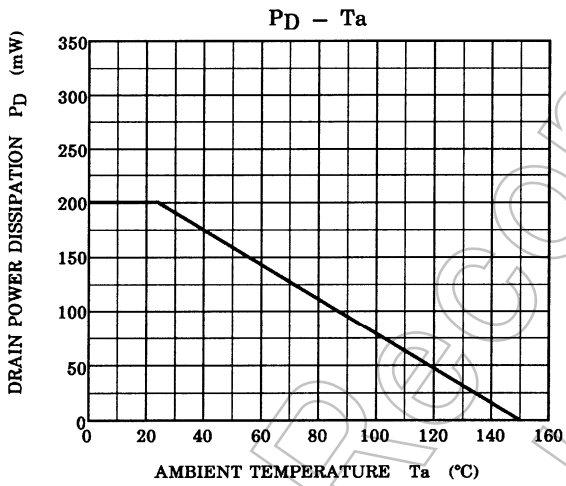
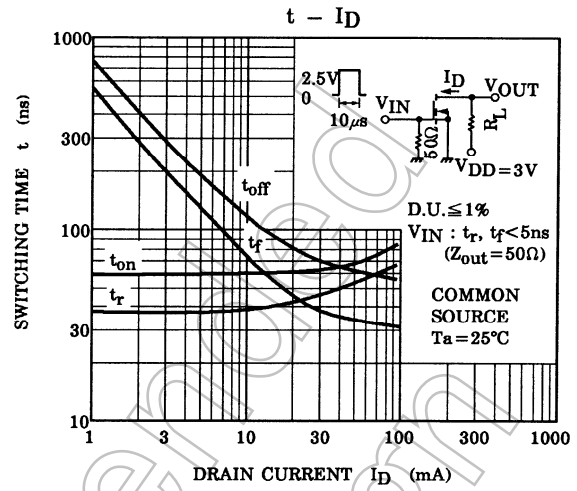
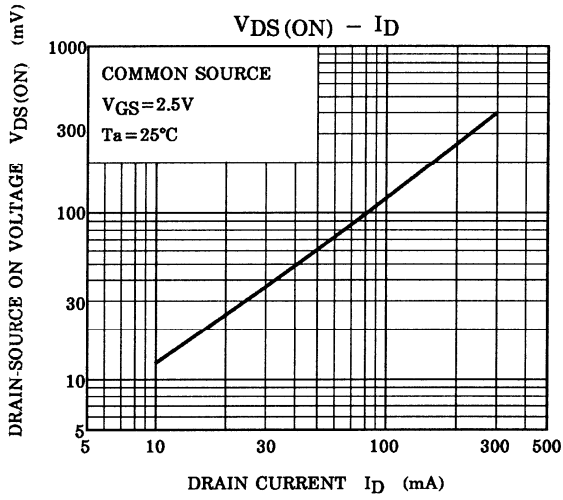
## Electrical Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	$I_{GSS}$	$V_{GS} = \pm 10\text{ V}, V_{DS} = 0$	—	—	$\pm 0.1$	$\mu\text{A}$
Drain-source breakdown voltage	$V_{(BR)DSS}$	$I_D = 1\text{ mA}, V_{GS} = 0$	30	—	—	V
Drain cut-off current	$I_{DSS}$	$V_{DS} = 30\text{ V}, V_{GS} = 0$	—	—	10	$\mu\text{A}$
Gate threshold voltage	$V_{th}$	$V_{DS} = 3\text{ V}, I_D = 0.1\text{ mA}$	0.5	—	1.5	V
Forward transfer admittance	$ Y_{fs} $	$V_{DS} = 3\text{ V}, I_D = 50\text{ mA}$	100	—	—	mS
Drain-source ON resistance	$R_{DS(ON)}$	$I_D = 50\text{ mA}, V_{GS} = 2.5\text{ V}$	—	1.2	2	$\Omega$
Input capacitance	$C_{iss}$	$V_{DS} = 3\text{ V}, V_{GS} = 0, f = 1\text{ MHz}$	—	70	—	pF
Reverse transfer capacitance	$C_{rss}$	$V_{DS} = 3\text{ V}, V_{GS} = 0, f = 1\text{ MHz}$	—	23	—	pF
Output capacitance	$C_{oss}$	$V_{DS} = 3\text{ V}, V_{GS} = 0, f = 1\text{ MHz}$	—	58	—	pF
Switching time	Turn-on time	$V_{DD} = 3\text{ V}, I_D = 10\text{ mA}, V_{GS} = 0\text{ to }2.5\text{ V}$	—	0.06	—	$\mu\text{s}$
	Turn-off time	$V_{DD} = 3\text{ V}, I_D = 10\text{ mA}, V_{GS} = 0\text{ to }2.5\text{ V}$	—	0.12	—	

## Switching Time Test Circuit







Not for New Design

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