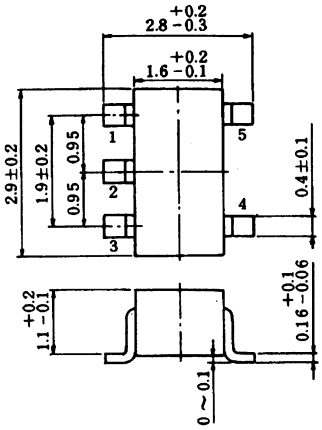
TOSHIBA Field Effect Transistor Silicon N Channel Junction Type

2SK2145

Audio Frequency Low Noise Amplifier Applications

- Including two devices in SM5 (super mini type with 5 leads.)
- High $|Y_{fs}|$: $|Y_{fs}|$ = 15 mS (typ.) at V_{DS} = 10 V, V_{GS} = 0
- High breakdown voltage: V_{GDS} = −50 V
- Low noise: NF = 1.0dB (typ.)
  at V_{DS} = 10 V, I_D = 0.5 mA, f = 1 kHz, R_g = 1 kΩ
- High input impedance: I_{GSS} = −1 nA (max) at V_{GS} = −30 V

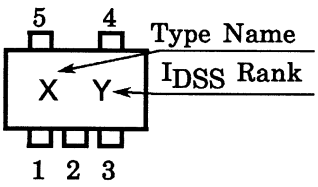
Unit: mm



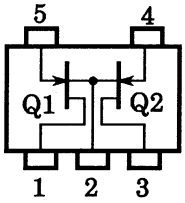
SMV	
JEDEC	—
JEITA	—
TOSHIBA	2-3L1C

Weight: 0.016 g (typ.)

Marking



Pin Assignment (top view)



Absolute Maximum Ratings (Ta = 25°C) (Q1, Q2 common)

Characteristics	Symbol	Rating	Unit
Gate-drain voltage	V_{GDS}	−50	V
Gate current	I_G	10	mA
Drain power dissipation	P_D (Note 1)	300	mW
Junction temperature	T_j	125	°C
Storage temperature	T_{stg}	−55 to 125	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Total rating

Start of commercial production
1993-03

Electrical Characteristics (Ta = 25°C) (Q1, Q2 common)

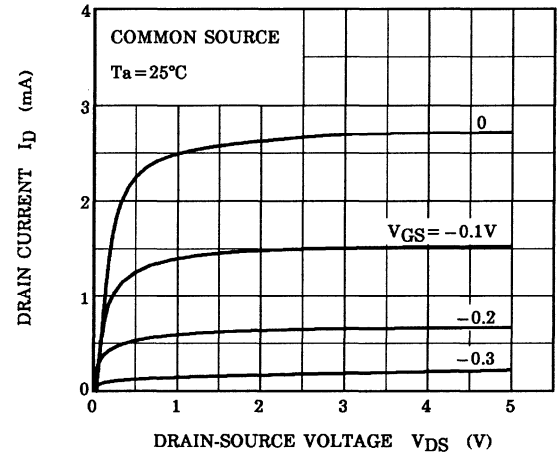
Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate-leakage current	I_{GSS}	V_{GS} = −30 V, V_{DS} = 0	—	—	−1.0	nA
Gate-drain breakdown voltage	$V_{(BR)\ GDS}$	V_{DS} = 0, I_G = −100 μA	−50	—	—	V
Drain current	I_{DSS} (Note 2)	V_{DS} = 10 V, V_{GS} = 0	1.2	—	14.0	mA
Gate-source cut-off voltage	$V_{GS\ (OFF)}$	V_{DS} = 10 V, I_D = 0.1 μA	−0.2	—	−1.5	V
Forward transfer admittance	$\|Y_{fs}\|$	V_{DS} = 10 V, V_{GS} = 0, f = 1 kHz	4.0	15	—	mS
Input capacitance	C_{iss}	V_{DS} = 10 V, V_{GS} = 0, f = 1 MHz	—	13	—	pF
Reverse transfer capacitance	C_{rss}	V_{DG} = 10 V, I_D = 0, f = 1 MHz	—	3	—	pF
Noise figure	NF (1)	V_{DS} = 10 V, R_g = 1 kΩ I_D = 0.5 mA, f = 10 Hz	—	5	—	dB
	NF (2)	V_{DS} = 10 V, R_g = 1 kΩ I_D = 0.5 mA, f = 1 kHz	—	1	—	

Note 2: I_{DSS} classification Y (Y): 1.2 to 3.0 mA, GR (G): 2.6 to 6.5 mA, BL (L): 6.0 to 14.0 mA

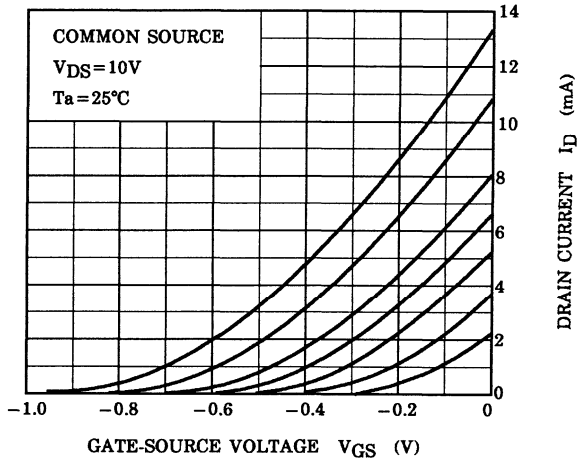
( ) Marking symbol

(Q1, Q2 common)

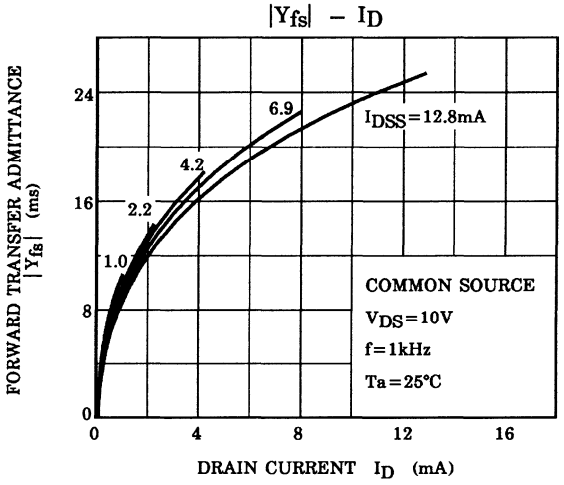
$I_D - V_{DS}$



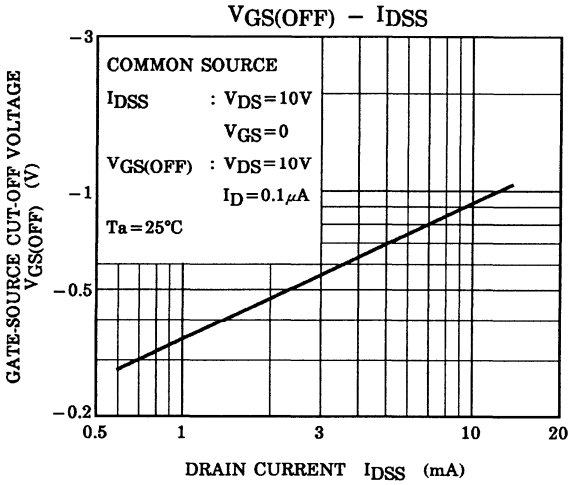
$I_D - V_{GS}$



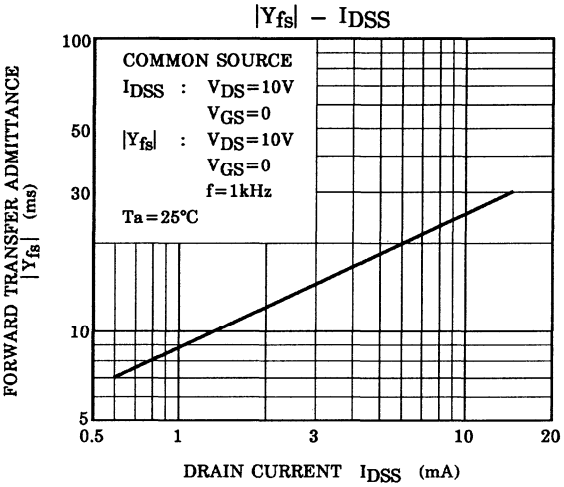
$|Y_{fs}| - I_D$



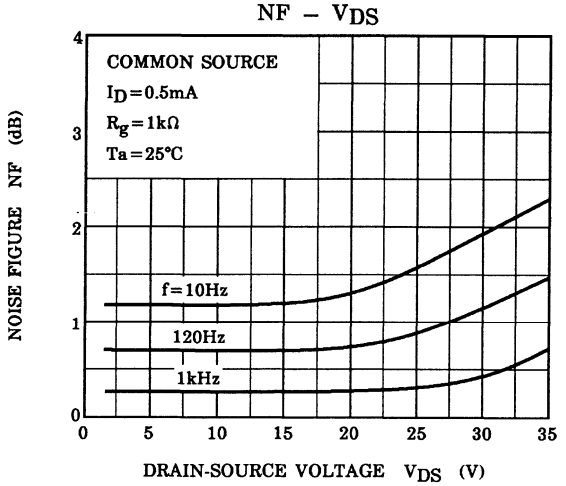
$V_{GS(OFF)} - I_{DSS}$



$|Y_{fs}| - I_{DSS}$

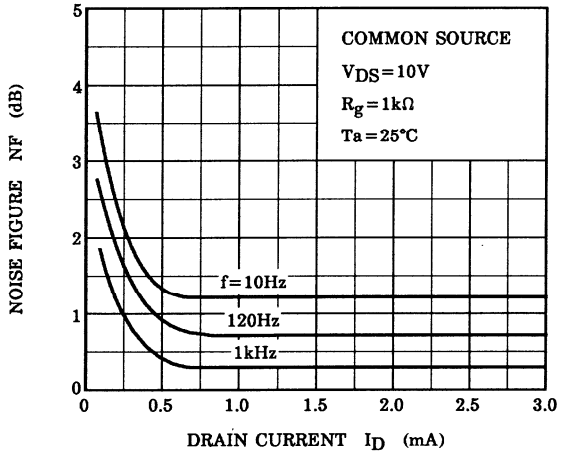


NF − V_{DS}

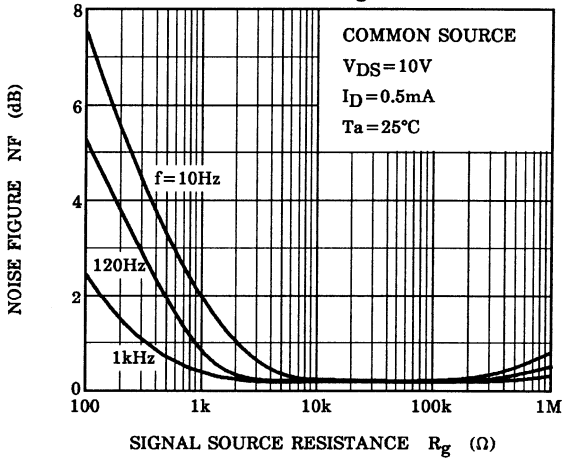


(Q1, Q2 common)

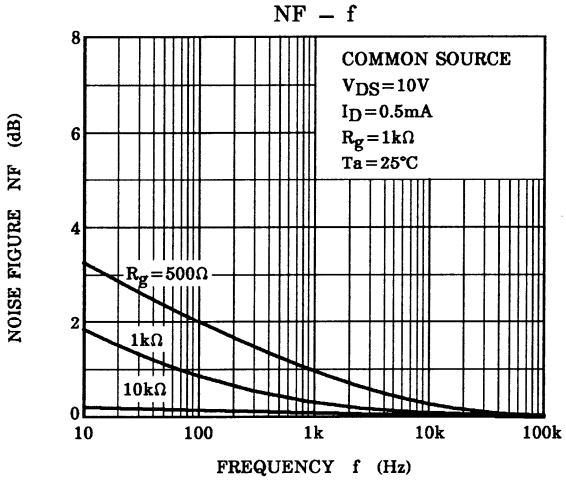
NF – I_D



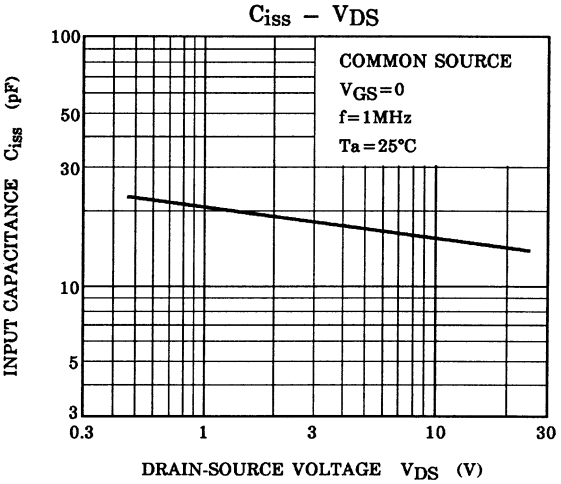
NF – R_g



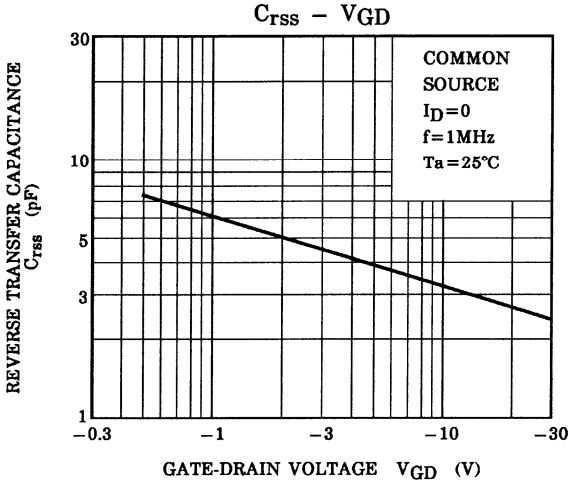
NF – f



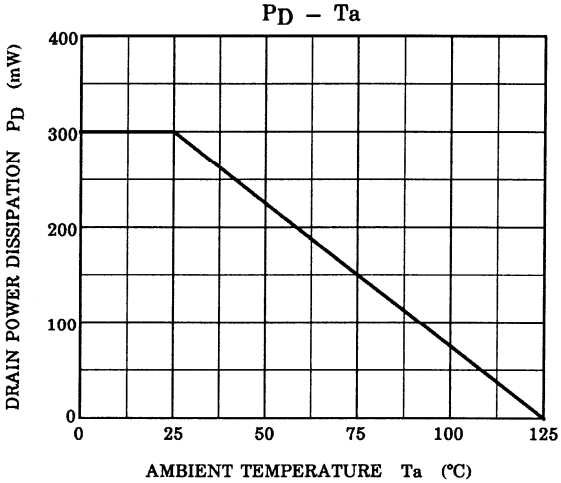
C_{iss} – V_{DS}



C_{rss} – V_{GD}



P_D – Ta



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