TOSHIBA Field Effect Transistor Silicon N Channel MOS Type

SSM6N17FU

High Speed Switching Applications

Analog Switch Applications

- Suitable for high-density mounting due to compact package
- High drain-source voltage
- High speed switching

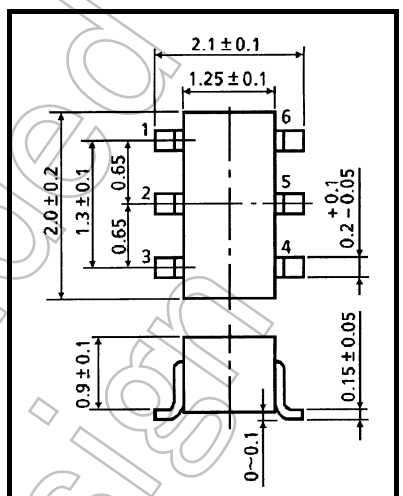
Absolute Maximum Ratings (Ta = 25°C) (Q1, Q2 Common)

Characteristics		Symbol	Rating	Unit
Drain-Source voltage		V_{DS}	50	V
Gate-Source voltage		V_{GSS}	±7	V
Drain current	DC	I_D	100	mA
	Pulse	I_{DP}	200	
Drain power dissipation (Ta = 25°C)		P_D(Note 1)	200	mW
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

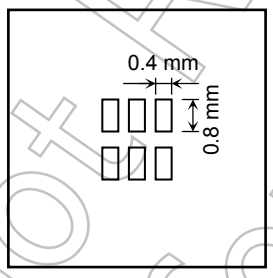
Note 1: Total rating,Mounted on FR4 board
(25.4 mm × 25.4 mm × 1.6 t, Cu Pad: 0.32 mm^2 × 6)

Unit: mm

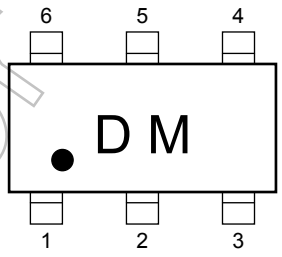


US6	
JEDEC	—
JEITA	SC-70 (6pin)
TOSHIBA	2-2J1C

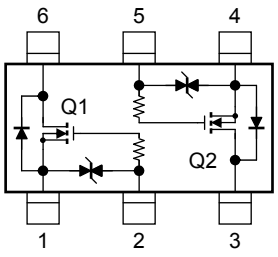
Weight: 6.8 mg (typ.)



Marking



Equivalent Circuit



This transistor is a electrostatic sensitive device. Please handle with caution.

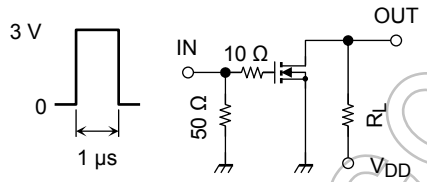
Start of commercial production
2001-11

Electrical Characteristics (Ta = 25°C) (Q1, Q2 Common)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±7 V, V_{DS} = 0	—	—	±5	μA
Drain-Source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 0.1 mA, V_{GS} = 0	50	—	—	V
Drain cut-off current		I_{DSS}	V_{DS} = 50 V, V_{GS} = 0	—	—	1	μA
Gate threshold voltage		V_{th}	V_{DS} = 3 V, I_D = 1 μA	0.9	—	1.5	V
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 3 V, I_D = 10 mA	20	40	—	mS
Drain-Source ON resistance		$R_{DS\ (ON)}$	I_D = 10 mA, V_{GS} = 4 V	—	12	20	Ω
			I_D = 10 mA, V_{GS} = 2.5 V	—	22	40	
Input capacitance		C_{iss}	V_{DS} = 3 V, V_{GS} = 0, f = 1 MHz	—	7	—	pF
Reverse transfer capacitance		C_{rss}		—	3	—	pF
Output capacitance		C_{oss}		—	7	—	pF
Switching time	Turn-on time	t_{on}	V_{DD} = 3 V, I_D = 20 mA, V_{GS} = 0 to 3 V, R_G = 10 Ω, R_L = 150 Ω	—	100	—	ns
	Turn-off time	t_{off}		—	40	—	

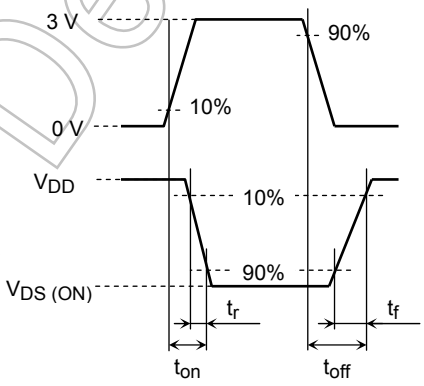
Switching Time Test Circuit

(a) Test circuit



V_{DD} = 3 V
Duty ≤ 1%
V_{IN}: t_r, t_f < 5 ns
(Z_{out} = 50 Ω)
Common source
Ta = 25°C

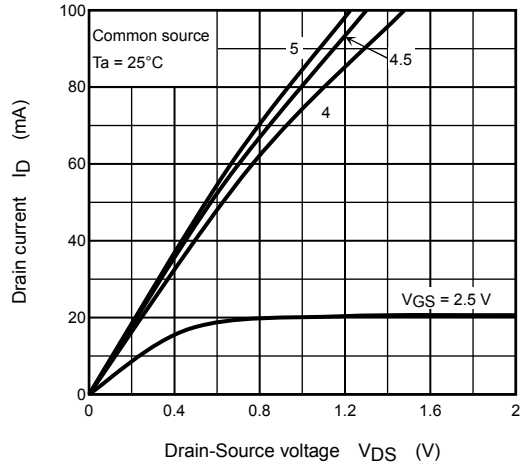
(b) V_{IN}



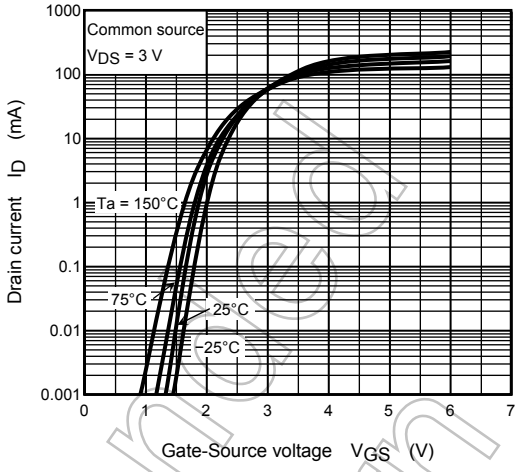
(c) V_{OUT}

(Q1, Q2 Common)

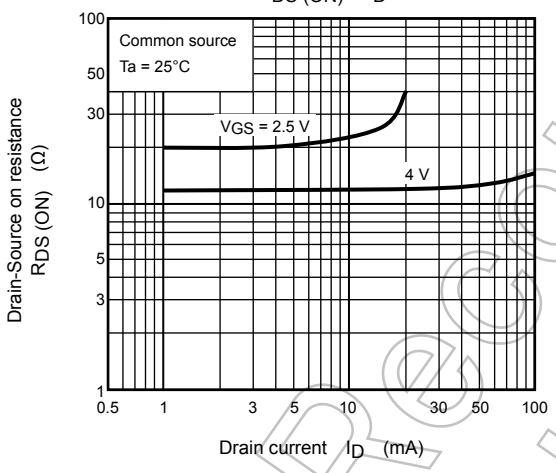
$I_D - V_{DS}$



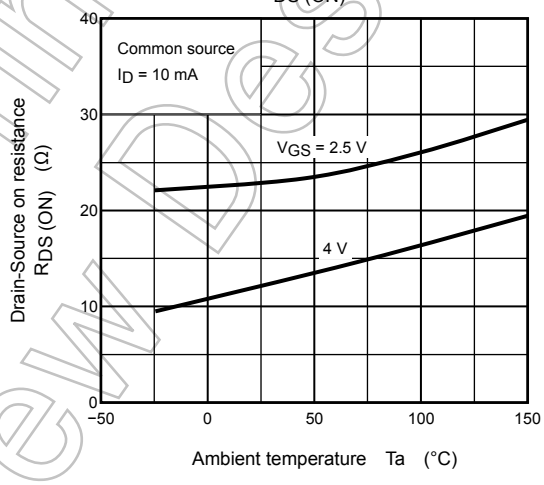
$I_D - V_{GS}$



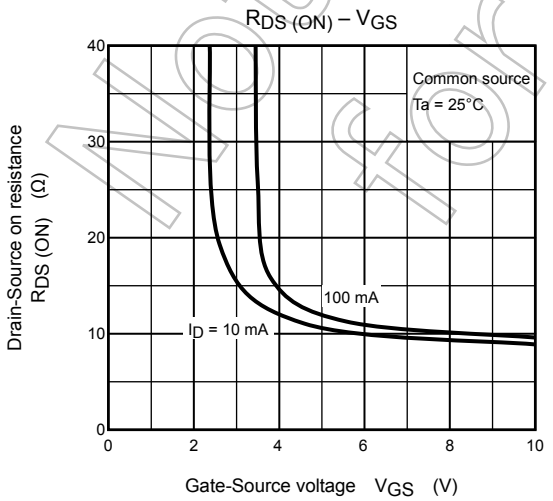
$R_{DS\ (ON)} - I_D$



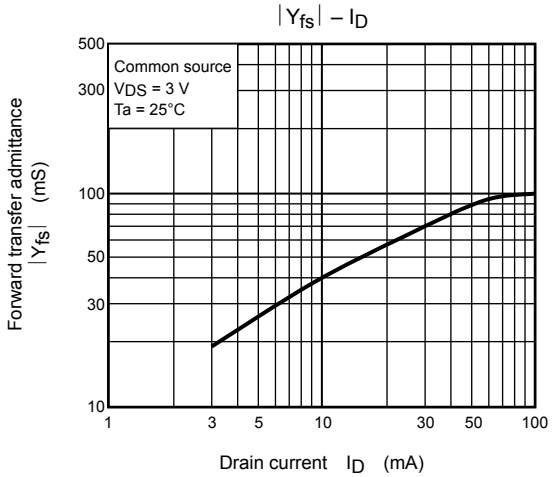
$R_{DS\ (ON)} - Ta$



$R_{DS\ (ON)} - V_{GS}$

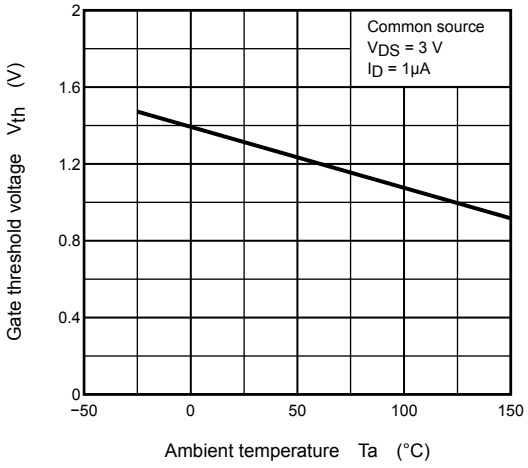


$|Y_{fs}| - I_D$

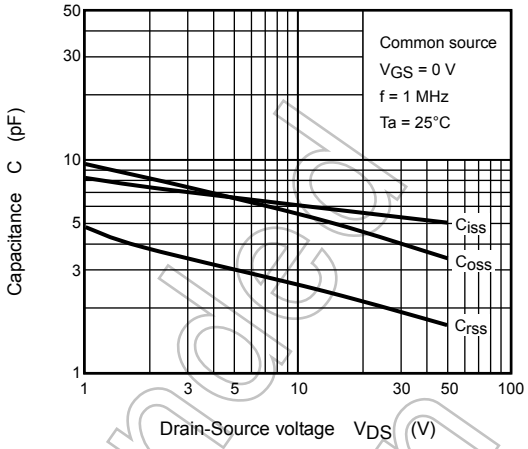


(Q1, Q2 Common)

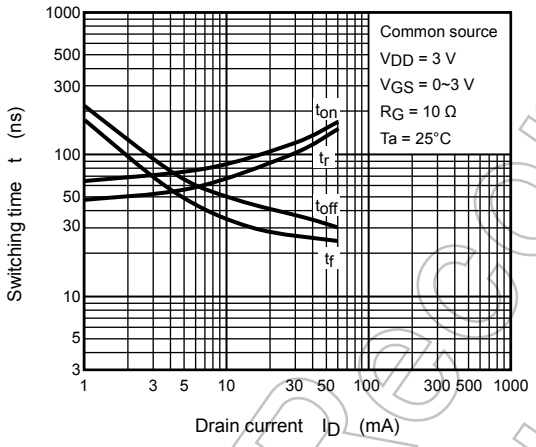
V_{th} – Ta



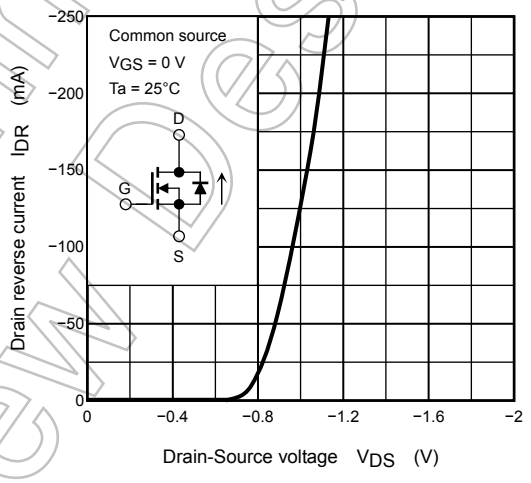
C – V_{DS}



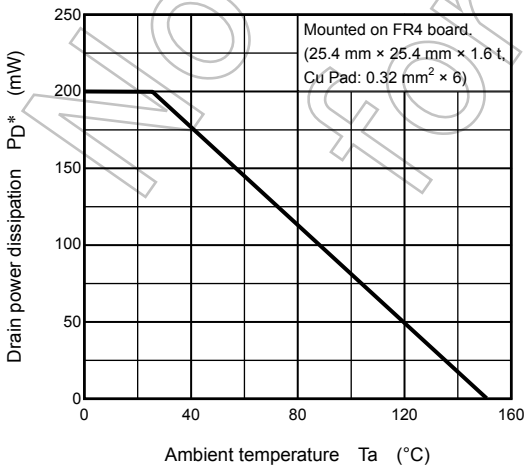
t – I_D



I_{DR} – V_{DS}



P_D* – Ta



*: Total rating

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