

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

# TC7WT241FU

## Non-Inverted, 3-State Outputs

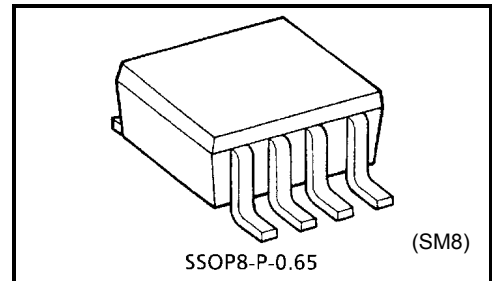
The TC7WT241FU is a high speed CMOS Dual Bus Buffers fabricated with silicon gate CMOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The input threshold levels are compatible with TTL output voltage.

It is a non-inverting 3-state buffer has one active-high and one active-low output enable.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

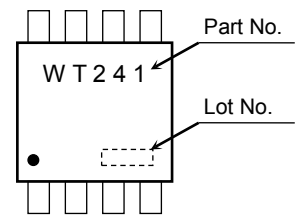


Weight: 0.02 g (typ.)

## Features

- High speed:  $t_{pd} = 13 \text{ ns}$  (typ.) at  $V_{CC} = 5 \text{ V}$
- Low power dissipation:  $I_{CC} = 2 \mu\text{A}$  (max) at  $T_a = 25 \text{ }^\circ\text{C}$
- High noise immunity:  $V_{IL} = 0.8 \text{ V}$  (max),  $V_{IH} = 2.0 \text{ V}$  (min)
- Output drive capability: 15 LSTTL loads
- Symmetrical output impedance:  $|I_{OH}| = I_{OL} = 6 \text{ mA}$  (min)

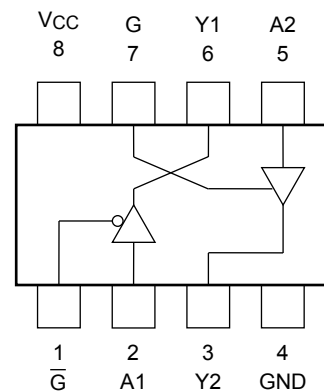
## Marking



## Absolute Maximum Ratings ( $T_a = 25^\circ\text{C}$ )

Characteristics	Symbol	Rating	Unit
Supply voltage range	$V_{CC}$	-0.5 to 7	V
DC input voltage	$V_{IN}$	-0.5 to $V_{CC} + 0.5$	V
DC output voltage	$V_{OUT}$	-0.5 to $V_{CC} + 0.5$	V
Input diode current	$I_{IK}$	$\pm 20$	mA
Output diode current	$I_{OK}$	$\pm 20$	mA
DC output current	$I_{OUT}$	$\pm 35$	mA
DC $V_{CC}$ /ground current	$I_{CC}$	$\pm 37.5$	mA
Power dissipation	$P_D$	300	mW
Storage temperature range	$T_{stg}$	-65 to 150	$^\circ\text{C}$
Lead temperature (10 s)	$T_L$	260	$^\circ\text{C}$

## Pin Configuration (top view)

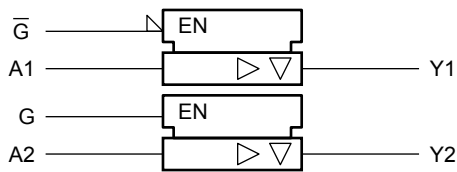


Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Start of commercial production  
1996-09

## Logic Diagram



## Truth Table

Inputs			Output
$\bar{G}$	G	A	Y
L	H	L	L
L	H	H	H
H	L	X	Z

X: Don't care  
Z: High impedance

## Operating Ranges

Characteristics	Symbol	Rating	Unit
Supply voltage	$V_{CC}$	4.5 to 5.5	V
Input voltage	$V_{IN}$	0 to $V_{CC}$	V
Output voltage	$V_{OUT}$	0 to $V_{CC}$	V
Operating temperature range	$T_{opr}$	-40 to 85	°C
Input rise and fall time	$t_r, t_f$	0 to 500	ns

## Electrical Characteristics

### DC Electrical Characteristics

Characteristics	Symbol	Test Condition	$V_{CC}$ (V)	$T_a = 25^\circ\text{C}$			$T_a = -40 \text{ to } 85^\circ\text{C}$		Unit		
				Min	Typ.	Max	Min	Max			
Input voltage	High level	$V_{IH}$	4.5 to 5.5	2.0	—	—	2.0	—	V		
	Low level	$V_{IL}$	4.5 to 5.5	—	—	0.8	—	0.8			
Output voltage	High level	$V_{OH}$	$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -20 \mu\text{A}$	4.5	4.4	4.5	—	4.4	—	V
				$I_{OH} = -6 \text{ mA}$	4.5	4.18	4.31	—	4.13	—	
	Low level	$V_{OL}$	$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 20 \mu\text{A}$	4.5	—	0	0.1	—	0.1	
				$I_{OL} = 6 \text{ mA}$	4.5	—	0.17	0.26	—	0.33	
3-state output off-state current	$I_{OZ}$	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $V_{OUT} = V_{CC} \text{ or } GND$	5.5	—	—	$\pm 0.5$	—	$\pm 5.0$	$\mu\text{A}$		
Input leakage current	$I_{IN}$	$V_{IN} = V_{CC} \text{ or } GND$	5.5	—	—	$\pm 0.1$	—	$\pm 1.0$	$\mu\text{A}$		
Quiescent supply current	$I_{CC}$	$V_{IN} = V_{CC} \text{ or } GND$	5.5	—	—	2.0	—	20.0	$\mu\text{A}$		
	$I_{CCT}$	PER INPUT : $V_{IN} = 0.5\text{V or } 2.4\text{V}$ OTHER INPUT : $V_{CC} \text{ or } GND$	5.5	—	—	2.0	—	2.9	mA		

## AC Electrical Characteristics (input $t_r = t_f = 6$ ns)

Characteristics	Symbol	Test Condition			Ta = 25°C			Ta = -40 to 85°C		Unit
			CL(pF)	VCC (V)	Min	Typ.	Max	Min	Max	
Output transition time	tTLH	—	50	4.5	—	7	12	—	15	ns
	tTHL			5.5	—	6	11	—	14	
Propagation delay time	tPLH	—	50	4.5	—	15	25	—	31	ns
				5.5	—	13	22	—	28	
	tPHL		150	4.5	—	21	33	—	41	
				5.5	—	18	29	—	37	
Output enable time	tPZL	RL = 1 kΩ	50	4.5	—	17	30	—	38	ns
				5.5	—	14	27	—	34	
	tPZH		150	4.5	—	23	38	—	48	
				5.5	—	20	34	—	43	
Output disable time	tPLZ	RL = 1 kΩ	50	4.5	—	16	30	—	38	ns
				tPHZ	5.5	—	13	27	—	
Input capacitance	CIN	—	—	—	—	5	10	—	10	pF
Output capacitance	COUT	—	—	—	—	10	—	—	—	pF
Power dissipation capacitance	CPD	(Note)	—	—	—	32	—	—	—	pF

Note: CPD is defined as the value of internal equivalent capacitance which is calculated from the operating current consumption without load.

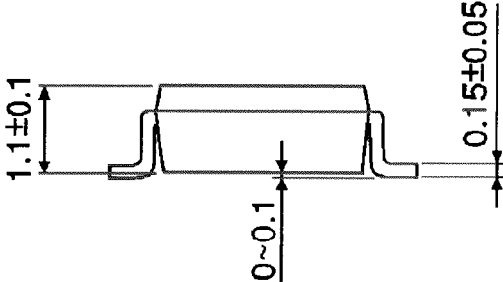
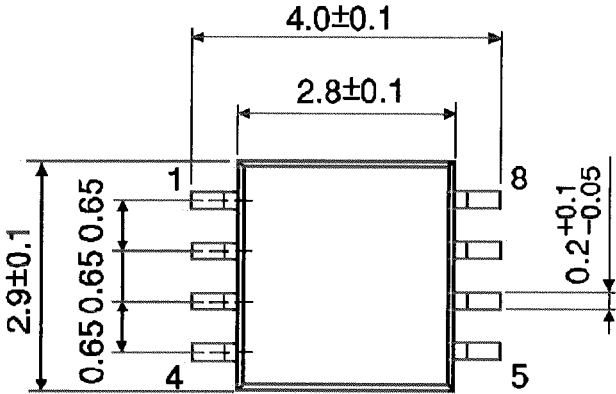
Average operating current can be obtained by the equation:

$$I_{CC (opr.)} = CPD \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \text{ (per gate)}$$

**Package Dimensions**

SSOP8-P-0.65

Unit : mm



Weight: 0.02 g (typ.)

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