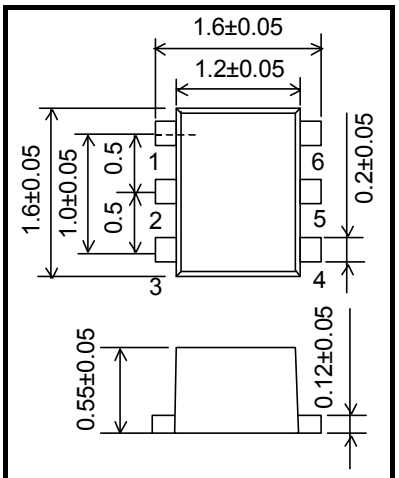
TOSHIBA Field Effect Transistor Silicon N Channel MOS Type (U-MOSIII)

# SSM6K24FE

## High Speed Switching Applications

- Optimum for high-density mounting in small packages
- Low on-resistance: $R_{on}$ = 145mΩ (max) (@$V_{GS}$ = 4.5 V)
  $R_{on}$ = 180mΩ (max) (@$V_{GS}$ = 2.5 V)

Unit: mm




1,2,5,6 :Drain
3 :Gate
4 :Source

| | |
|---|---|
| ES6 | |
| JEDEC | — |
| JEITA | — |
| TOSHIBA | 2-2N1A |

Weight: 3.0 mg (typ.)

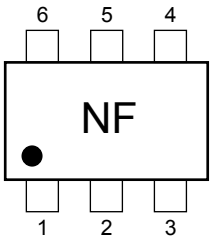
## Absolute Maximum Ratings (Ta = 25°C)

| Characteristics | | Symbol | Rating | Unit |
|---|---|---|---|---|
| Drain-Source voltage | | $V_{DS}$ | 30 | V |
| Gate-Source voltage | | $V_{GSS}$ | ± 12 | V |
| Drain current | DC | $I_D$ | 0.5 | A |
| | Pulse | $I_{DP}$ | 1.5 | |
| Drain power dissipation | | $P_D$ (Note 1) | 500 | mW |
| Channel temperature | | $T_{ch}$ | 150 | °C |
| Storage temperature range | | $T_{stg}$ | −55 to 150 | °C |

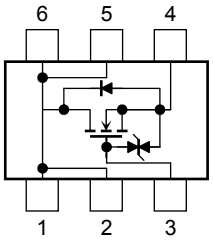
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Mounted on FR4 board.
(25.4 mm × 25.4 mm × 1.6 t, Cu Pad: 645 $mm^2$ )

## Marking




## Equivalent Circuit (top view)




## Handling Precaution

When handling individual devices (which are not yet mounted on a circuit board), be sure that the environment is protected against electrostatic electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

Start of commercial production
2004-01

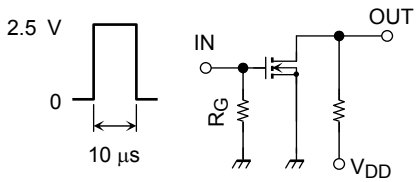
## Electrical Characteristics (Ta = 25°C)

| Characteristics | | Symbol | Test Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|
| Gate leakage current | | $I_{GSS}$ | $V_{GS}$ = ±□12 V, $V_{DS}$ = 0 | — | — | ±1 | μA |
| Drain-Source breakdown voltage | | $V_{(BR)\ DSS}$ | $I_D$ = 1 mA, $V_{GS}$ = 0 | 30 | — | — | V |
| | | $V_{(BR)\ DSX}$ | $I_D$ = 1 mA, $V_{GS}$ = −12 V | 18 | — | — | |
| Drain cut-off current | | $I_{DSS}$ | $V_{DS}$ = 30 V, $V_{GS}$ = 0 | — | — | 1 | μA |
| Gate threshold voltage | | $V_{th}$ | $V_{DS}$ = 3 V, $I_D$ = 0.1 mA | 0.5 | — | 1.1 | V |
| Forward transfer admittance | | $\|Y_{fs}\|$ | $V_{DS}$ = 3 V, $I_D$ = 0.25 A (Note2) | 1.0 | 2.0 | — | S |
| Drain-Source on-resistance | | $R_{DS\ (ON)}$ | $I_D$ = 0.50 A, $V_{GS}$ = 4.5 V (Note2) | — | 120 | 145 | mΩ |
| | | | $I_D$ = 0.25 A, $V_{GS}$ = 2.5 V (Note2) | — | 140 | 180 | |
| Input capacitance | | $C_{iss}$ | $V_{DS}$ = 10 V, $V_{GS}$ = 0, f = 1 MHz | — | 245 | — | pF |
| Reverse transfer capacitance | | $C_{rss}$ | $V_{DS}$ = 10 V, $V_{GS}$ = 0, f = 1 MHz | — | 33 | — | pF |
| Output capacitance | | $C_{oss}$ | $V_{DS}$ = 10 V, $V_{GS}$ = 0, f = 1 MHz | — | 41 | — | pF |
| Switching time | Turn-on time | $t_{on}$ | $V_{DD}$ = 10 V, $I_D$ = 0.25 A, | — | 9 | — | ns |
| | Turn-off time | $t_{off}$ | $V_{GS}$ = 0~2.5 V, $R_G$ = 4.7 Ω | — | 15 | — | |

Note2: Pulse test

## Switching Time Test Circuit

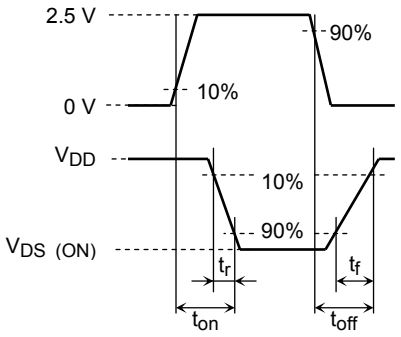
### (a) Test Circuit




$V_{DD}$ = 10 V
$R_G$ = 4.7 Ω
Duty ≤ 1%
$V_{IN}$: $t_r$, $t_f$ < 5 ns
Common Source
Ta = 25°C

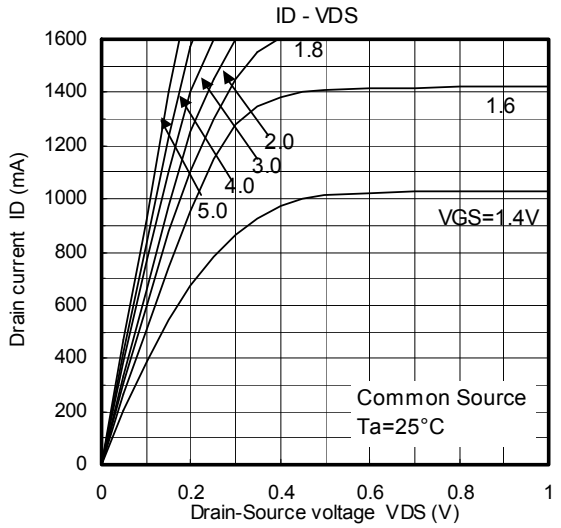
### (b) $V_{IN}$

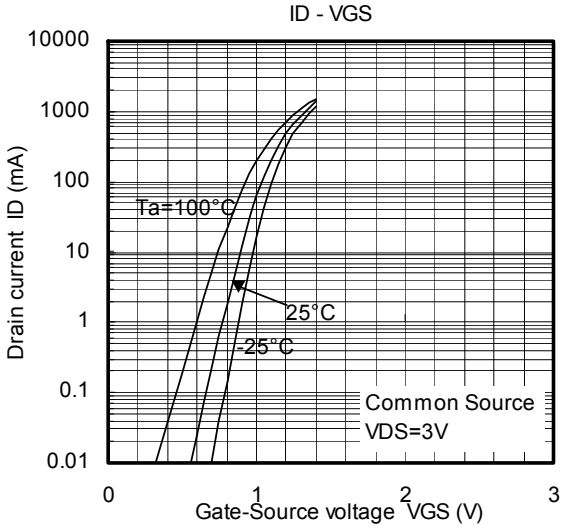
### (c) $V_{OUT}$

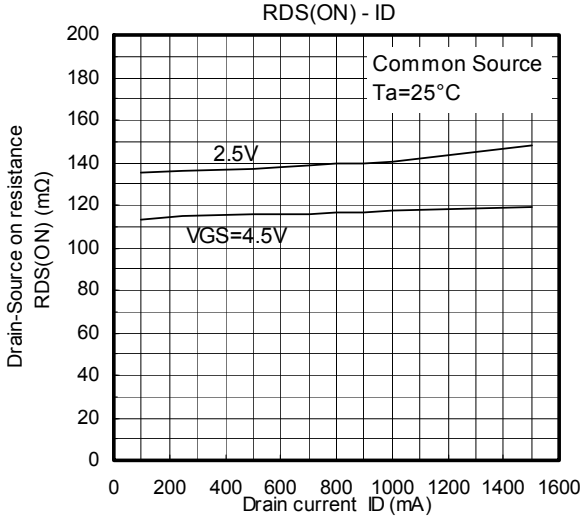


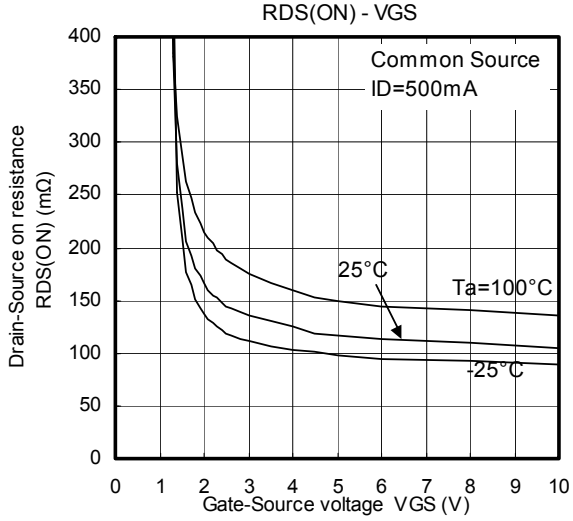

## Precaution

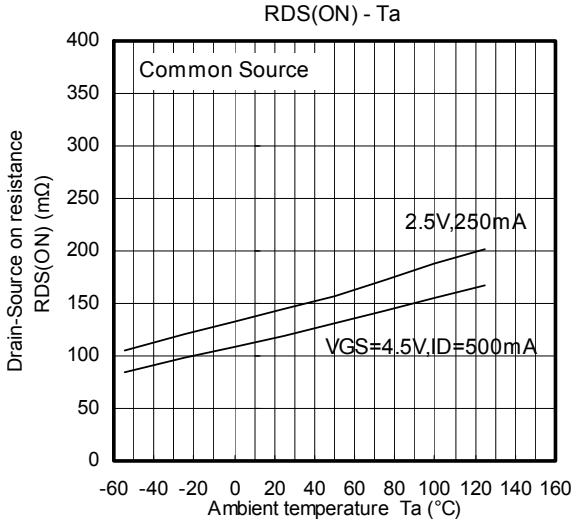
$V_{th}$ can be expressed as the voltage between gate and source when the low operating current value is $I_D$ = 100 μA for this product. For normal switching operation, $V_{GS\ (on)}$ requires a higher voltage than $V_{th}$ and $V_{GS\ (off)}$ requires a lower voltage than $V_{th}$.
(The relationship can be established as follows: $V_{GS\ (off)} < V_{th} < V_{GS\ (on)}$ )
Please take this into consideration when using the device.

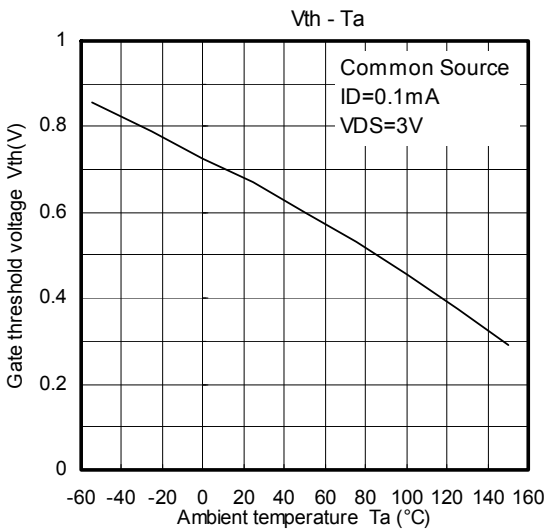

ID - VDS
Drain current ID (mA)
Drain-Source voltage VDS (V)
1.8
1.6
2.0
3.0
4.0
5.0
VGS=1.4V
Common Source
Ta=25°C

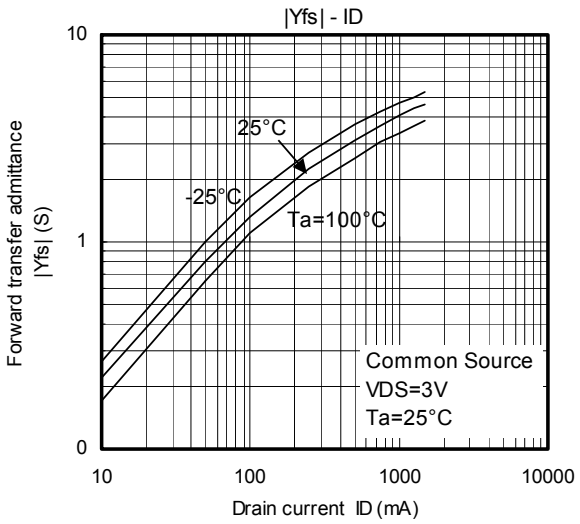

ID - VGS
Drain current ID (mA)
Gate-Source voltage VGS (V)
Ta=100°C
25°C
-25°C
Common Source
VDS=3V

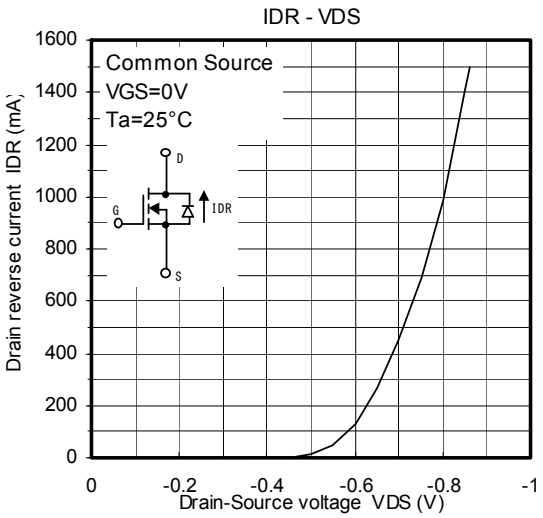

RDS(ON) - ID
Drain-Source on resistance RDS(ON) (mΩ)
Drain current ID (mA)
Common Source
Ta=25°C
2.5V
VGS=4.5V

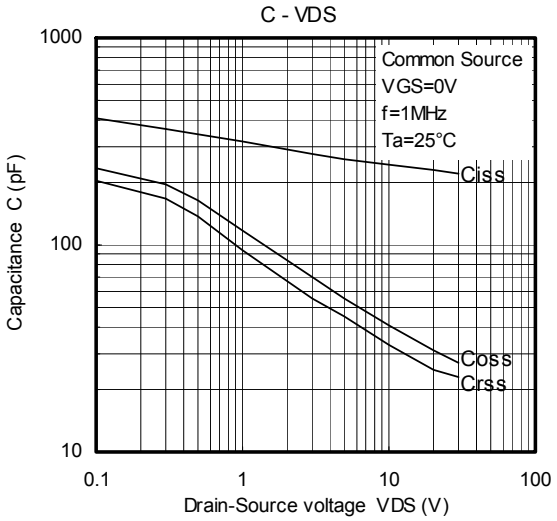

RDS(ON) - VGS
Drain-Source on resistance RDS(ON) (mΩ)
Gate-Source voltage VGS (V)
Common Source
ID=500mA
25°C
Ta=100°C
-25°C

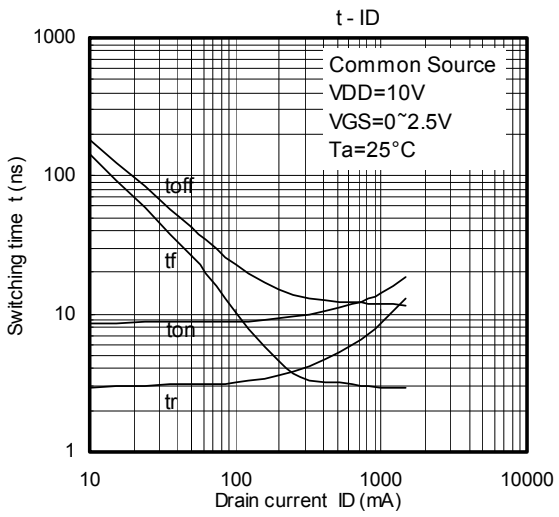

RDS(ON) - Ta
Drain-Source on resistance RDS(ON) (mΩ)
Ambient temperature Ta (°C)
Common Source
2.5V,250mA
VGS=4.5V,ID=500mA

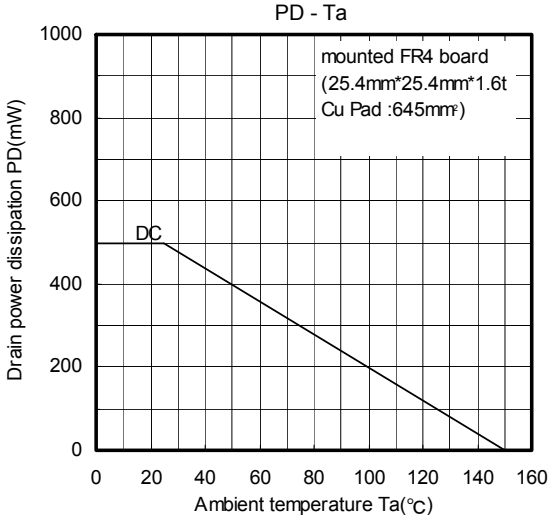

Vth - Ta
Gate threshold voltage Vth(V)
Ambient temperature Ta (°C)
Common Source
ID=0.1mA
VDS=3V


|Yfs| - ID
Forward transfer admittance |Yfs| (S)
Drain current ID (mA)
25°C
-25°C
Ta=100°C
Common Source
VDS=3V
Ta=25°C
10
1
0
10
100
1000
10000


IDR - VDS
Drain reverse current IDR (mA)
Drain-Source voltage VDS (V)
Common Source
VGS=0V
Ta=25°C
D
G
S
IDR
1600
1400
1200
1000
800
600
400
200
0
0
-0.2
-0.4
-0.6
-0.8
-1


C - VDS
Capacitance C (pF)
Drain-Source voltage VDS (V)
Common Source
VGS=0V
f=1MHz
Ta=25°C
Ciss
Coss
Crss
1000
100
10
0.1
1
10
100


t - ID
Switching time t (ns)
Drain current ID (mA)
Common Source
VDD=10V
VGS=0~2.5V
Ta=25°C
toff
tf
ton
tr
1000
100
10
1
10
100
1000
10000


PD - Ta
Drain power dissipation PD(mW)
Ambient temperature Ta(°C)
mounted FR4 board
(25.4mm*25.4mm*1.6t
Cu Pad :645mm²)
DC
1000
800
600
400
200
0
0
20
40
60
80
100
120
140
160

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