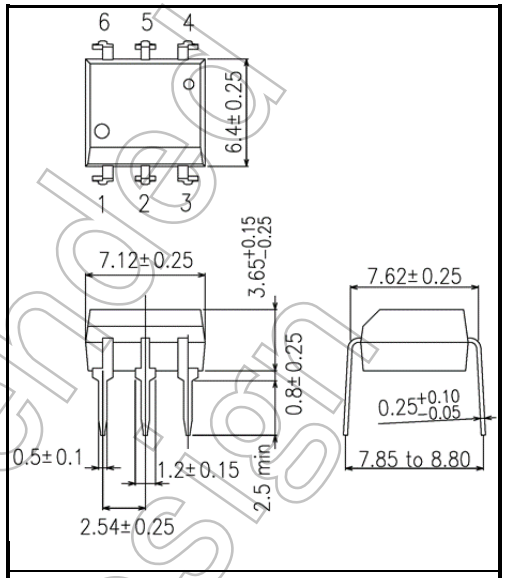
TOSHIBA Photocoupler IRED LED + Photo IC

TLP513

Line Receiver
Microprocessor System Interface
Data transfers between circuits of different potentials
Computer Terminal Interface
Ground Loop Elimination

Unit: mm



JEDEC	—
JEITA	—
TOSHIBA	11−7A8S

Weight: 0.4 g (typ.)

TLP513 is a 6-PIN DIP photocoupler, which consists of an infrared emitting diode and a high-gain, high-speed IC detector chip.

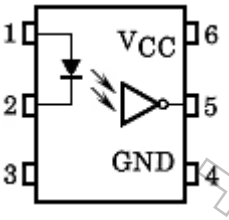
It has a Schottky clamped transistor and has an open collector output type.

- Threshold input current : I_F = 5 mA (max)
- Switching Speed : 10 MBd
- Guaranteed performance over temperature: 0 to 70°C
- Isolation voltage : 2500 V_{rms} (min)
- UL-recognized : UL 1577, File No.E67349

Truth Table (positive Logic)

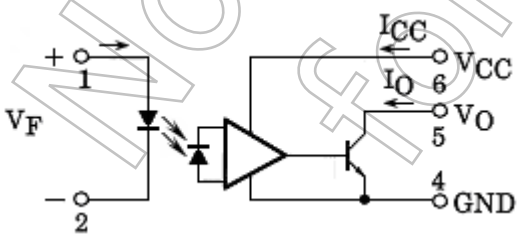
Input	Output
H	L
L	H

Pin Configuration (top View)



1: Anode
2: Cathode
3: N.C.
4: GND
5: V_O(open-collector)
6: V_{CC}

Schematic



Note: A 0.1 μF bypass capacitor must be connected between pins 6 and 4.

Start of commercial production
1987-09

Absolute Maximum Rating (Ta = 25°C)

Characteristics			Symbol	Rating	Unit
LED	Forward current		I_F	20	mA
	Forward current derating (Ta ≥ 85°C)		ΔIF/ΔTa	-1.6	mA/°C
	Pulse forward current	(Note 1)	I_{FP}	40	mA
	Peak transient forward current	(Note 2)	I_{FPT}	1	A
	Reverse voltage		V_R	5	V
	Input power dissipation		P_D	100	mW
	Input power dissipation derating(Ta ≥ 85°C)		ΔP_D/°C	-2.5	mW/°C
Detector	Output current		I_O	25	mA
	Output voltage		V_O	7	V
	Supply voltage	(Note 3)	V_{CC}	7	V
	Output power dissipation		P_O	40	mW
	Output power dissipation derating (Ta≥ 85°C)		ΔPo/ ΔTa	-1.0	mW/°C
Storage temperature range			T_{stg}	−55 to 125	°C
Operating temperature range			T_{opr}	−40 to 85	°C
Lead solder temperature	(10 s)	(Note 4)	T_{sol}	260	°C
Isolation voltage		(Note 5)	BV_S	2500	V_{rms}

Note: Using continuously under heavy loads (e.g. application of high temperature/current/voltage and a significant change in temperature, etc.) may cause this product to decrease in reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: 50 % duty cycle, 1 ms pulse width.

Note 2: Pulse width ≤1 μs, 300 pps.

Note 3: 1 minute maximum.

Note 4: Soldering is performed 2mm from the bottom of the package.

Note 5: AC, 60 s, R.H. ≤ 60 %
Device considered a two-terminal device: 1, 2 and 3 shorted together and pins 4, 5 and 6 shorted together.

Recommended Operating Conditions

Characteristics		Symbol	Min	Typ.	Max	Unit
‘L’ level input voltage		V_{FL}	−3	0	1.0	V
‘H’ level input current		I_{FH}	6.3*	8	20	mA
Supply voltage**		V_{CC}	4.5	5	5.5	V
Fan-out	(TTL load)	N	—	—	8	—
Operating temperature		T_{opr}	0	—	70	°C

Note: The recommended operating conditions are given as a design guideline to obtain the expected performance of the device. In addition, each item is an independent guideline. In developing designs using this product, please confirm the specified characteristics shown in this document.

* 6.3 mA is a guard banded value which allows for at least 20 % CTR degradation.
Initial input current threshold is 5 mA or less.

** This item denotes the operating range and not the recommended operating conditions.

Electrical Characteristics

(Unless otherwise specified Ta = 0 to 70°C, V_{CC} = 4.5 to 5.5 V, V_{FL}≤1.0 V)

Characteristics	Symbol	Test Conditions	Min	Typ.*	Max	Unit
Forward voltage	V_F	I_F = 10 mA, Ta = 25 °C	—	1.65	1.8	V
Temperature coefficient of forward voltage	$\Delta V_F / \Delta Ta$	I_F = 10 mA	—	−2.0	—	mV /°C
Input reverse current	I_R	V_R = 5 V, Ta = 25 °C	—	—	10	μA
Input capacitance	C_T	V_F = 0 V, f = 1 MHz, Ta = 25 °C	—	45	—	pF
"H" level output current	I_{OH}	V_F = 1.0 V, V_O = 5.5 V	—	—	250	μA
		V_F = 1.0 V, V_O = 5.5 V, Ta = 25 °C	—	0.5	10	
"L" level output voltage	V_{OL}	I_F = 5 mA, I_{OL} = 13 mA (sinking)	—	0.4	0.6	V
"H→L" threshold input current	I_{FH}	I_{OL} = 13 mA (sinking), V_{OL} = 0.6 V	—	—	5	mA
"H" level supply current	I_{CCH}	V_{CC} = 5.5 V, I_F = 0 mA	—	7	15	mA
"L" level supply current	I_{CCL}	V_{CC} = 5.5 V, I_F = 10 mA	—	12	18	mA
Isolation resistance	R_S	V_S = 500 V, R.H. ≤ 60 %, Ta = 25 °C (Note 7)	5×10^{10}	10^{14}	—	Ω
Input to output capacitance	C_S	V_S = 0 V, f = 1 MHz, Ta = 25 °C (Note 7)	—	0.6	—	pF

* : All typical values are at Ta = 25°C.

Switching Characteristics (Ta = 25°C, V_{CC} = 5 V)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Propagation delay time (H→L)	t_{pHL}	1	I_F = 0→7.5 mA, R_L = 350 Ω, C_L = 15 pF	—	60	120	ns
Propagation delay time (L→H)	t_{pLH}		I_F = 7.5 →0 mA, R_L = 350 Ω, C_L = 15 pF	—	60	120	ns
Rise time, fall time (10 to 90%)	t_r, t_f		I_F = 0⇄7.5 mA, R_L = 350 Ω, C_L = 15 pF	—	30	—	ns
Common mode transient immunity at high level output	CM_H	2	I_F = 0 mA, R_L = 350 Ω, V_{CM} = 200 V, V_O (min) = 2 V (Note 8)	—	200	—	V / μs
Common mode transient immunity at low level output	CM_L		I_F = 7.5 mA, R_L = 350 Ω, V_{CM} = 200 V, V_O (max) = 0.8 V (Note 9)	—	−500	—	V / μs

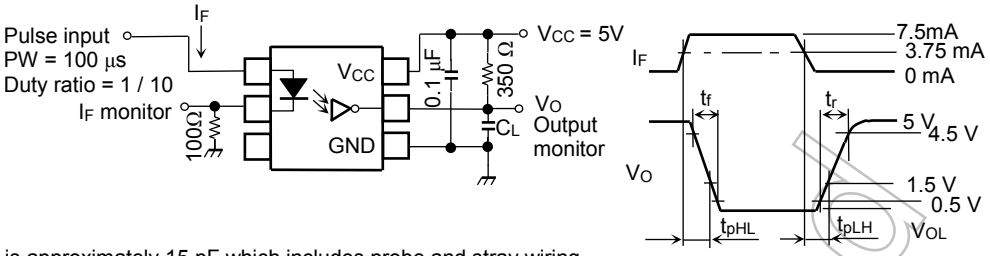
Note 6: The V_{CC} supply voltage to each TLP513 isolator must be bypassed by a 0.1 μF capacitor. This can be either a ceramic or solid tantalum capacitor with good high frequency characteristic and should be connected as close as possible to the V_{CC} and GND pins of each device.

Note 7: Device considered a 2-terminal device: Pins 1, 2 and 3 shorted together, and pins 4, 5 and 6 shorted together.

Note 8: CM_H: The maximum tolerable rate of rise of the common mode voltage to ensure the output will remain in the high output state (i.e., V_O > 2.0 V). Measured in volts per microsecond (V / μs).

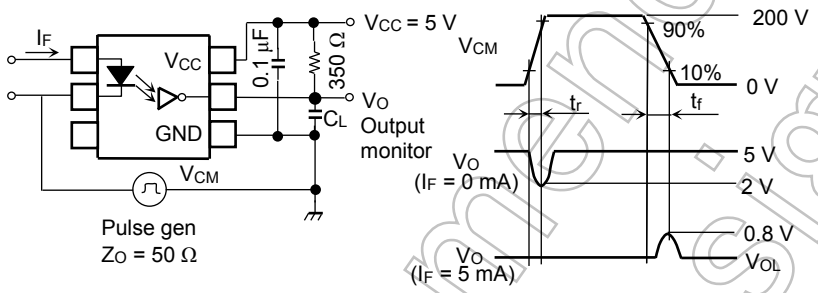
Note 9: CM_L: The maximum tolerable rate of fall of the common mode voltage to ensure the output will remain in the low output state (i.e., V_O < 0.8 V). Measured in volts per microsecond (V / μs).

Test Circuit 1: Switching Time Test Circuit



C_L is approximately 15 pF which includes probe and stray wiring

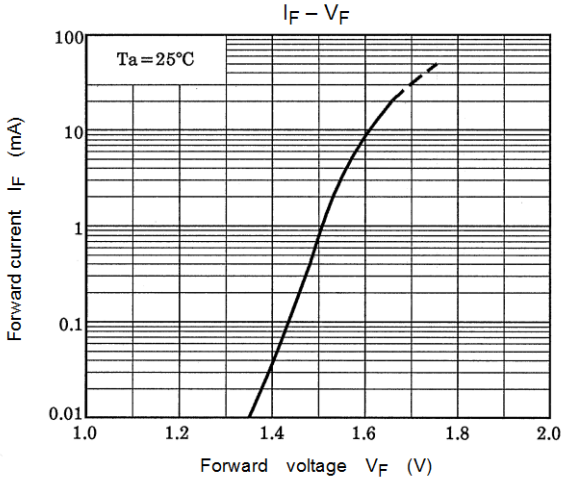
Test Circuit 2: Common Mode Noise Immunity Test Circuit



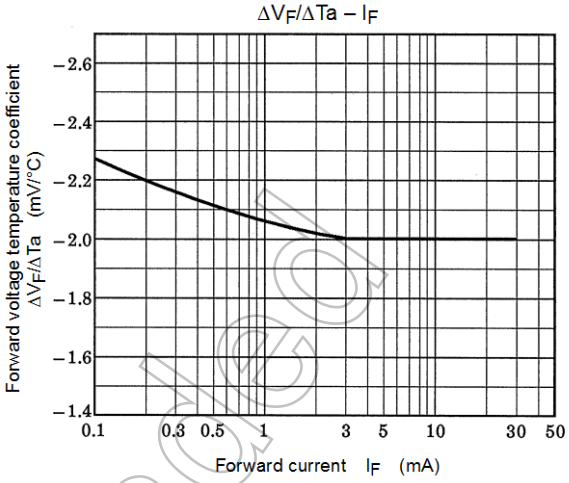
$$CM_H = \frac{160\ (V)}{t_r\ (\mu s)},\quad CM_L = \frac{160\ (V)}{t_f\ (\mu s)}$$

C_L is approximately 15 pF which includes probe and stray wiring

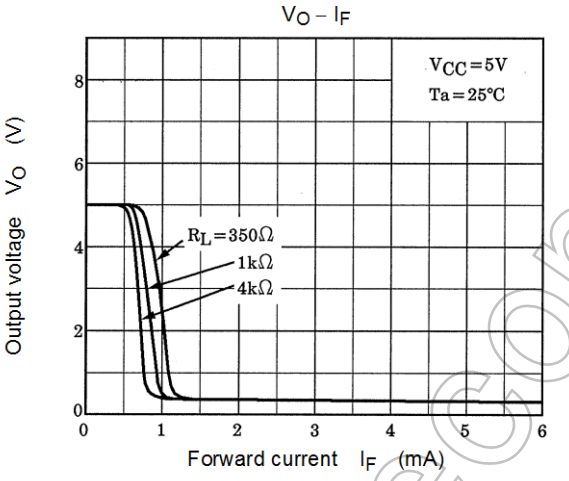
$I_F - V_F$



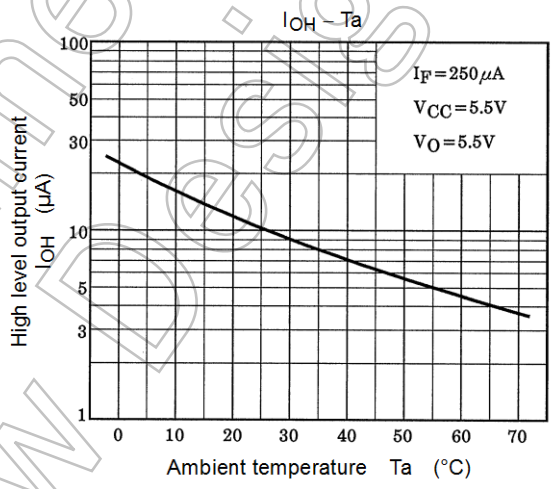
$\Delta V_F/\Delta Ta - I_F$



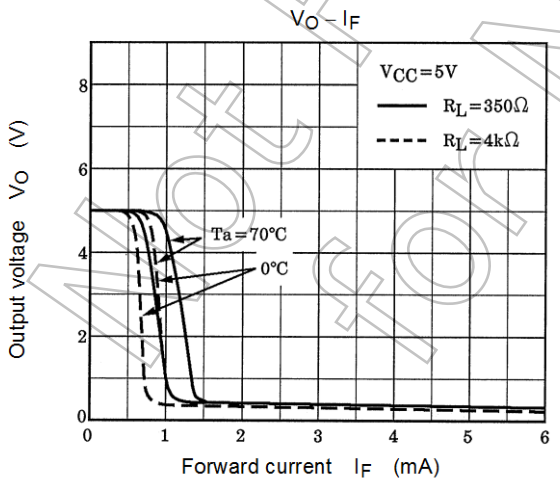
$V_O - I_F$



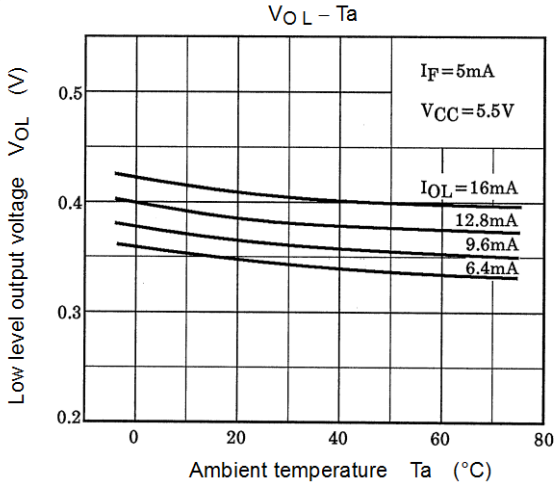
$I_{OH} - Ta$



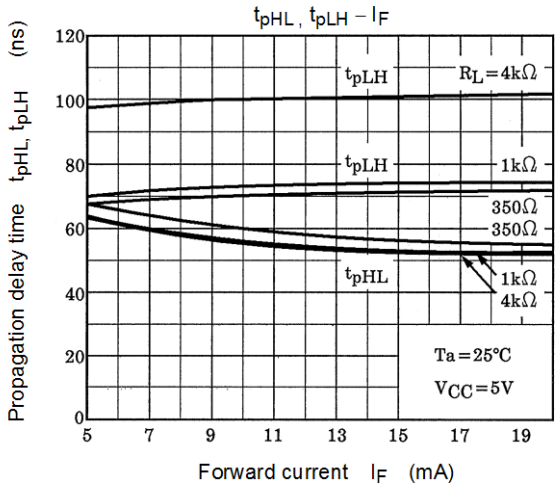
$V_O - I_F$

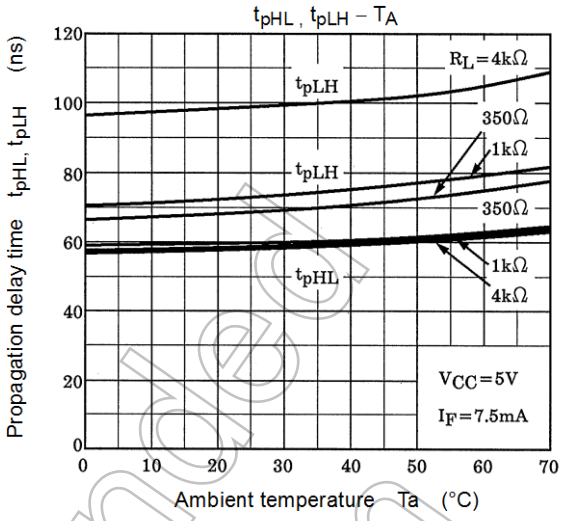


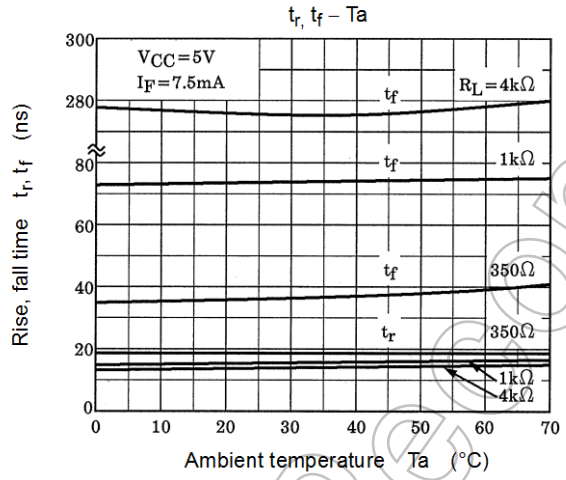
$V_{OL} - Ta$



NOTE: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.







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