

TLP718

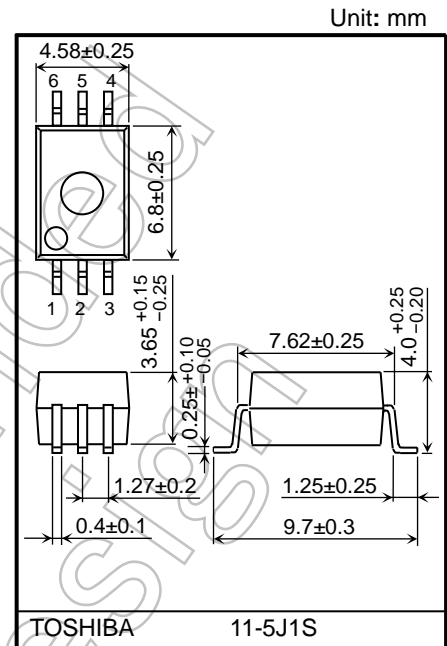
Isolated Bus Drivers
 High Speed Line Receivers
 Microprocessor System Interfaces

The Toshiba TLP718 consists of an infrared emitting diode and an integrated high-gain, high-speed photodetector. This unit is a 6-pin SDIP. The TLP718 is 50% smaller than the 8-PIN DIP and meets the reinforced insulation class requirements of international safety standards. Therefore the mounting area can be reduced in equipment requiring safety standard certification.

The detector has a totem pole output stage to provide both source and sink driving. The detector IC has an internal shield that provides a guaranteed common-mode transient immunity of 10 kV/μs.

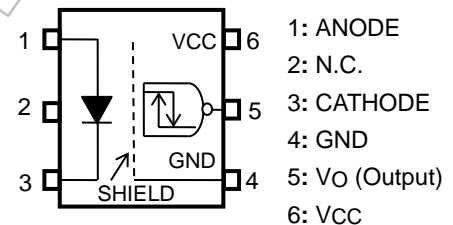
The TLP718 is inverter logic type. For buffer logic type, the TLP715 is in line-up.

- Inverter logic type (totem pole output)
- Guaranteed performance over temperature : -40 to 100°C
- Power supply voltage : 4.5 to 20 V
- Input current: IFHL = 3 mA (max)
- Switching time (t_{pHL} / t_{pLH}) : 250 ns (max)
- Common-mode transient immunity : ±10 kV/μs (min)
- Isolation voltage : 5000 Vrms (min)
- UL-recognized: UL 1577, File No.E67349
- cUL-recognized: CSA Component Acceptance Service No.5A
File No.E67349
- VDE-approved: EN 60747-5-5 , EN 62368-1 (Note1)



Weight: 0.26 g (typ.)

Pin Configuration (Top View)



Note 1 : When a VDE approved type is needed,
 please designate the **Option(D4)**.

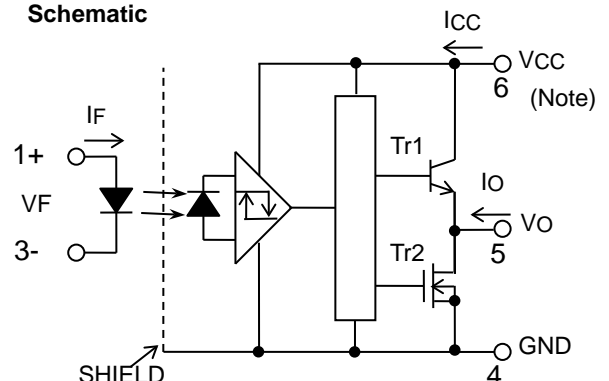
Construction Mechanical Rating

	7.62 mm pitch standard type	10.16 mm pitch TLPXXXF type
Creepage Distance	7.0 mm (min)	8.0 mm (min)
Clearance	7.0 mm (min)	8.0 mm (min)
Insulation Thickness	0.4 mm (min)	0.4 mm (min)

Truth Table

Input	LED	Tr1	Tr2	Output
H	ON	OFF	ON	L
L	OFF	ON	OFF	H

Schematic



Note: 0.1 μF bypass capacitor must be connected between pins 6 and 4.

Start of commercial production
 2008-12

Absolute Maximum Ratings (Ta = 25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
LED	Forward Current (Ta ≤ 83°C)	IF	20	mA
	Forward Current Derating (Ta ≥ 83°C)	ΔIF/ΔTa	-0.48	mA/°C
	Peak Transient Forward Current (Note 1)	IFPT	1	A
	Reverse Voltage	VR	5	V
	Input power dissipation	P _b	40	mW
	Input power dissipation derating (Ta ≥ 83°C)	ΔP _b /ΔTa	-0.96	mW/°C
	Junction Temperature	T _j	125	°C
DETECTOR	Output Current 1 (Ta ≤ 25°C)	IO1	25 / -15	mA
	Output Current 2 (Ta ≤ 100°C)	IO2	13 / -13	mA
	Output Voltage	VO	-0.5 to 20	V
	Supply Voltage	VCC	-0.5 to 20	V
	Output power dissipation	P _o	75	mW
	Output power dissipation derating (Ta ≥ 25°C)	ΔP _o /ΔTa	-0.75	mW / °C
	Junction Temperature	T _j	125	°C
Operating Temperature Range		T _{opr}	-40 to 100	°C
Storage Temperature Range		T _{stg}	-55 to 125	°C
Lead Solder Temperature (10 s)		T _{sol}	260	°C
Isolation Voltage (AC, 60 s, R.H. ≤ 60 %) (Note 2)		BVs	5000	V _{rms}

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Pulse width PW ≤ 1 μs, 300 pps.

Note 2: Device Considered a two terminal device: pins 1, 2 and 3 shorted together and pins 4, 5 and 6 shorted together.

Recommended Operating Conditions

CHARACTERISTIC	SYMBOL	MIN	TYP.	MAX	UNIT
Input Current, ON	IF (ON)	4.5	-	10	mA
Input Voltage, OFF	VF (OFF)	0	-	0.8	V
Supply Voltage (Note 1)	VCC	4.5	-	20	V
Operating Temperature	T _{opr}	-40	-	100	°C

Note: Recommended operating conditions are given as a design guideline to obtain expected performance of the device. Additionally, each item is an independent guideline respectively. In developing designs using this product, please confirm specified characteristics shown in this document.

Note 1: This item denotes operating ranges, not meaning of recommended operating conditions.

Electrical Characteristics

(Unless otherwise specified, Ta = -40 to 100°C, VCC = 4.5 to 20 V)

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	CONDITION	MIN	TYP.	MAX	UNIT
Input forward voltage	V _F	—	I _F = 5 mA, Ta = 25 °C	1.4	1.6	1.7	V
Temperature coefficient of forward voltage	ΔV _F /ΔTa	—	I _F = 5 mA	—	-2.0	—	mV/°C
Input reverse current	I _R	—	V _R = 5 V, Ta = 25 °C	—	—	10	μA
Input capacitance	C _T	—	V = 0 V, f = 1 MHz, Ta = 25 °C	—	45	—	pF
Logic LOW output voltage	V _{OL}	Figure 1	I _{OL} = 3.5 mA, I _F = 5 mA	—	0.2	0.6	V
Logic HIGH output voltage (Note 1)	V _{OH}	Figure 2	I _{OH} = -2.6 mA, V _F = 0.8 V	V _{CC} = 4.5 V 2.7	3.5	—	V
				V _{CC} = 20 V 17.4	19	—	
Logic LOW supply current	I _{CCL}	Figure 3	I _F = 5 mA	—	—	3.0	mA
Logic HIGH supply current	I _{CCH}	Figure 4	V _F = 0 V	—	—	3.0	mA
Logic LOW short circuit output current (Note 2)	I _{OSL}	Figure 5	I _F = 5 mA	V _{CC} = V _O = 5.5 V 15	80	—	mA
				V _{CC} = V _O = 20 V 20	90	—	
Logic HIGH short circuit output current (Note 3)	I _{OSH}	Figure 6	V _F = 0 V, V _O = GND	V _{CC} = 5.5 V -5	-15	—	mA
				V _{CC} = 20 V -10	-20	—	
Input current logic LOW output	I _{FHL}	—	I _O = 3.5 mA, V _O < 0.6 V	—	0.4	3	mA
Input voltage logic HIGH output	V _{FLH}	—	I _O = -2.6 mA, V _O > 2.4 V	0.8	—	—	V
Input current hysteresis	I _{HYS}	—	V _{CC} = 5 V	—	0.05	—	mA

Note: All typical values are at Ta = 25 °C, VCC = 5 V unless otherwise specified.

Note 1: V_{OH} = V_{CC} - V_O [V]

Note 2: Duration of output short circuit time should not exceed 10 ms.

Note 3: A ceramic capacitor (0.1 μF) should be connected from pin 6 to pin 4 to stabilize the operation of the high gain linear amplifier. Failure to provide the bypassing may impair the switching property. The total lead length between capacitor and coupler should not exceed 1 cm.

Isolation Characteristics (Ta = 25°C)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN	TYP.	MAX	UNIT
Capacitance input to output	C _S (Note 1)	V _S = 0 V, f = 1 MHz	—	1.0	—	pF
Isolation resistance	R _S (Note 1)	R.H. ≤ 60 %, V _S = 500 V	1×10 ¹²	10 ¹⁴	—	Ω
Isolation voltage	B _V S (Note 1)	AC, 60 s	5000	—	—	V _{rms}

Note : This device is considered as a two-terminal device: Pins 1, 2 and 3 are shorted together, and pins 4, 5 and 6 are shorted together.

Switching Characteristics

(Unless otherwise specified, $T_a = -40$ to 100°C , $V_{CC} = 4.5$ to 20 V)

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	CONDITION	MIN	TYP.	MAX	UNIT
Propagation delay time to logic HIGH output	t_{pLH}	Figure 7, Figure 8	$I_F = 3 \rightarrow 0$ mA	30	120	250	ns
Propagation delay time to logic LOW output	t_{pHL}		$I_F = 0 \rightarrow 3$ mA	30	120	250	ns
Switching time dispersion between ON and OFF	$ t_{pHL} - t_{pLH} $		—	—	—	220	ns
Rise Time (10 – 90 %)	t_r		$I_F = 3 \rightarrow 0$ mA, $V_{CC} = 5$ V	—	30	—	ns
Fall Time (90 – 10 %)	t_f		$I_F = 0 \rightarrow 3$ mA, $V_{CC} = 5$ V	—	30	—	ns
Common-mode transient Immunity at HIGH level output	CM_H	Figure 9	$V_{CM} = 1000$ V _{p-p} , $I_F = 0$ mA, $V_{CC} = 20$ V, $T_a = 25^\circ\text{C}$	10000	—	—	V/ μs
Common-mode transient Immunity at LOW level output	CM_L		$V_{CM} = 1000$ V _{p-p} , $I_F = 5$ mA, $V_{CC} = 20$ V, $T_a = 25^\circ\text{C}$	-10000	—	—	V/ μs

Note: All typical values are at $T_a = 25^\circ\text{C}$.

Figure 1: V_{OL} TEST CIRCUIT

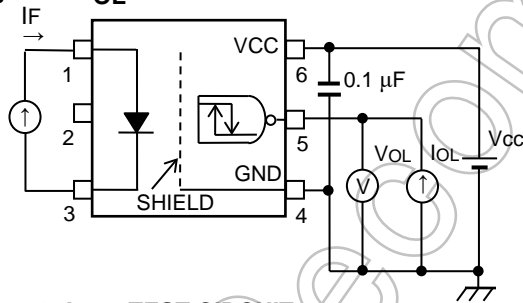


Figure 2: V_{OH} TEST CIRCUIT

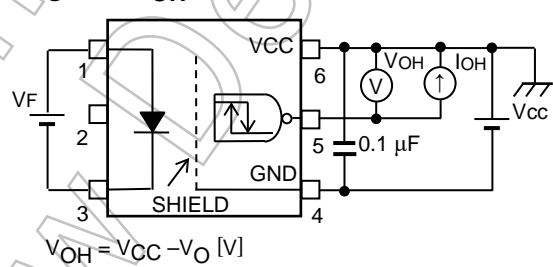


Figure 3: I_{CCL} TEST CIRCUIT

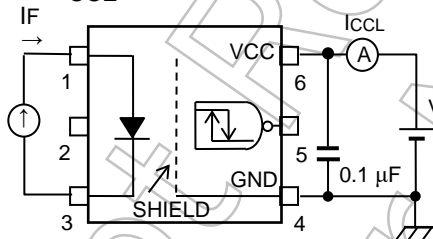


Figure 4: I_{CCH} TEST CIRCUIT

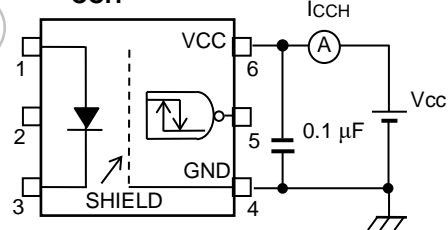


Figure 5: I_{OSL} TEST CIRCUIT

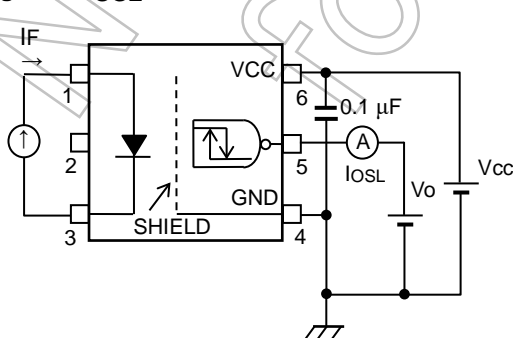


Figure 6: I_{OSH} TEST CIRCUIT

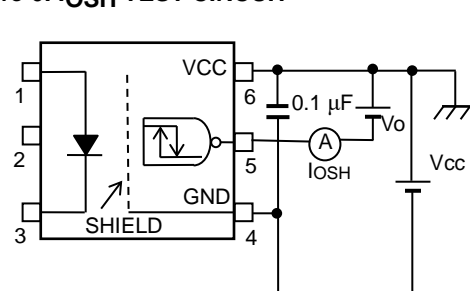
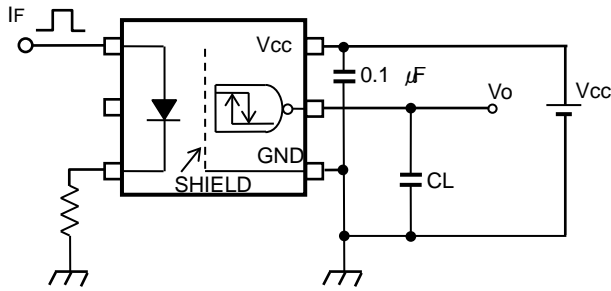


Figure 7: Switching Time Test Circuit

$I_F = 3 \text{ mA (P.G)}$
 ($f = 50 \text{ kHz}$, duty = 50%
 less than $t_r = t_f = 5 \text{ ns}$)



CL: stray capacitance of probe and wiring (to 15 pF)

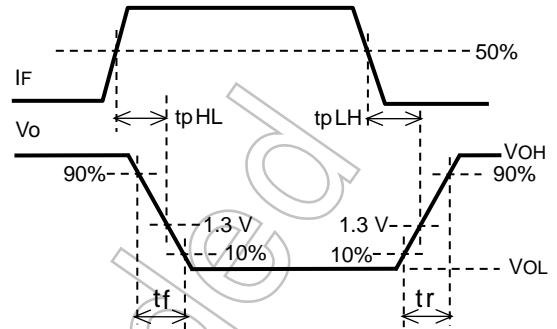
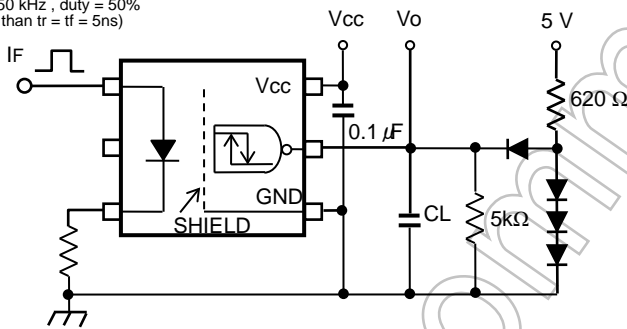


Figure 8: Switching Time Test Circuit

$I_F = 3 \text{ mA (P.G)}$
 ($f = 50 \text{ kHz}$, duty = 50%
 less than $t_r = t_f = 5 \text{ ns}$)



CL: stray capacitance of probe and wiring (to 15 pF)

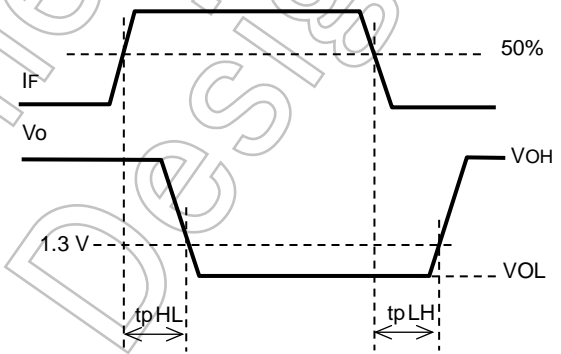
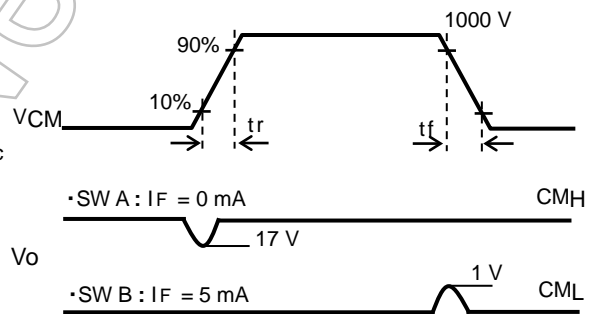
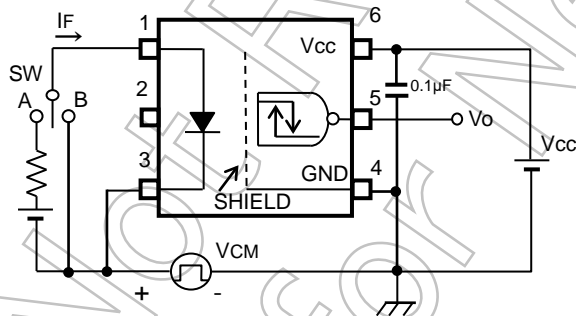


Figure 9: Common-Mode Transient Immunity Test Circuit



$$CM_H = \frac{800(V)}{t_r (\mu s)} \quad CM_L = -\frac{800(V)}{t_f (\mu s)}$$

CM_H (CM_L) is the maximum rate of rise (fall) of the common mode voltage that can be sustained with the output voltage in the high (low) state.

EN 60747-5-5 Option:(D4)

Types : TLP718, TLP718F

Type designations for "option: (D4)", which are tested under EN 60747 requirements.

Ex.: TLP718 (D4-TP,F) D4 : EN 60747 option
 TP : Standard tape & reel type
 F : [[G]]/RoHS COMPATIBLE (Note 1)

Note: Use TOSHIBA standard type number for safety standard application.

Ex.: TLP718 (D4-TP,F) → TLP718



Note 1 : Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product.

The RoHS is the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

EN 60747 Isolation Characteristics

Description	Symbol	Rating	Unit
Application classification for rated mains voltage ≤ 300 V _{rms} for rated mains voltage ≤ 600 V _{rms}		I-IV I-III	—
Climatic classification		40 / 100 / 21	—
Pollution degree		2	—
Maximum operating insulation voltage	TLPxxx type	V _{IORM}	Vpk
	TLPxxxF type		
Input to output test voltage, method A V _{pr} = 1.6×V _{IORM} , type and sample test t _p = 10 s, partial discharge < 5 pC	TLPxxx type	V _{pr}	Vpk
	TLPxxxF type		
Input to output test voltage, method B V _{pr} = 1.875×V _{IORM} , 100% production test t _p = 1 s, partial discharge < 5 pC	TLPxxx type	V _{pr}	Vpk
	TLPxxxF type		
Highest permissible overvoltage (transient overvoltage, t _{pr} = 60 s)	V _{TR}	8000	Vpk
Safety limiting values (max permissible ratings in case of fault, also refer to thermal derating curve) current (input current I _F , P _{si} = 0) power (output or total power dissipation) temperature	I _{si} P _{si} T _{si}	300 700 150	mA mW °C
Insulation resistance, V _{IO} = 500 V, T _a = 25°C V _{IO} = 500 V, T _a = 100°C V _{IO} = 500 V, T _a = T _{si}	R _{si}	≥10 ¹² ≥10 ¹¹ ≥10 ⁹	Ω

Insulation Related Specifications

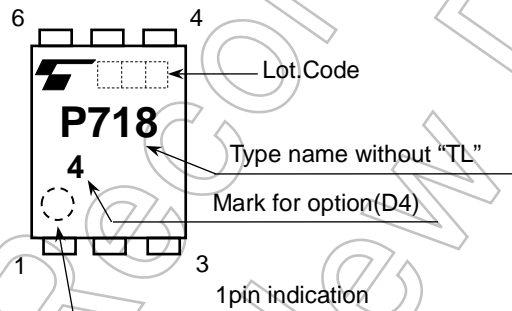
		 7.62 mm pitch TLPxxx type	 10.16 mm pitch TLPxxxF type
Minimum creepage distance	Cr	7.0 mm	8.0 mm
Minimum clearance	Cl	7.0 mm	8.0 mm
Minimum insulation thickness	ti	0.4 mm	
Comperative tracking index	CTI	175	

Note: If a printed circuit is incorporated, the creepage distance and clearance may be reduced below this value. If this is not permissible, the user shall take suitable measures.

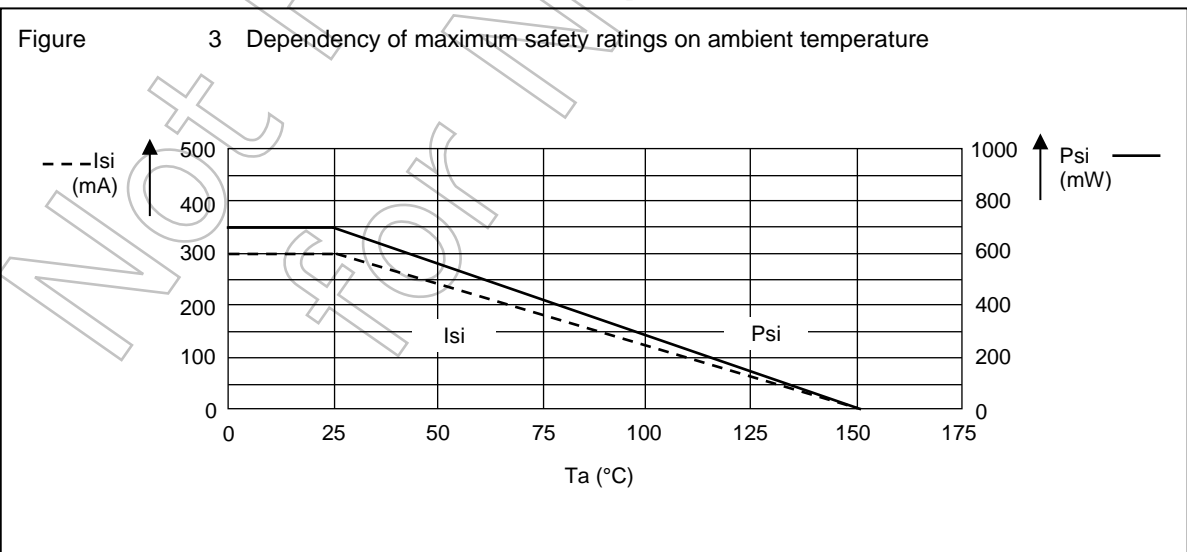
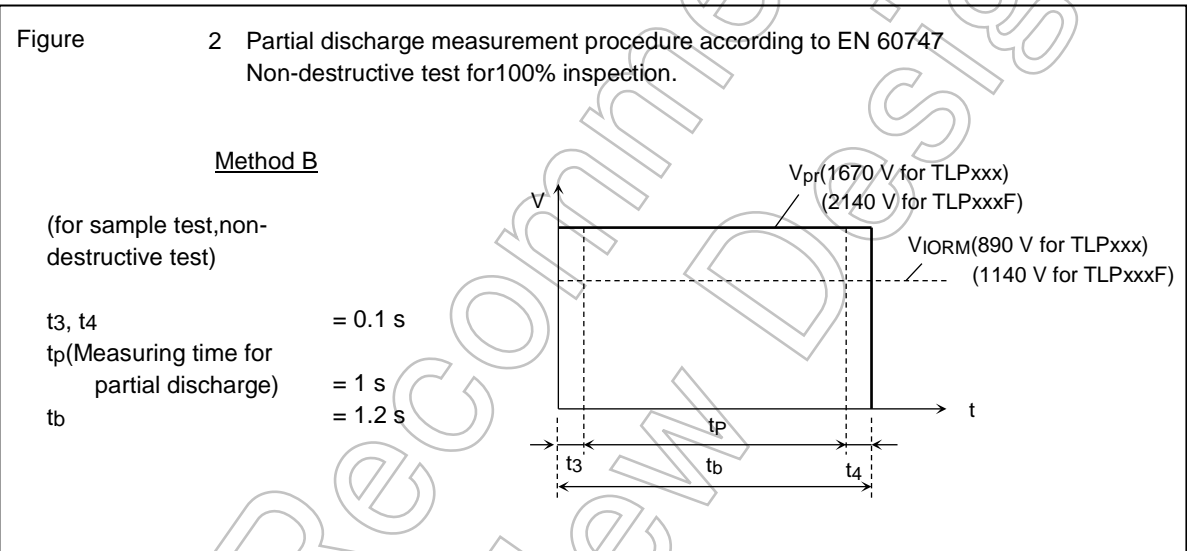
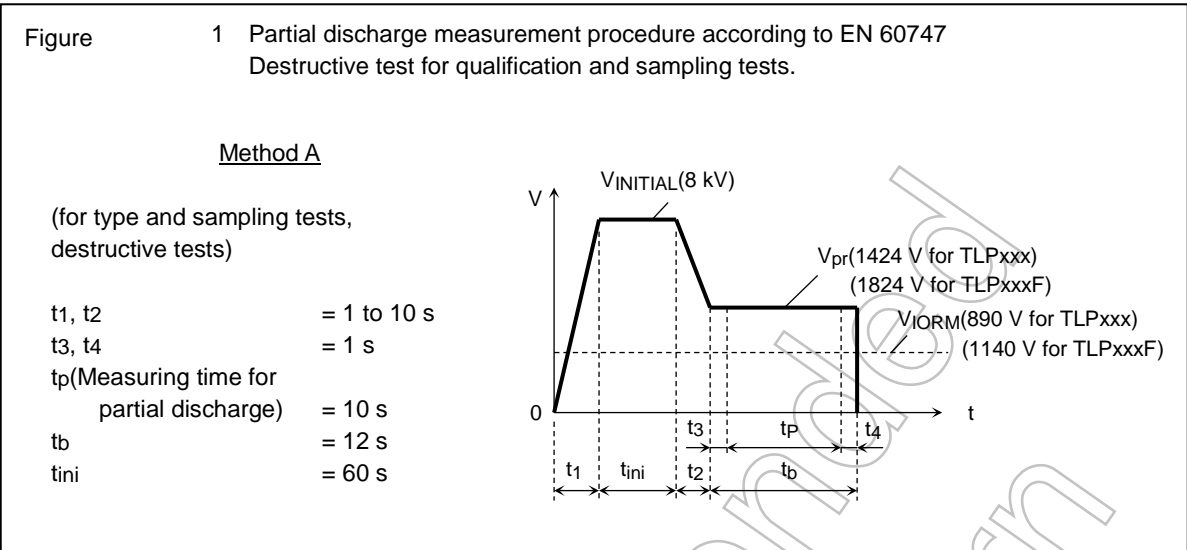
Note: This photocoupler is suitable for 'safe electrical isolation' only within the safety limit data. Maintenance of the safety data shall be ensured by means of protective circuits.

Marking on product for EN 60747 : **4**

Marking Example:



Note: The above marking is applied to the photocouplers that have been qualified according to option (D4) of EN 60747.



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