

TOSHIBA Field Effect Transistor Silicon P Channel MOS Type

SSM3J15FS

High Speed Switching Applications

Analog Switch Applications

- Small package
- Low ON resistance : $R_{on} = 12 \Omega$ (max) (@ $V_{GS} = -4 V$)
: $R_{on} = 32 \Omega$ (max) (@ $V_{GS} = -2.5 V$)

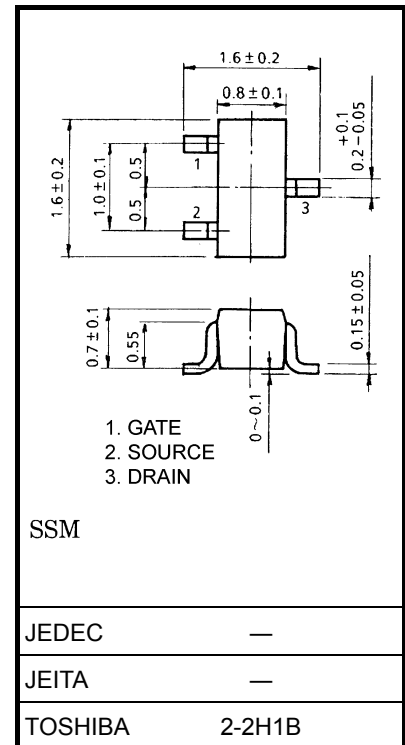
Absolute Maximum Ratings ($T_a = 25^\circ C$)

| Characteristics | | Symbol | Rating | Unit |
|--|-------|-----------|------------|------------|
| Drain-Source voltage | | V_{DS} | -30 | V |
| Gate-Source voltage | | V_{GSS} | ± 20 | V |
| Drain current | DC | I_D | -100 | mA |
| | Pulse | I_{DP} | -200 | |
| Drain power dissipation ($T_a = 25^\circ C$) | | P_D | 100 | mW |
| Channel temperature | | T_{ch} | 150 | $^\circ C$ |
| Storage temperature range | | T_{stg} | -55 to 150 | $^\circ C$ |

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

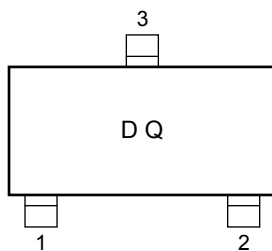
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Unit: mm

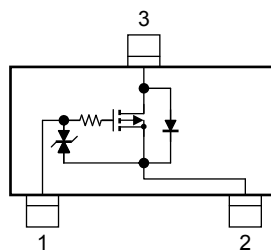


Weight: 0.0024 g(typ.)

Marking



Equivalent Circuit (top view)



Handling Precaution

When handling individual devices (which are not yet mounting on a circuit board), be sure that the environment is protected against electrostatic electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

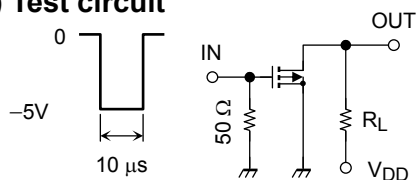
Start of commercial production
2002-03

Electrical Characteristics (Ta = 25°C)

| Characteristic | Symbol | Test Condition | MIN. | TYP. | MAX. | UNIT |
|--------------------------------|---------------|--|--|------|---------|---------------|
| Gate leakage current | I_{GSS} | $V_{GS} = \pm 16 \text{ V}, V_{DS} = 0$ | — | — | ± 1 | μA |
| Drain-Source breakdown voltage | $V_{(BR)DSS}$ | $I_D = -0.1 \text{ mA}, V_{GS} = 0$ | -30 | — | — | V |
| Drain cut-off current | I_{DSS} | $V_{DS} = -30 \text{ V}, V_{GS} = 0$ | — | — | -1 | μA |
| Gate threshold voltage | V_{th} | $V_{DS} = -3 \text{ V}, I_D = -0.1 \text{ mA}$ | -1.1 | — | -1.7 | V |
| Forward transfer admittance | $ Y_{fs} $ | $V_{DS} = -3 \text{ V}, I_D = -10 \text{ mA}$ | 20 | — | — | mS |
| Drain-Source ON resistance | $R_{DS(ON)}$ | $I_D = -10 \text{ mA}, V_{GS} = -4 \text{ V}$ | — | 8 | 12 | Ω |
| | | $I_D = -1 \text{ mA}, V_{GS} = -2.5 \text{ V}$ | — | 14 | 32 | |
| Input capacitance | C_{iss} | $V_{DS} = -3 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}$ | — | 9.1 | — | pF |
| Reverse transfer capacitance | C_{rss} | | — | 3.5 | — | pF |
| Output capacitance | C_{oss} | | — | 8.6 | — | pF |
| Switching time | Turn-on time | t_{on} | $V_{DD} = -5 \text{ V}, I_D = -10 \text{ mA},$ | | 65 | ns |
| | Turn-off time | t_{off} | $V_{GS} = 0 \text{ to } -5 \text{ V}$ | | 175 | |

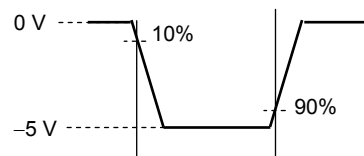
Switching Time Test Circuit

(a) Test circuit

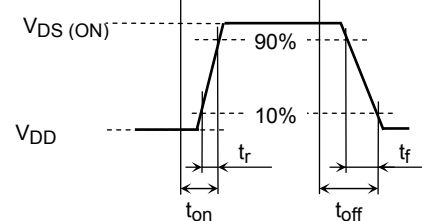


$V_{DD} = -5 \text{ V}$
 Duty $\leq 1\%$
 V_{IN} : $t_r, t_f < 5 \text{ ns}$
 ($Z_{out} = 50 \Omega$)
 Common Source
 $T_a = 25^\circ\text{C}$

(b) V_{IN}



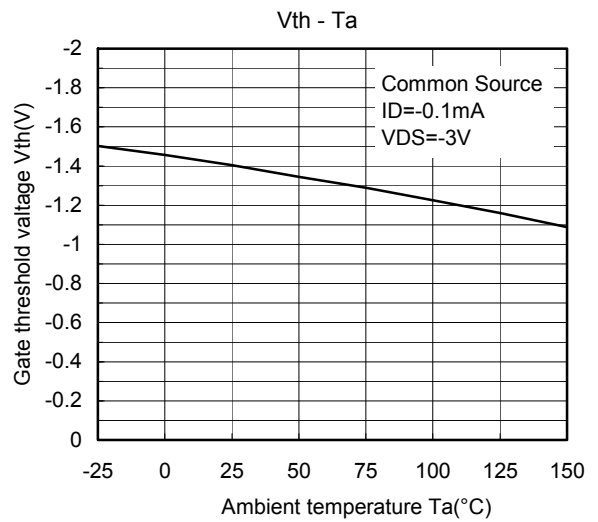
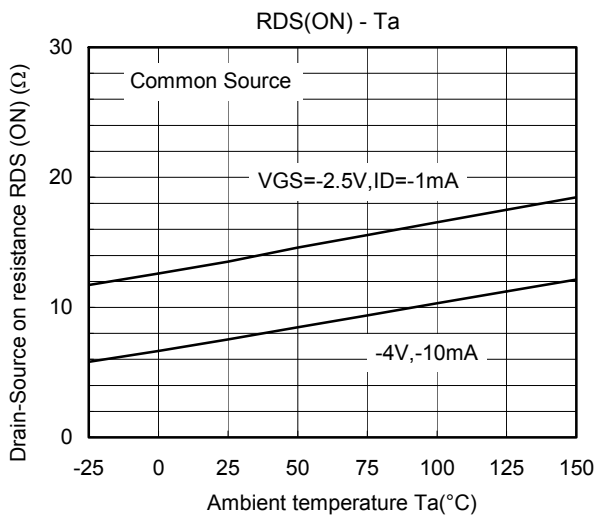
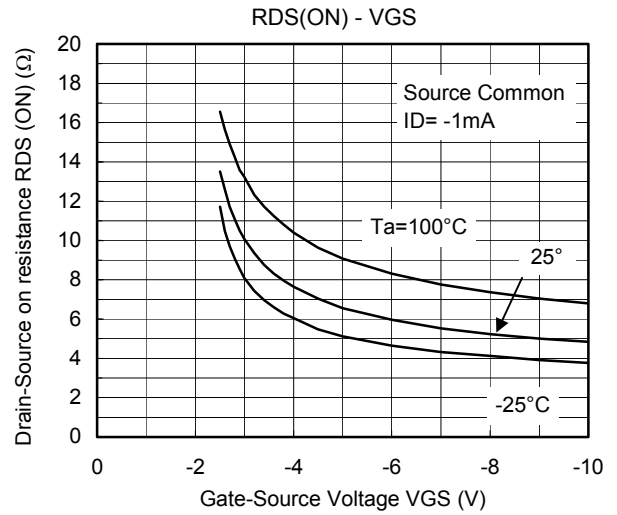
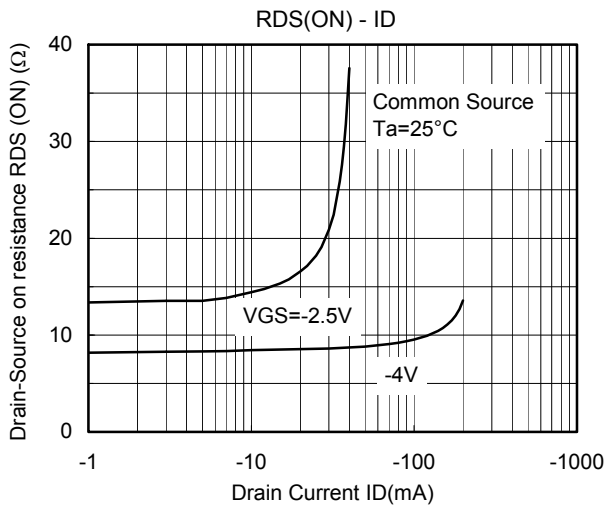
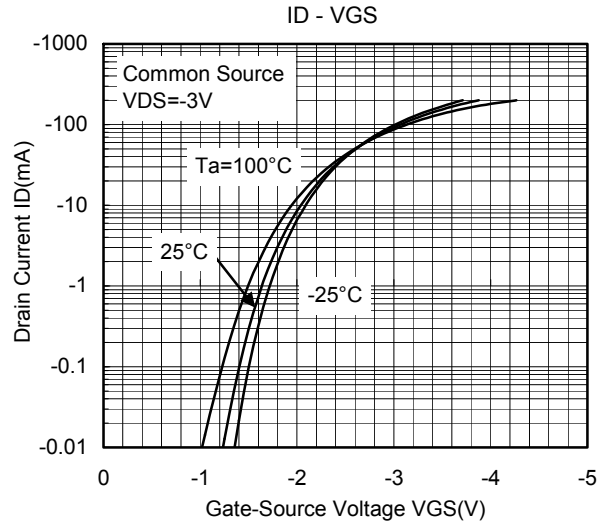
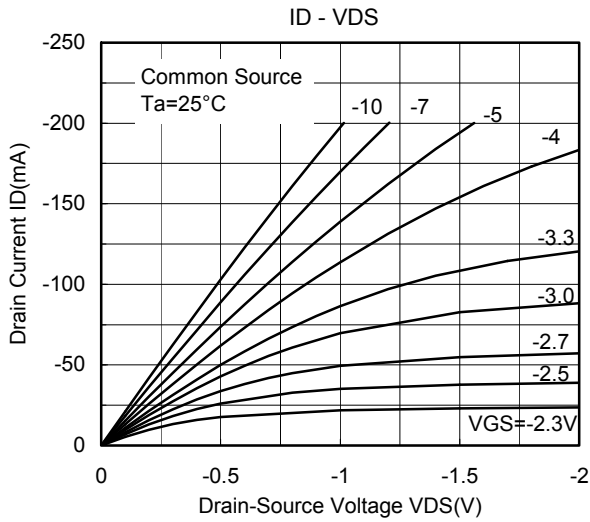
(c) V_{OUT}

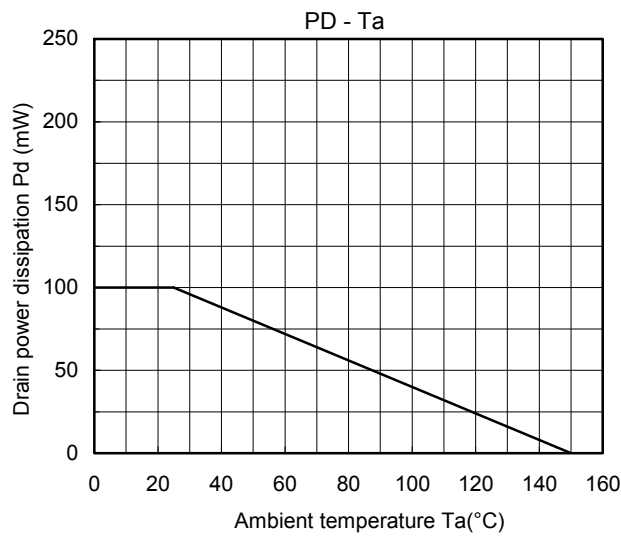
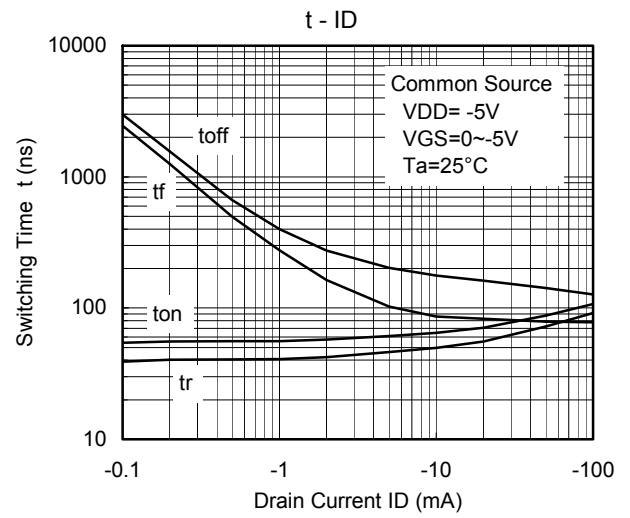
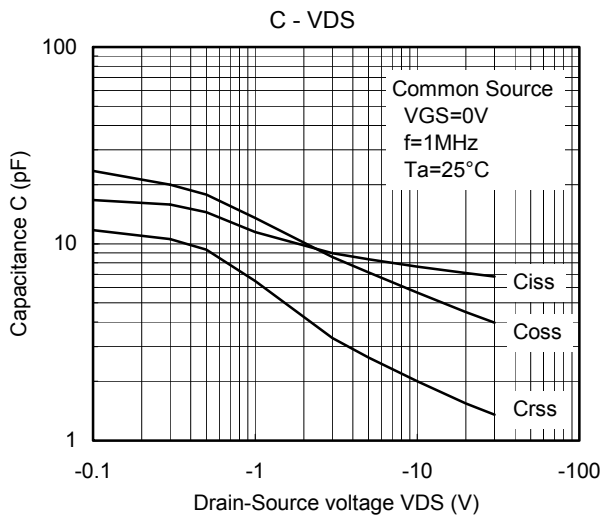
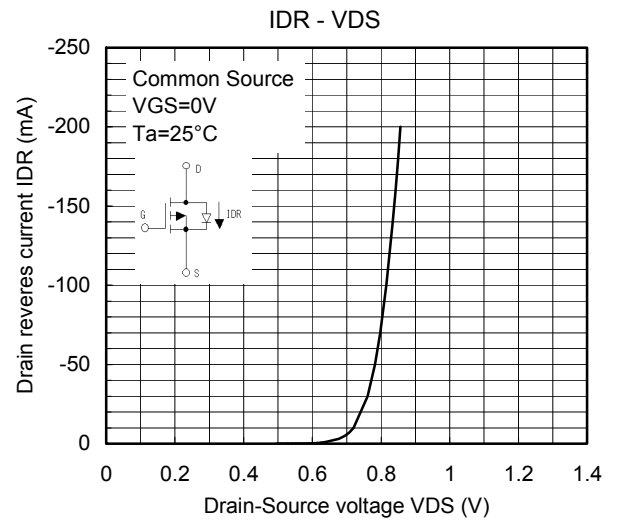
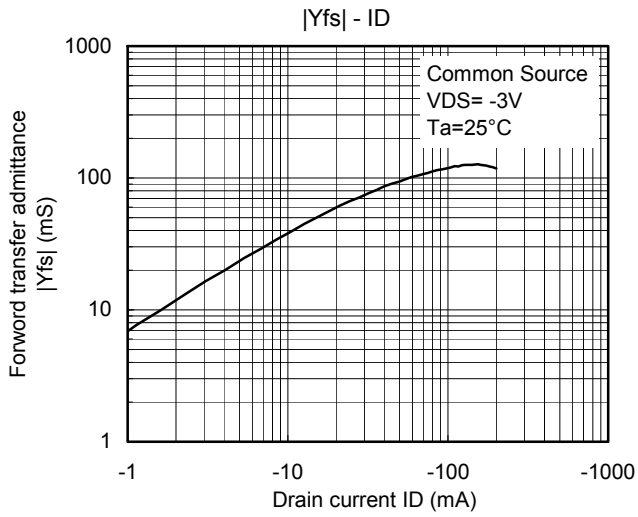


Precaution

V_{th} can be expressed as voltage between gate and source when low operating current value is $I_D = -100 \mu\text{A}$ for this product. For normal switching operation, $V_{GS(ON)}$ requires higher voltage than V_{th} and $V_{GS(OFF)}$ requires lower voltage than V_{th} . (Relationship can be established as follows: $V_{GS(OFF)} < V_{th} < V_{GS(ON)}$)

Please take this into consideration for using the device.





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