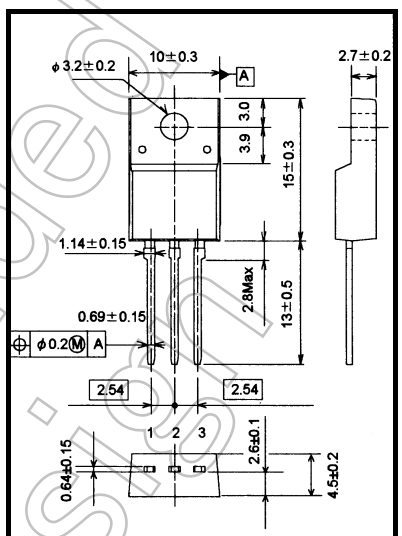
TOSHIBA Field Effect Transistor Silicon N Channel MOS Type (π-MOSⅦ)

TK8A65D

Switching Regulator Applications

- Low drain-source ON-resistance: $R_{DS\ (ON)}$ = 0.7 Ω (typ.)
- High forward transfer admittance: $|Y_{fs}|$ = 4.5 S (typ.)
- Low leakage current: I_{DSS} = 10 μA (max) (V_{DS} = 650 V)
- Enhancement mode: V_{th} = 2.0 to 4.0 V (V_{DS} = 10 V, I_D = 1 mA)

Unit: mm



JEDEC	—
JEITA	SC-67
TOSHIBA	2-10U1B

Weight: 1.7 g (typ.)

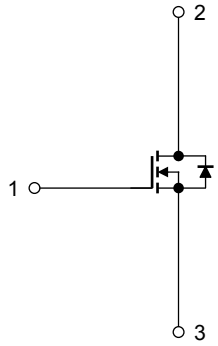
Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	650	V
Gate-source voltage		V_{GSS}	±30	V
Drain current	DC (Note 1)	I_D	8	A
	Pulse (Note 1)	I_{DP}	32	
Drain power dissipation (Tc = 25°C)		P_D	45	W
Single pulse avalanche energy (Note 2)		E_{AS}	416	mJ
Avalanche current		I_{AR}	8	A
Repetitive avalanche energy (Note 3)		E_{AR}	4.5	mJ
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/”Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Thermal Characteristics

Characteristics	Symbol	Max	Unit
Thermal resistance, channel to case	$R_{th\ (ch\text{-}c)}$	2.78	°C/W
Thermal resistance, channel to ambient	$R_{th\ (ch\text{-}a)}$	62.5	°C/W



Note 1: Ensure that the channel temperature does not exceed 150°C.

Note 2: V_{DD} = 90 V, T_{ch} = 25°C (initial), L = 11.5 mH, R_G = 25 Ω, I_{AR} = 8 A

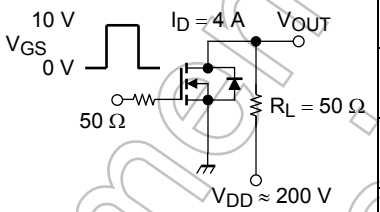
Note 3: Repetitive rating: pulse width limited by maximum channel temperature

This transistor is an electrostatic-sensitive device. Handle with care.

Start of commercial production
2009-01

Not Recommended for New Design

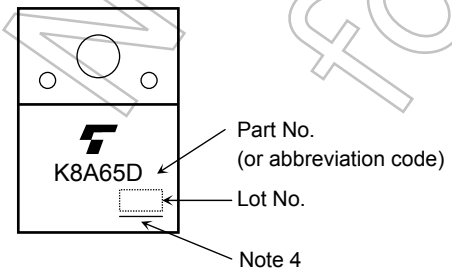
Electrical Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±30 V, V_{DS} = 0 V	—	—	±1	μA
Drain cut-off current		I_{DSS}	V_{DS} = 650 V, V_{GS} = 0 V	—	—	10	μA
Drain-source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 10 mA, V_{GS} = 0 V	650	—	—	V
Gate threshold voltage		V_{th}	V_{DS} = 10 V, I_D = 1 mA	2.0	—	4.0	V
Drain-source ON-resistance		$R_{DS\ (ON)}$	V_{GS} = 10 V, I_D = 4 A	—	0.7	0.84	Ω
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 10 V, I_D = 4 A	1.3	4.5	—	S
Input capacitance		C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	—	1350	—	pF
Reverse transfer capacitance		C_{rss}		—	6	—	
Output capacitance		C_{oss}		—	135	—	
Switching time	Rise time	t_r		—	22	—	ns
	Turn-on time	t_{on}		—	55	—	
	Fall time	t_f		—	15	—	
	Turn-off time	t_{off}	Duty ≤ 1%, t_w = 10 μs	—	100	—	
Total gate charge		Q_g	V_{DD} ≈ 400 V, V_{GS} = 10 V, I_D = 8 A	—	25	—	nC
Gate-source charge		Q_{gs}		—	16	—	
Gate-drain charge		Q_{gd}		—	9	—	

Source-Drain Ratings and Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Continuous drain reverse current (Note 1)	I_{DR}	—	—	—	8	A
Pulse drain reverse current (Note 1)	I_{DRP}	—	—	—	32	A
Forward voltage (diode)	V_{DSF}	I_{DR} = 8 A, V_{GS} = 0 V	—	—	−1.7	V
Reverse recovery time	t_{rr}	I_{DR} = 8 A, V_{GS} = 0 V,	—	1300	—	ns
Reverse recovery charge	Q_{rr}	dI_{DR}/dt = 100 A/μs	—	12	—	μC

Marking

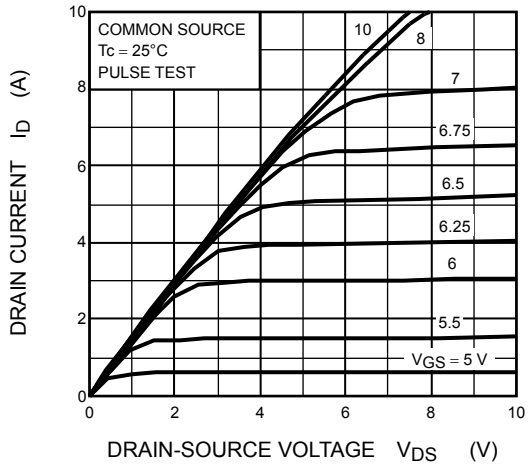


Note 4 : A line under a Lot No. identifies the indication of product Labels
[[G]]/RoHS COMPATIBLE or [[G]]/RoHS [[Pb]]

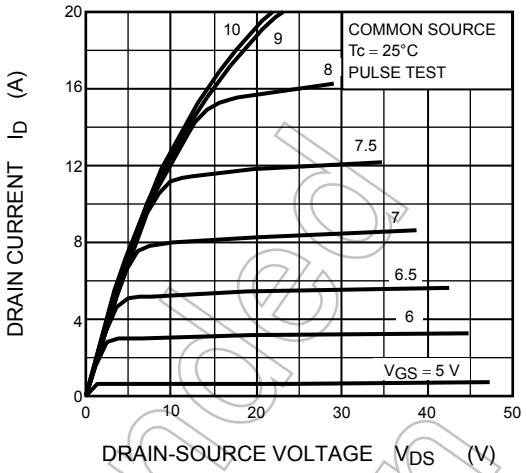
Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product. The RoHS is Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment

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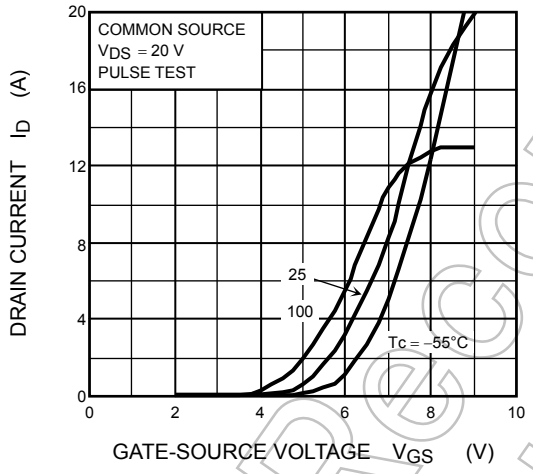
$I_D - V_{DS}$



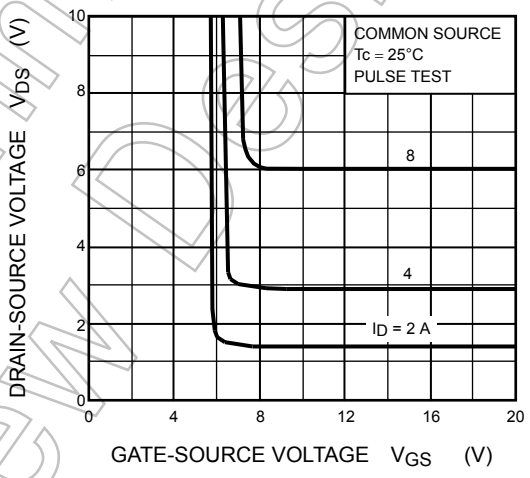
$I_D - V_{DS}$



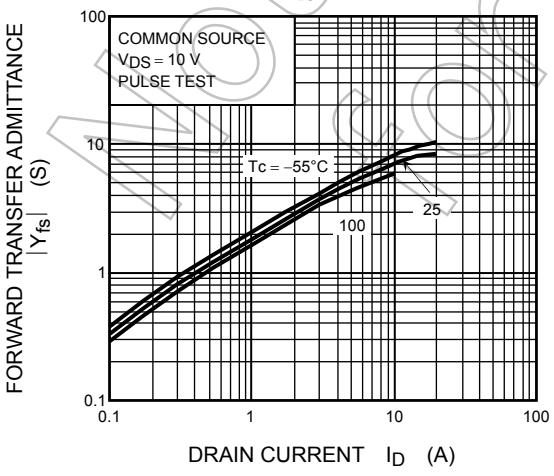
$I_D - V_{GS}$



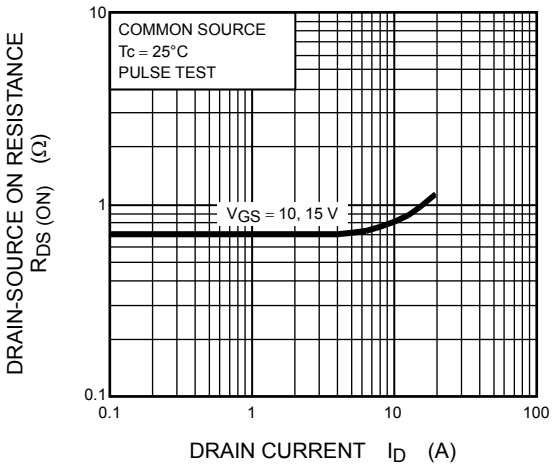
$V_{DS} - V_{GS}$



$|Y_{fs}| - I_D$

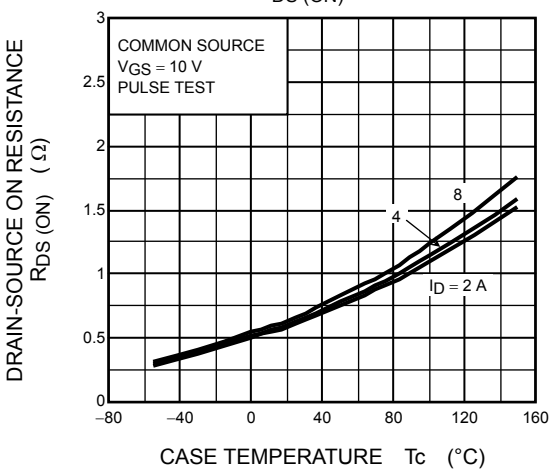


$R_{DS\ (ON)} - I_D$

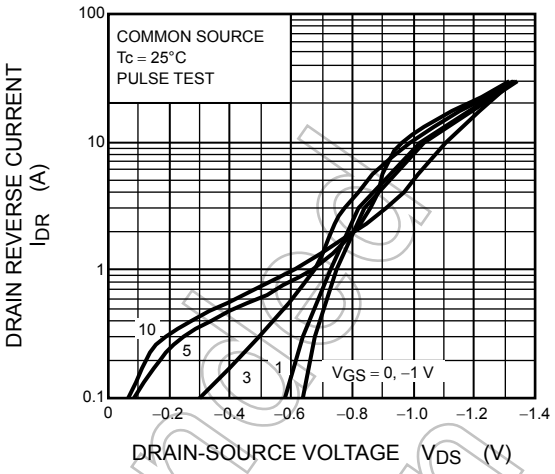


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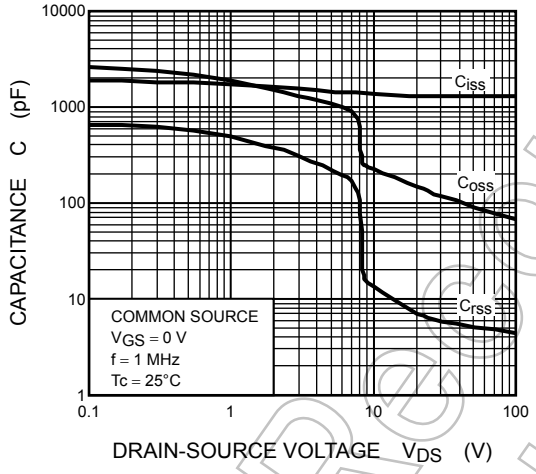
$R_{DS\ (ON)}$ – Tc



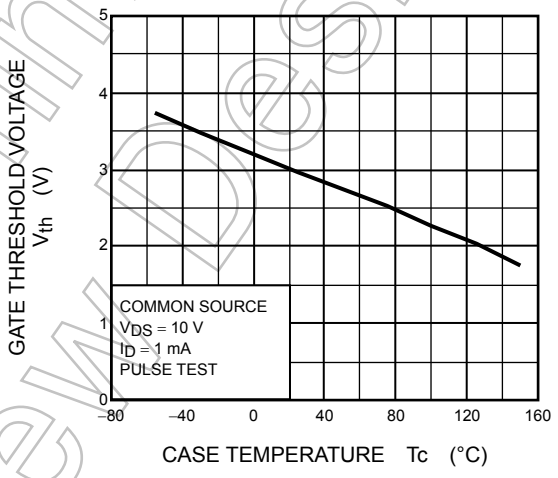
I_{DR} – V_{DS}



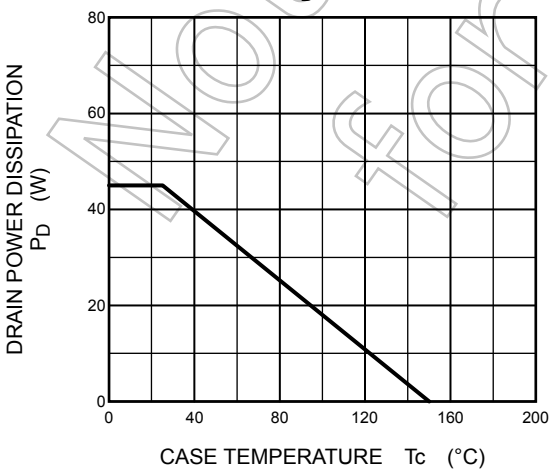
CAPACITANCE – V_{DS}



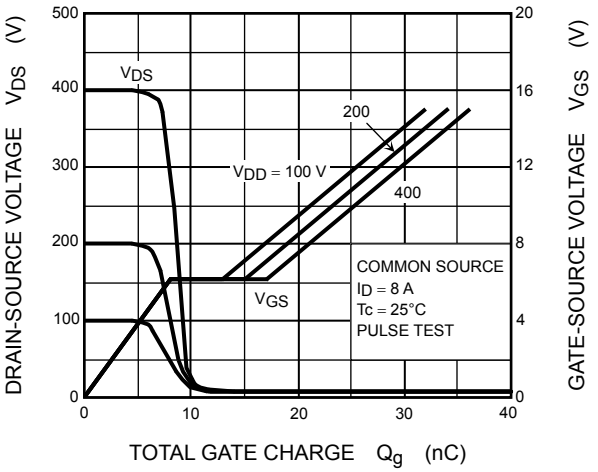
V_{th} – Tc



P_D – Tc

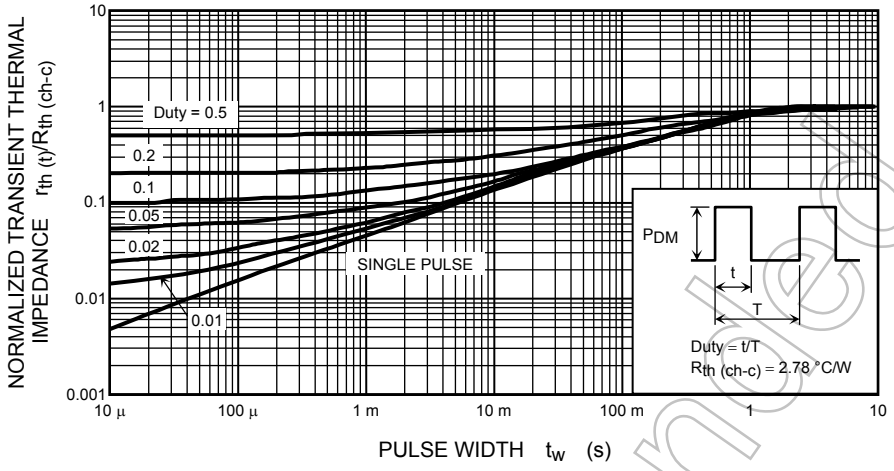


DYNAMIC INPUT / OUTPUT CHARACTERISTICS

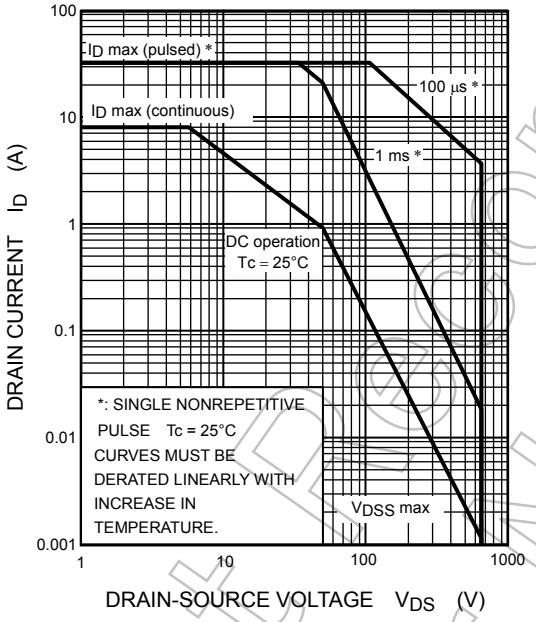


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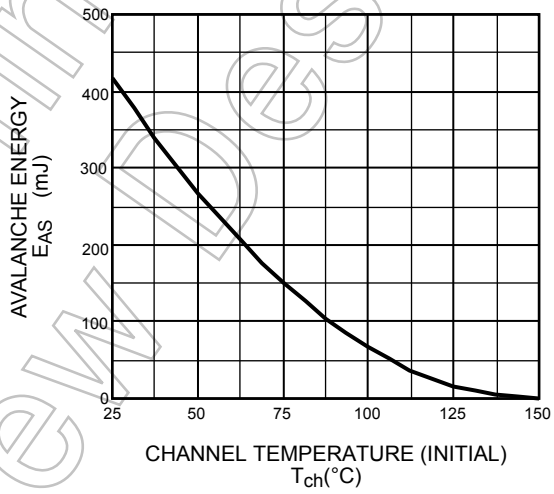
$r_{th} - t_w$

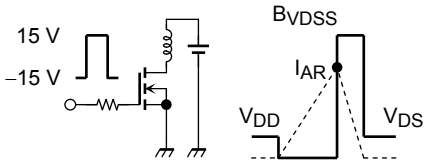


SAFE OPERATING AREA



$E_{AS} - T_{ch}$





TEST CIRCUIT WAVEFORM

$R_G = 25\ \Omega$
$V_{DD} = 90$ V, L = 11.5 mH

$$E_{AS} = \frac{1}{2} \cdot L \cdot I^2 \cdot \left(\frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$$

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