

# SSM6L14FE

- Power Management Switch Applications
- High-Speed Switching Applications

- N-ch: 1.5-V drive  
P-ch: 1.5-V drive
- N-ch, P-ch, 2-in-1
- Low ON-resistance Q1 N-ch:  $R_{DS(ON)} = 330 \text{ m}\Omega$  (max) (@ $V_{GS} = 2.5 \text{ V}$ )  
 $R_{DS(ON)} = 240 \text{ m}\Omega$  (max) (@ $V_{GS} = 4.5 \text{ V}$ )  
Q2 P-ch:  $R_{DS(ON)} = 440 \text{ m}\Omega$  (max) (@ $V_{GS} = -2.5 \text{ V}$ )  
 $R_{DS(ON)} = 300 \text{ m}\Omega$  (max) (@ $V_{GS} = -4.5 \text{ V}$ )

### Q1 Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain-source voltage		$V_{DSS}$	20	V
Gate-source voltage		$V_{GSS}$	±10	V
Drain current	DC	$I_D$	0.8	A
	Pulse	$I_{DP}$	1.6	

### Q2 Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain-source voltage		$V_{DSS}$	-20	V
Gate-source voltage		$V_{GSS}$	±8	V
Drain current	DC	$I_D$	-0.72	A
	Pulse	$I_{DP}$	-1.44	

### Absolute Maximum Ratings (Ta = 25 °C) (Q1, Q2 Common)

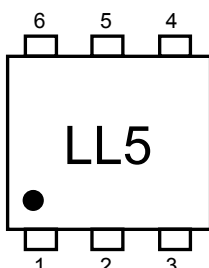
Characteristics	Symbol	Rating	Unit
Power dissipation	$P_D$ (Note 1)	150	mW
Channel temperature	$T_{ch}$	150	°C
Storage temperature range	$T_{stg}$	-55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

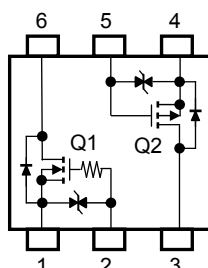
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note1: Mounted on an FR4 board. (total dissipation)  
(25.4 mm × 25.4 mm × 1.6 mm, Cu Pad: 0.135 mm<sup>2</sup> × 6)

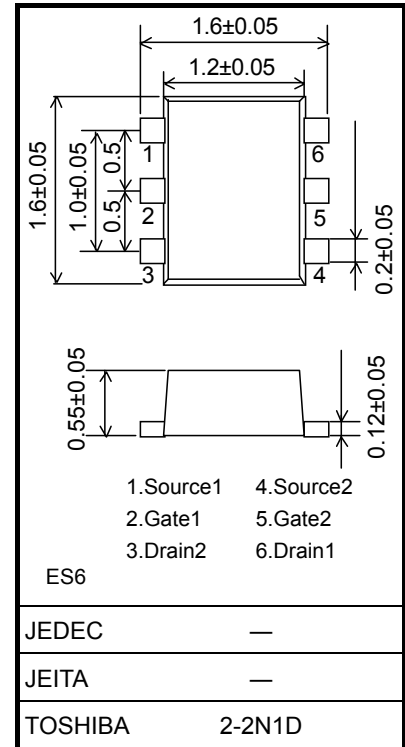
### Marking



### Equivalent Circuit (top view)



Unit: mm



Weight: 3.0 mg (typ.)

Start of commercial production  
2009-12

## Q1 Electrical Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Conditions	Min	Typ.	Max	Unit
Drain-source breakdown voltage	V (BR) DSS	I <sub>D</sub> = 1 mA, V <sub>GS</sub> = 0 V	20	—	—	V
	V (BR) DSX	I <sub>D</sub> = 1 mA, V <sub>GS</sub> = -10 V	12	—	—	
Drain cutoff current	I <sub>DSS</sub>	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V	—	—	1	μA
Gate leakage current	I <sub>GSS</sub>	V <sub>GS</sub> = ±8 V, V <sub>DS</sub> = 0 V	—	—	±1	μA
Gate threshold voltage	V <sub>th</sub>	V <sub>DS</sub> = 3 V, I <sub>D</sub> = 1 mA	0.35	—	1.0	V
Forward transfer admittance	Y <sub>fs</sub>	V <sub>DS</sub> = 3 V, I <sub>D</sub> = 500 mA (Note 2)	1.05	2.1	—	S
Drain-source ON-resistance	R <sub>DS (ON)</sub>	I <sub>D</sub> = 500 mA, V <sub>GS</sub> = 4.5 V (Note 2)	—	185	240	mΩ
		I <sub>D</sub> = 400 mA, V <sub>GS</sub> = 2.5 V (Note 2)	—	245	330	
		I <sub>D</sub> = 250 mA, V <sub>GS</sub> = 1.8 V (Note 2)	—	310	450	
		I <sub>D</sub> = 150 mA, V <sub>GS</sub> = 1.5 V (Note 2)	—	370	600	
Input capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 0 V, f = 1 MHz	—	90	—	pF
Output capacitance	C <sub>oss</sub>		—	21	—	
Reverse transfer capacitance	C <sub>rss</sub>		—	15	—	
Total gate charge	Q <sub>g</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 0.8 A V <sub>GS</sub> = 4.5 V	—	2.00	—	nC
Gate-source charge	Q <sub>gs</sub>		—	1.02	—	
Gate-drain charge	Q <sub>gd</sub>		—	0.98	—	
Switching time	Turn-on time	t <sub>on</sub>	V <sub>DD</sub> = 10 V, I <sub>D</sub> = 200 mA V <sub>GS</sub> = 0 to 2.5 V, R <sub>G</sub> = 4.7 Ω	—	18	ns
	Turn-off time	t <sub>off</sub>		—	50	
Drain-source forward voltage	V <sub>DSF</sub>	I <sub>D</sub> = -0.8 A, V <sub>GS</sub> = 0 V (Note 2)	—	-0.84	-1.2	V

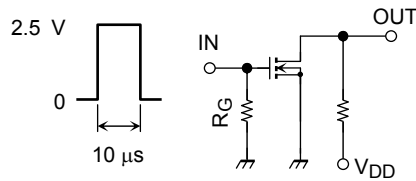
## Q2 Electrical Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Conditions	Min	Typ.	Max	Unit
Drain-source breakdown voltage	V (BR) DSS	I <sub>D</sub> = -1 mA, V <sub>GS</sub> = 0 V	-20	—	—	V
	V (BR) DSX	I <sub>D</sub> = -1 mA, V <sub>GS</sub> = 8 V	-12	—	—	
Drain cutoff current	I <sub>DSS</sub>	V <sub>DS</sub> = -20 V, V <sub>GS</sub> = 0 V	—	—	-10	μA
Gate leakage current	I <sub>GSS</sub>	V <sub>GS</sub> = ±8 V, V <sub>DS</sub> = 0 V	—	—	±1	μA
Gate threshold voltage	V <sub>th</sub>	V <sub>DS</sub> = -3 V, I <sub>D</sub> = -1 mA	-0.3	—	-1.0	V
Forward transfer admittance	Y <sub>fs</sub>	V <sub>DS</sub> = -3 V, I <sub>D</sub> = -400 mA (Note2)	850	—	—	mS
Drain-source ON-resistance	R <sub>DS (ON)</sub>	I <sub>D</sub> = -400 mA, V <sub>GS</sub> = -4.5 V (Note2)	—	0.25	0.30	Ω
		I <sub>D</sub> = -200 mA, V <sub>GS</sub> = -2.5 V (Note2)	—	0.34	0.44	
		I <sub>D</sub> = -100 mA, V <sub>GS</sub> = -1.8 V (Note2)	—	0.44	0.67	
		I <sub>D</sub> = -50 mA, V <sub>GS</sub> = -1.5 V (Note2)	—	0.55	1.04	
Input capacitance	C <sub>iss</sub>	V <sub>DS</sub> = -10 V, V <sub>GS</sub> = 0 V, f = 1 MHz	—	110	—	pF
Output capacitance	C <sub>oss</sub>		—	28	—	
Reverse transfer capacitance	C <sub>rss</sub>		—	20	—	
Total gate charge	Q <sub>g</sub>	V <sub>DS</sub> = -10 V, I <sub>DS</sub> = -720 mA V <sub>GS</sub> = -4.5 V	—	1.76	—	nC
Gate-source charge	Q <sub>gs</sub>		—	1.22	—	
Gate-drain charge	Q <sub>gd</sub>		—	0.54	—	
Switching time	Turn-on time	t <sub>on</sub>	V <sub>DD</sub> = -10 V, I <sub>D</sub> = -100 mA V <sub>GS</sub> = 0 to -2.5 V, R <sub>G</sub> = 50 Ω	—	11	ns
	Turn-off time	t <sub>off</sub>		—	38	
Drain-source forward voltage	V <sub>DSF</sub>	I <sub>D</sub> = 720 mA, V <sub>GS</sub> = 0 V (Note2)	—	0.85	1.2	V

Note 2: Pulse test

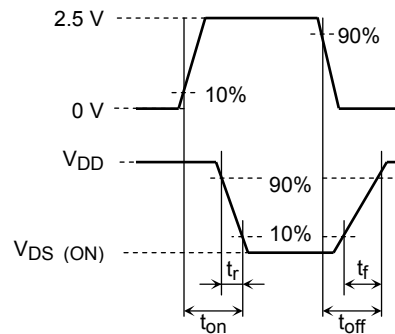
**Q1 Switching Time Test Circuit**

**(a) Test Circuit**

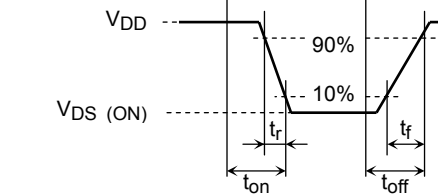


$V_{DD} = 10\text{ V}$   
 $R_G = 4.7\ \Omega$   
 Duty  $\leq 1\%$   
 $V_{IN}$ :  $t_r, t_f < 5\text{ ns}$   
 Common Source  
 $T_a = 25^\circ\text{C}$

**(b)  $V_{IN}$**

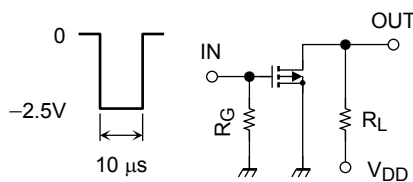


**(c)  $V_{OUT}$**



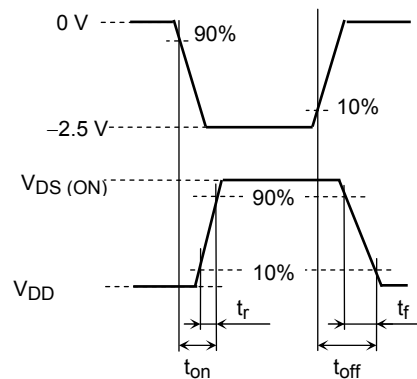
**Q2 Switching Time Test Circuit**

**(a) Test Circuit**

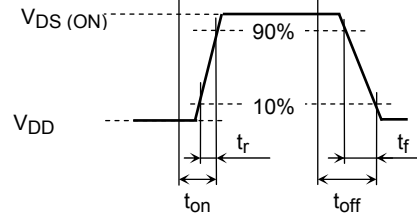


$V_{DD} = -10\text{ V}$   
 $R_G = 50\ \Omega$   
 Duty  $\leq 1\%$   
 $V_{IN}$ :  $t_r, t_f < 5\text{ ns}$   
 Common Source  
 $T_a = 25^\circ\text{C}$

**(b)  $V_{IN}$**



**(c)  $V_{OUT}$**



**Q1 Usage Considerations**

Let  $V_{th}$  be the voltage applied between gate and source that causes the drain current ( $I_D$ ) to be below (1 mA for the Q1 of the SSM6L14FE). Then, for normal switching operation,  $V_{GS(on)}$  must be higher than  $V_{th}$ , and  $V_{GS(off)}$  must be lower than  $V_{th}$ . This relationship can be expressed as:  $V_{GS(off)} < V_{th} < V_{GS(on)}$ .

Take this into consideration when using the device.

**Q2 Usage Considerations**

Let  $V_{th}$  be the voltage applied between gate and source that causes the drain current ( $I_D$ ) to be below (-1 mA for the Q2 of the SSM6L14FE). Then, for normal switching operation,  $V_{GS(on)}$  must be higher than  $V_{th}$ , and  $V_{GS(off)}$  must be lower than  $V_{th}$ . This relationship can be expressed as:  $V_{GS(off)} < V_{th} < V_{GS(on)}$ .

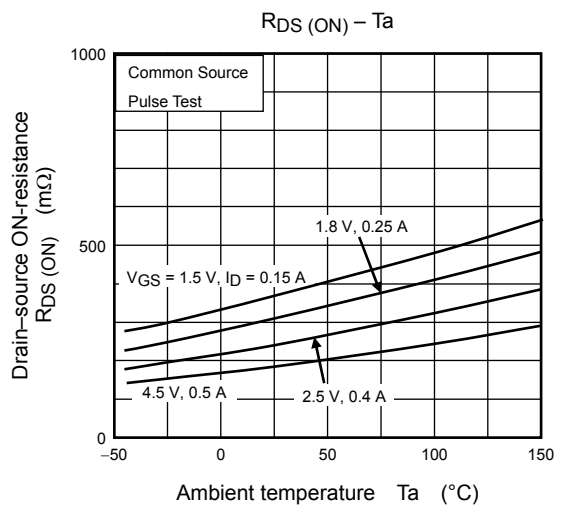
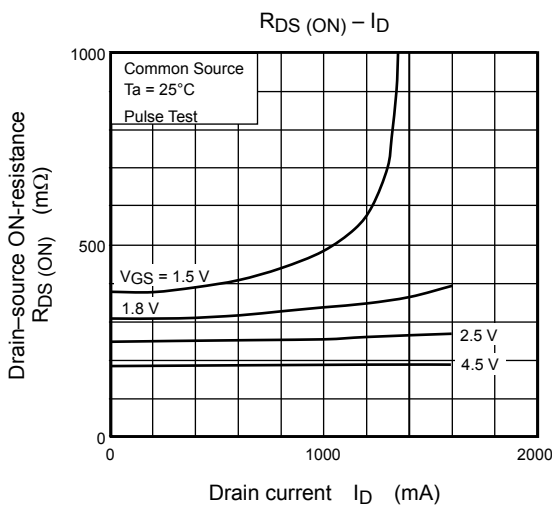
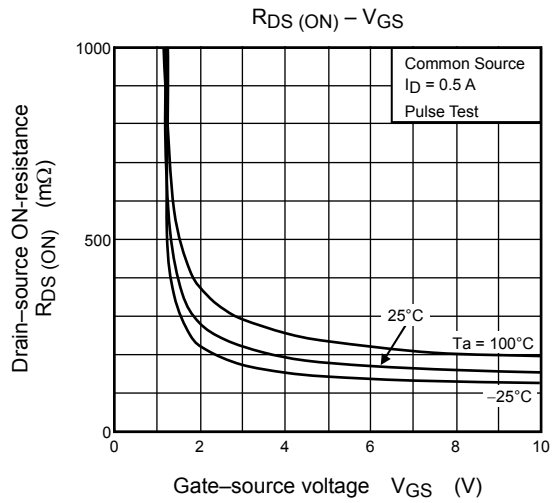
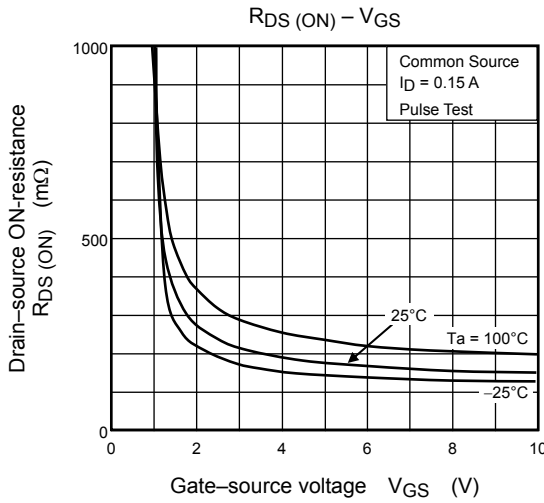
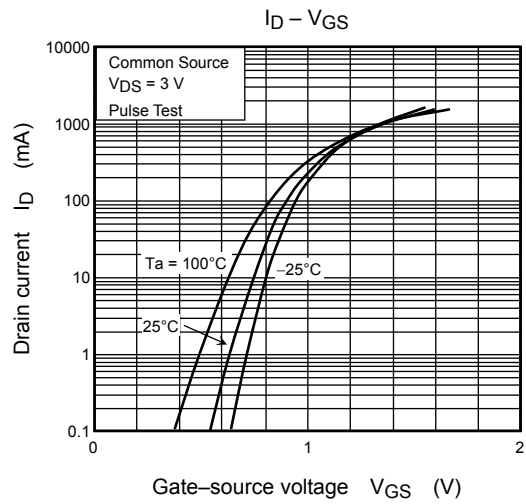
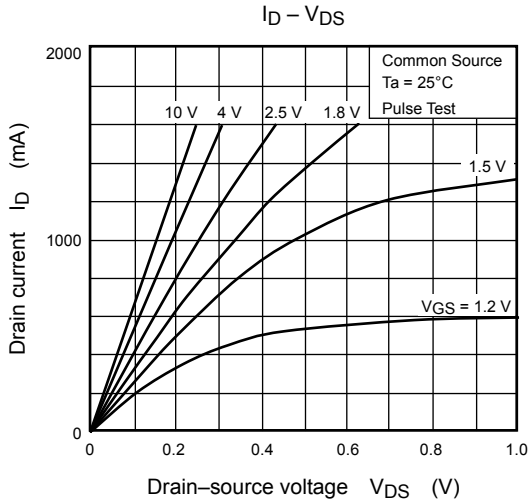
Take this into consideration when using the device.

**Handling Precaution**

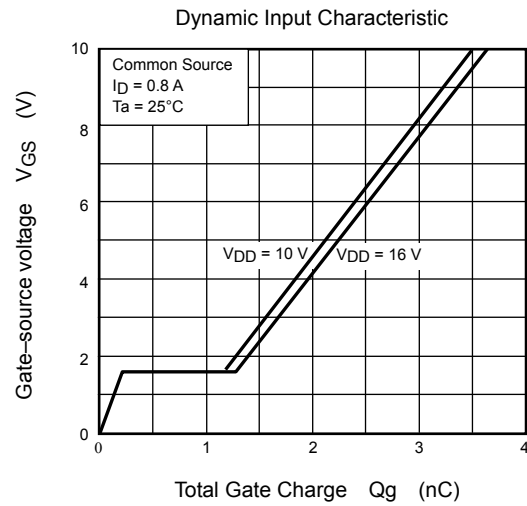
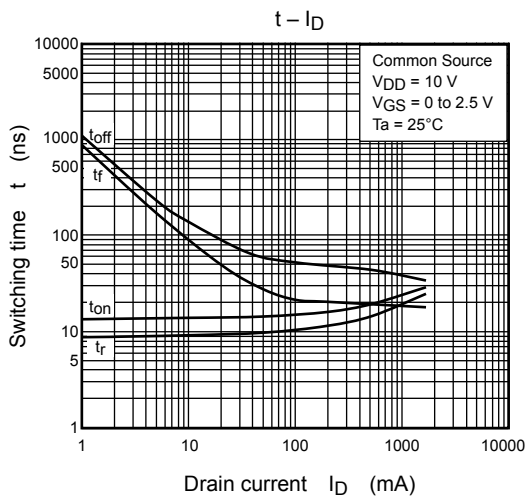
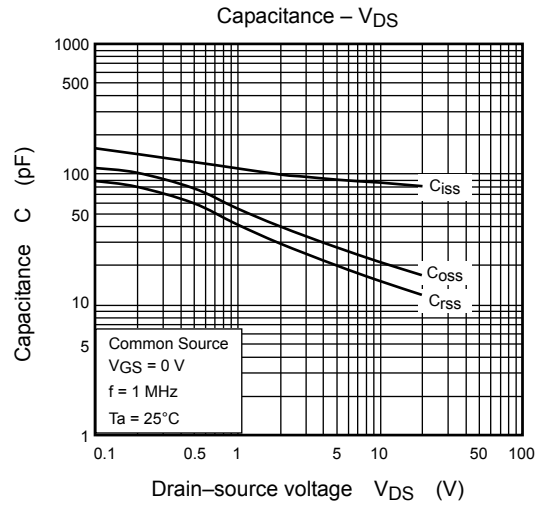
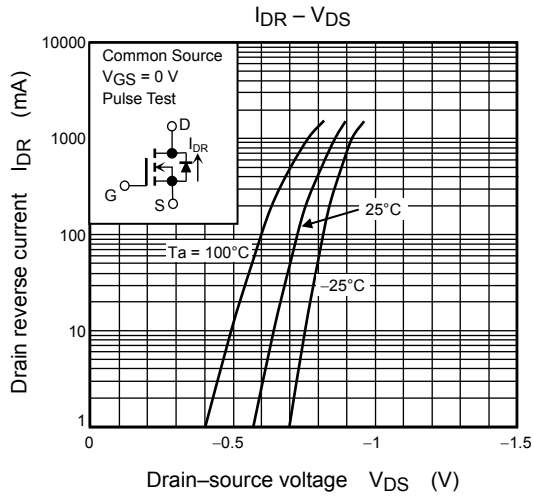
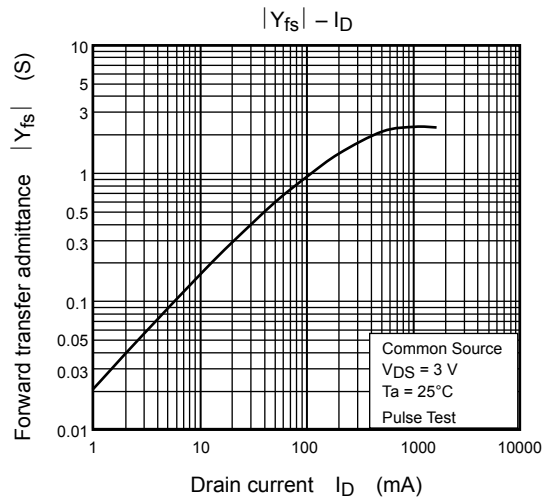
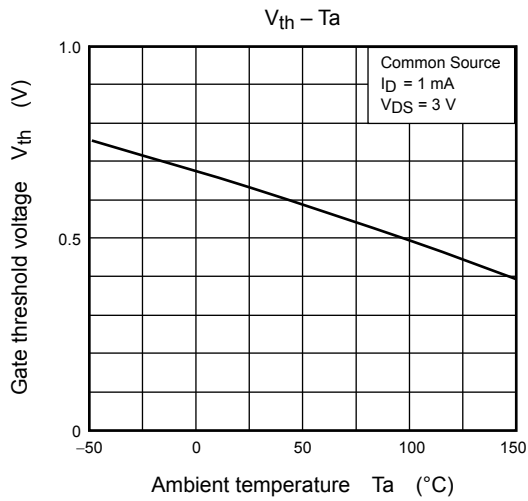
When handling individual devices that are not yet mounted on a circuit board, make sure that the environment is protected against electrostatic discharge. Operators should wear antistatic clothing, and containers and other objects that come into direct contact with devices should be made of antistatic materials.

Thermal resistance  $R_{th(ch-a)}$  and power dissipation  $P_D$  vary depending on board material, board area, board thickness and pad area. When using this device, please take heat dissipation into consideration

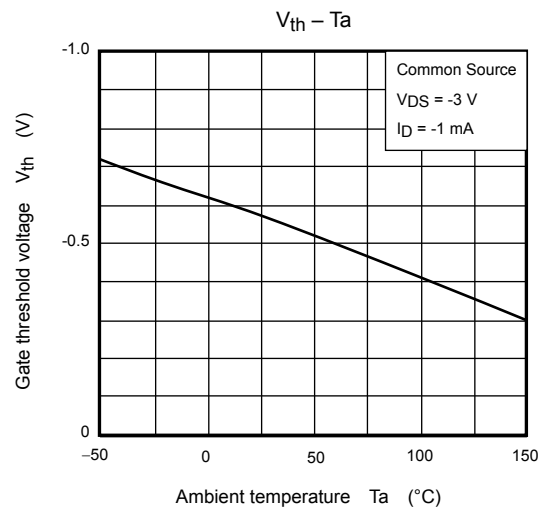
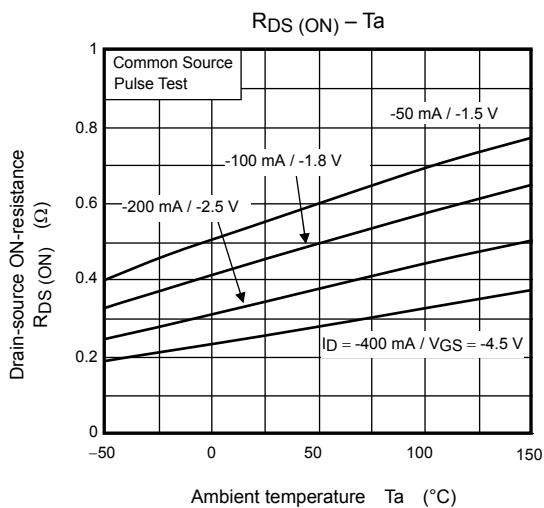
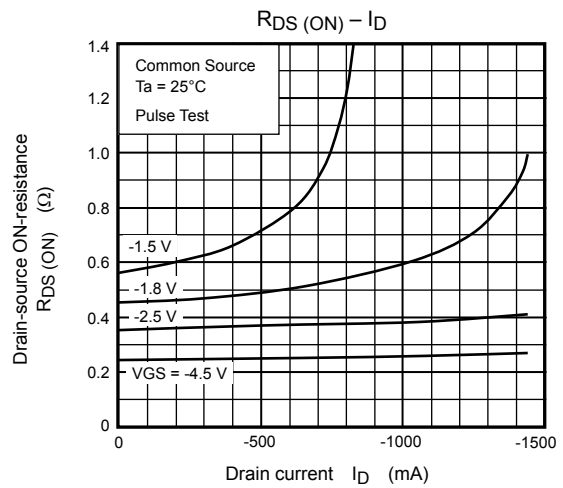
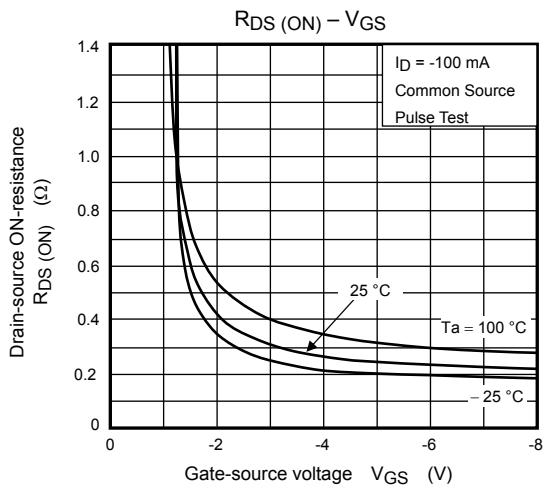
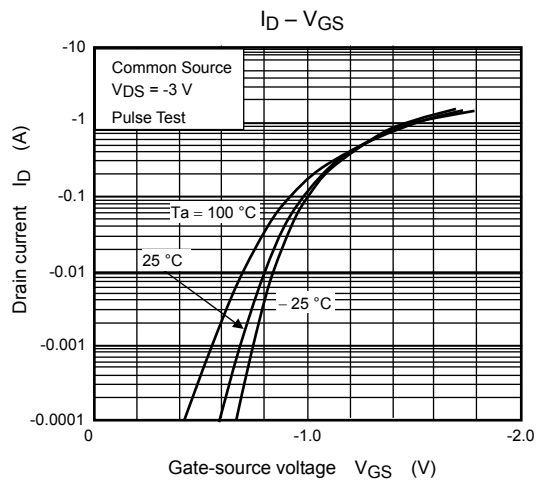
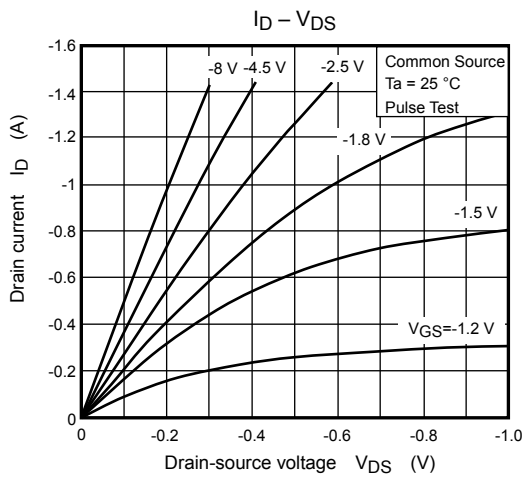
**Q1 (N-ch MOSFET)**



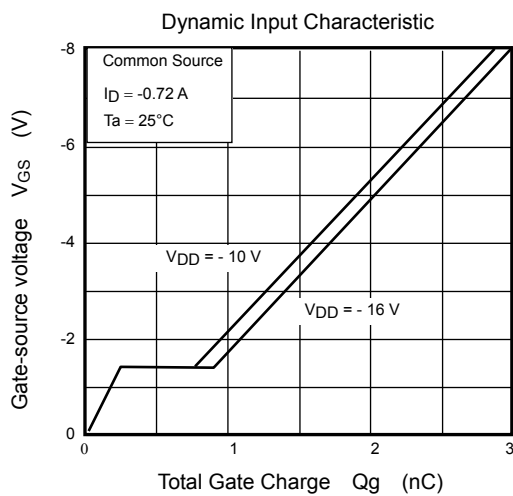
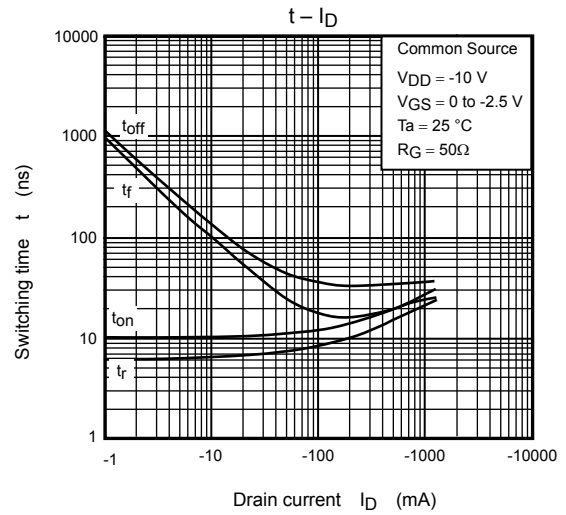
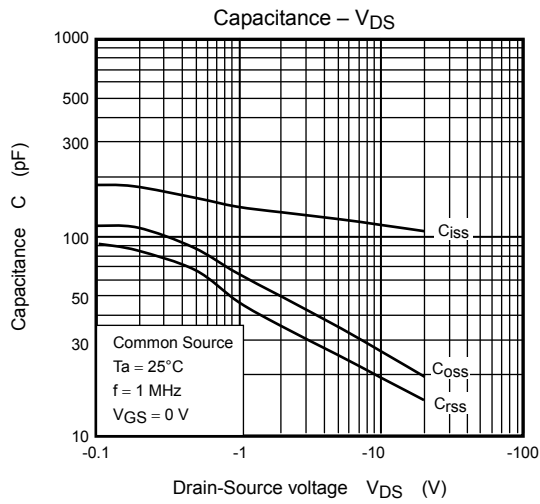
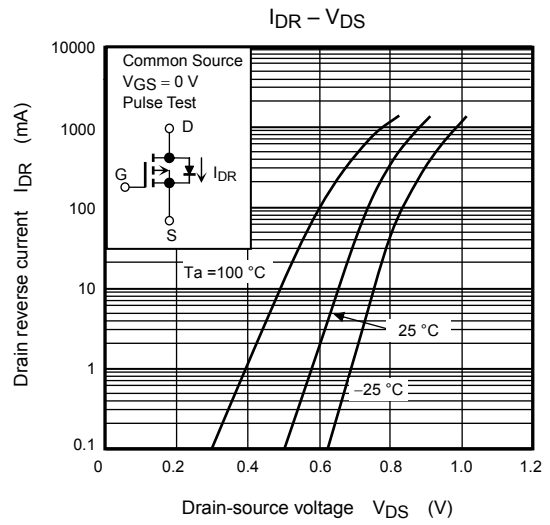
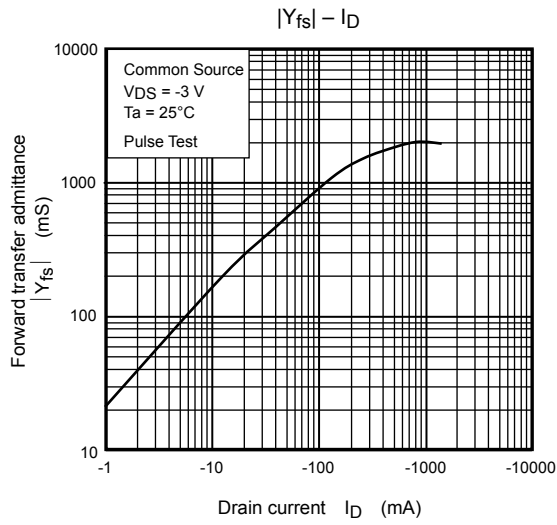
## Q1 (N-ch MOSFET)



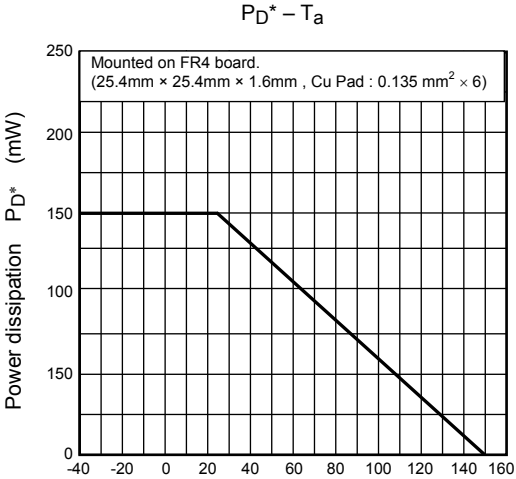
## Q2 (P-ch MOSFET)



## Q2 (P-ch MOSFET)



Q1, Q2 Common



\*:Total Rating    Ambient temperature  $T_a$  (°C)



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