TOSHIBA Field Effect Transistor Silicon N-Channel MOS Type ($L^2 - \pi - MOS V$)

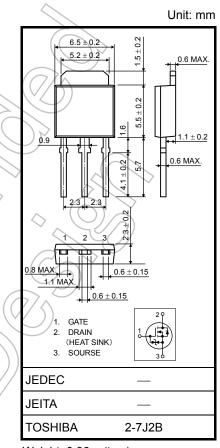
2SK4018

Chopper Regulator, DC-DC Converter and Motor Drive Applications

- 4-V gate drive
- Low drain-source ON-resistance: $R_{DS (ON)} = 0.28 \Omega$ (typ.)
- High forward transfer admittance: |Y_{fs}| = 3.5 S (typ.)
- Low leakage current: $I_{DSS} = 100 \ \mu A \ (max) \ (V_{DS} = 100 \ V)$
- Enhancement mode: V_{th} = 0.8 to 2.0 V (V_{DS} = 10 V, I_D = 1 mA)

Absolute Maximum Ratings (Ta = 25°C)

Init
Y
V
V
А
A
W
mJ
А
Jm
°C
°C



Weight: 0.36 g (typ.)

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Thermal Characteristics

Characteristic	Symbol	Мах	Unit
Thermal resistance, channel to case	R _{th (ch-c)}	6.25	°C / W
Thermal resistance, channel to ambient	R _{th (ch-a)}	125	°C / W

Note 1: Ensure that the channel temperature does not exceed 150°C.

Note 2: V_{DD} = 50 V, T_{ch} = 25°C (initial), L = 25 mH, R_G = 25 Ω , I_{AR} = 3 A

Note 3: Repetitive rating: pulse width limited by maximum channel temperature

This transistor is an electrostatic-sensitive device. Handle with care.

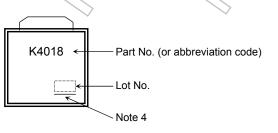
Electrical Characteristics (Ta = 25°C)

Chara	cteristic	Symbol	Test Condition	Min	Тур.	Max	Unit
Gate leakage cu	urrent	I _{GSS}	V _{GS} = ±16 V, V _{DS} = 0 V	_	_	±10	μΑ
Drain cutoff curr	ent	IDSS	V _{DS} = 100 V, V _{GS} = 0 V	_		100	μA
Drain-source br	reakdown voltage	V (BR) DSS	I _D = 10 mA, V _{GS} = 0 V	100	_		V
Gate threshold	voltage	V _{th}	V _{DS} = 10 V, I _D = 1 mA	0.8	-	2.0	V
Davia a contra ON accietar		R _{DS (ON)}	V _{GS} = 4 V, I _D = 2 A	Æ	0.36	0.45	Ω
Drain-source O	ain-source ON-resistance		V _{GS} = 10 V, I _D = 2 A	$\sqrt{2}$	0.28	0.35	52
Forward transfe	r admittance	Y _{fs}	V _{DS} = 10 V, I _D = 2 A	1.5	3.5	_	S
Input capacitance		C _{iss}		_	280		
Reverse transfer capacitance		C _{rss}	V _{DS} = 10 V, V _{GS} = 0 V, f = 1 MHz	[^] —	50		pF
Output capacitance		C _{oss}		_	105		
Switching time	Rise time	tr	$v_{\rm GS} {}^{10V}_{\rm OV} \prod I_{\rm D} = 2A$	- (20		
	Turn-on time	t _{on}	$\begin{array}{c} \mathbf{C} \mathbf{C} \mathbf{C} \mathbf{C} \mathbf{C} \mathbf{C} \mathbf{C} C$		50) —	
	Fall time	t _f			40	_	ns
	Turn-off time	t _{off}	$V_{DD} \approx 50V$ Duty $\leq 1\%$, $t_w = 10 \mu s$) -	170	_	
Total gate charge (gate-source plus gate-drain)		Qg		_	13.5	_	
Gate-source charge		Q _{gs}	$V_{DD} \approx 80 \text{ V}, \text{ V}_{GS} = 10 \text{ V}, \text{ I}_{D} = 3 \text{ A}$	_	8.5	_	nC
Gate-drain ("Miller") charge		Q _{gd}		_	5	—	

Source–Drain Ratings and Characteristics (Ta = 25°C)

Characteristic	Symbol	Test Condition	Min	Тур.	Max	Unit
Continuous drain reverse current (Note 1)	IDR		_	_	3	A
Pulse drain reverse current (Note 1)	I _{DRP}			_	12	A
Forward voltage (diode)	V _{DSF}	I _{DR} = 3 A, V _{GS} = 0 V	-	_	-1.5	V
Reverse recovery time	t _{rr}	I _{DR} = 3 A, V _{GS} = 0 V, dI _{DR} / dt = 50 A / μs	-	100	_	ns
Reverse recovery charge	Q _{rr}	$DR = 3 A$, $VGS = 0 V$, $diDR / di = 50 A / \mu s$	_	0.2	_	μC

Marking

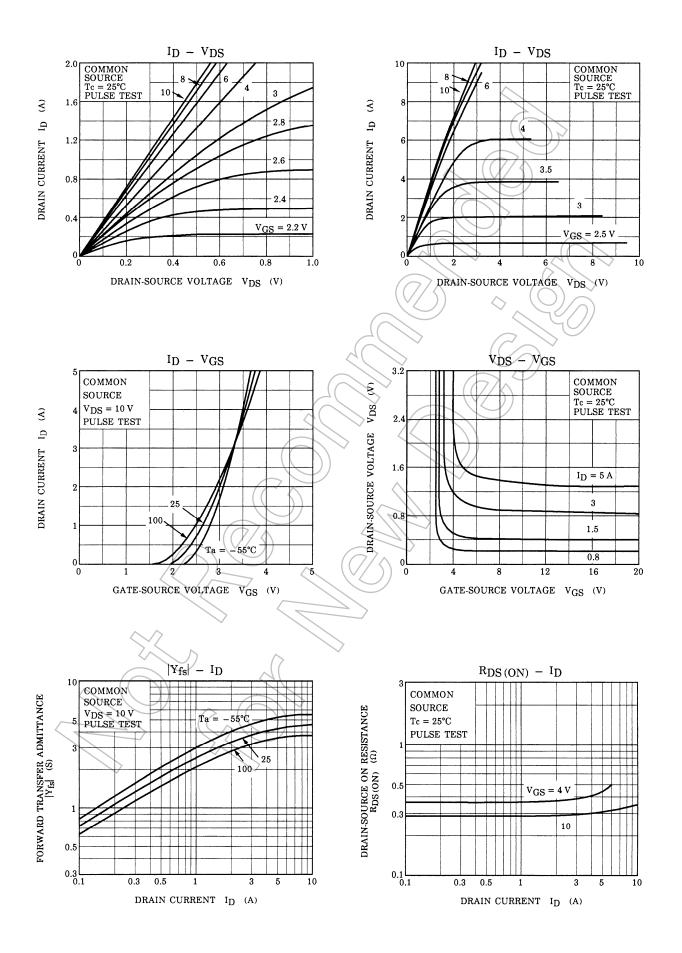


Note 4: A line under a Lot No. identifies the indication of product Labels.

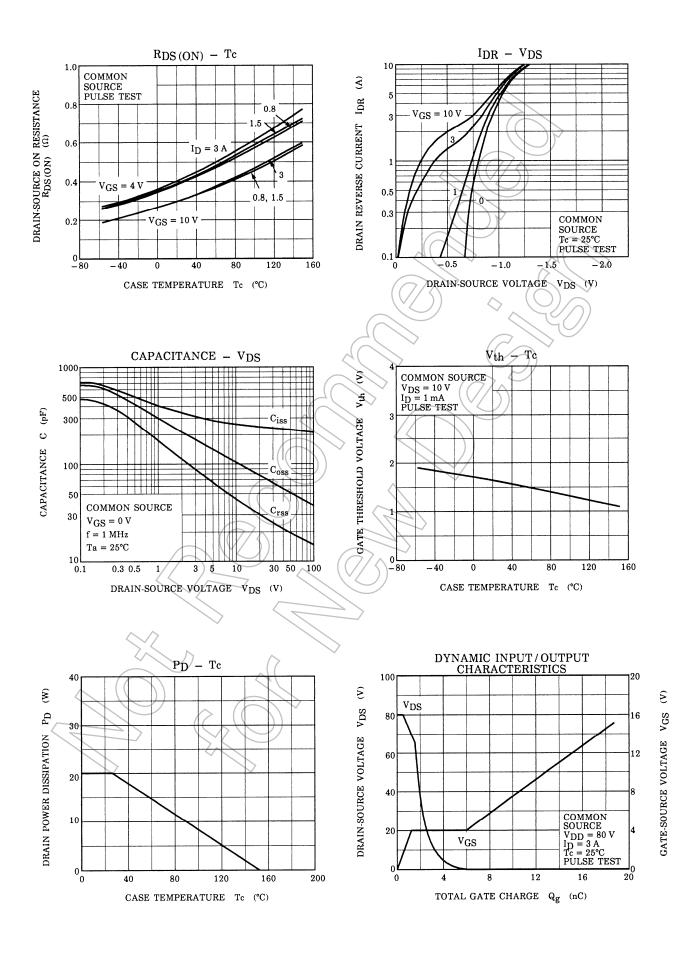
[[G]]/RoHS COMPATIBLE or [[G]]/RoHS [[Pb]]

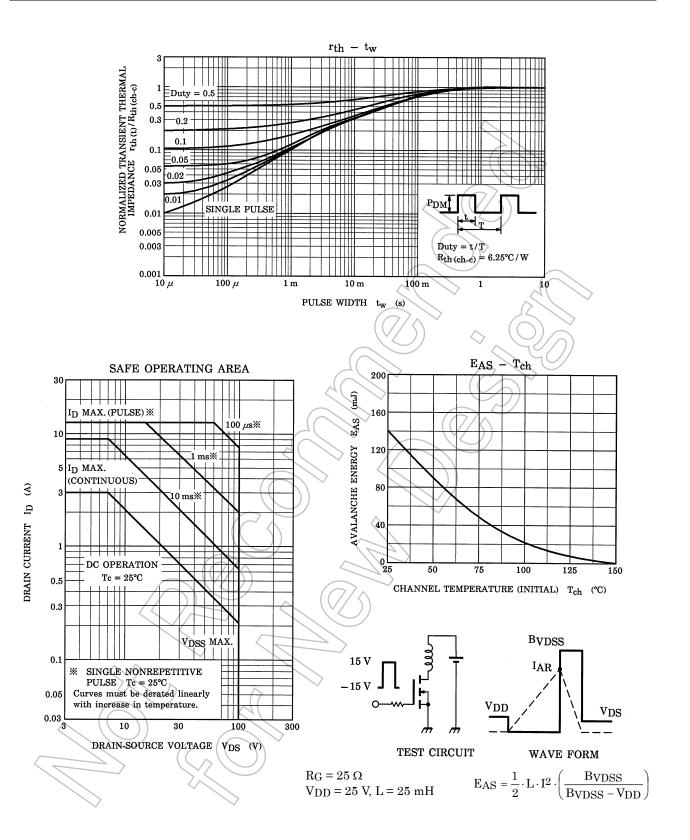
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