

74VHCV374FT

1. Functional Description

- Octal Schmitt D-Type Flip-Flop with 3-State Outputs

2. General

The 74VHCV374FT is an advanced high speed CMOS OCTAL FLIP-FLOP with 3-STATE OUTPUT fabricated with silicon gate CMOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

This 8-bit D-type flip-flop is controlled by a clock input (CK) and an output enable input (\overline{OE}).

When the \overline{OE} input is high, the eight outputs are in a high impedance state.

Input pin have hysteresis between the positive-going and negative-going thresholds. Thus the 74VHCV374FT are capable of squaring up transitions of slowly changing input signals and provides an improved noise immunity.

Input protection and output circuit ensure that 0 to 5.5 V can be applied to the input and output (Note) pins without regard to the supply voltage. These structure prevents device destruction due to mismatched supply and input/output voltages such as battery back up, hot board insertion, etc.

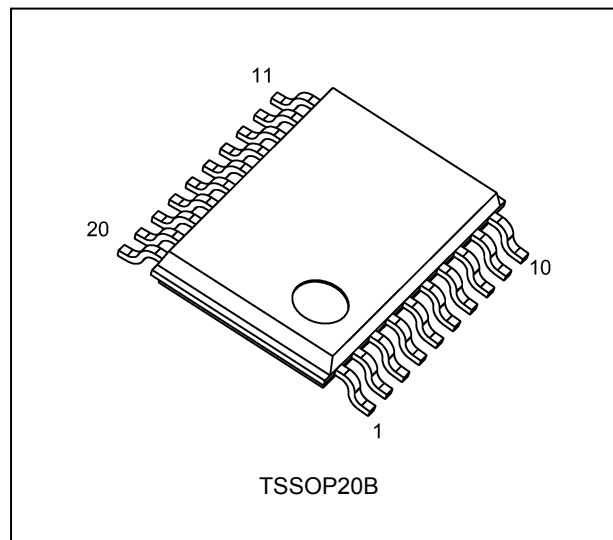
Note: Output in off-state

3. Features

- (1) AEC-Q100 (Rev. H) (Note 1)
- (2) Wide operating temperature range: $T_{opr} = -40$ to 125 °C
- (3) High speed: $f_{MAX} = 185$ MHz (typ.) at $V_{CC} = 5.0$ V
- (4) Low power dissipation: $I_{CC} = 2.0$ μ A (max) at $T_a = 25$ °C
- (5) Wide operating voltage range: $V_{CC(opr)} = 1.8$ V to 5.5 V
- (6) Output current: $|I_{OH}|/I_{OL} = 16$ mA (min)($V_{CC} = 4.5$ V)
- (7) Power-down protection is provided on all inputs and outputs.
- (8) Pin and function compatible with the 74 series (74AC/HC/AHC/LV etc.) 374 type.

Note 1: This device is compliant with the reliability requirements of AEC-Q100. For details, contact your Toshiba sales representative.

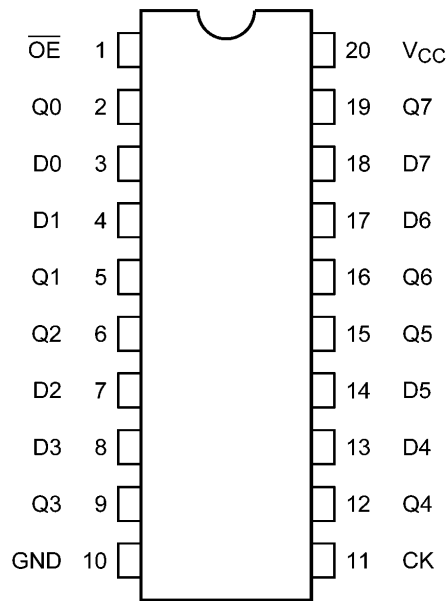
4. Packaging



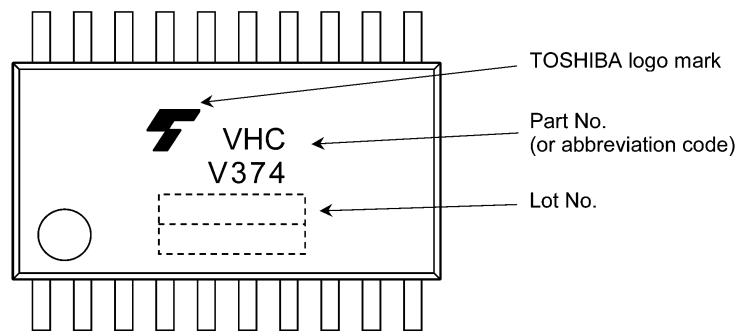
Start of commercial production

2015-02

5. Pin Assignment



6. Marking

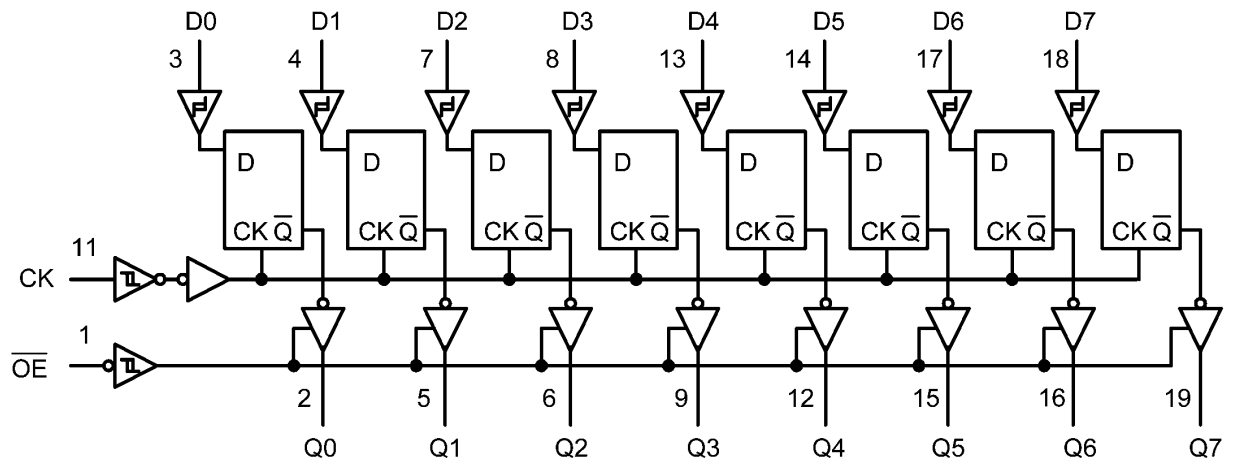


7. Truth Table

Inputs			Output
\overline{OE}	CK	D	
H	X	X	Z
L	\downarrow	X	Qn
L	\uparrow	L	L
L	\uparrow	H	H

X: Don't care
 Z: High impedance
 Qn: No change

8. System Diagram



9. Absolute Maximum Ratings (Note)

Characteristics	Symbol	Note	Rating	Unit
Supply voltage	V_{CC}		-0.5 to 7.0	V
Input voltage	V_{IN}		-0.5 to 7.0	V
Output voltage	V_{OUT}	(Note 1)	-0.5 to 7.0	V
		(Note 2)	-0.5 to $V_{CC} + 0.5$	
Input diode current	I_{IK}		-50	mA
Output diode current	I_{OK}	(Note 3)	± 50	mA
Output current	I_{OUT}		± 50	mA
Power dissipation	P_D	(Note 4)	180	mW
V_{CC} /ground current	I_{CC}/I_{GND}		± 100	mA
Storage temperature	T_{stg}		-65 to 150	$^{\circ}C$

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Output in OFF state.

Note 2: High (H) or Low (L) state. I_{OUT} absolute maximum rating must be observed.

Note 3: $V_{OUT} < GND$, $V_{OUT} > V_{CC}$

Note 4: 180 mW in the range of $T_a = -40$ to $85^{\circ}C$. From $T_a = 85$ to $125^{\circ}C$ a derating factor of -3.25 mW/ $^{\circ}C$ shall be applied until 50 mW.

10. Operating Ranges (Note)

Characteristics	Symbol	Test Condition	Note	Rating	Unit
Supply voltage	V_{CC}	—		1.8 to 5.5	V
Input voltage	V_{IN}	—		0 to 5.5	V
Output voltage	V_{OUT}	—	(Note 1)	0 to 5.5	V
			(Note 2)	0 to V_{CC}	
Operating temperature	T_{opr}	—		-40 to 125	$^{\circ}C$
Input rise and fall times	dt/dv	$V_{CC} = 3.3 \pm 0.3$ V		0 to 20	ms/V
		$V_{CC} = 5.0 \pm 0.5$ V		0 to 1	

Note: The operating ranges must be maintained to ensure the normal operation of the device.

Unused inputs must be tied to either V_{CC} or GND.

Note 1: Output in OFF state.

Note 2: High (H) or Low (L) state.

11. Electrical Characteristics

11.1. DC Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Min	Typ.	Max	Unit	
Positive threshold voltage	V_P	—	1.8	—	—	1.65	V	
			2.3	—	—	1.85		
			3.0	—	—	2.20		
			4.5	—	—	3.15		
			5.5	—	—	3.85		
Negative threshold voltage	V_N	—	1.8	0.15	—	—	V	
			2.3	0.45	—	—		
			3.0	0.90	—	—		
			4.5	1.35	—	—		
			5.5	1.65	—	—		
Hysteresis voltage	V_H	—	1.8	0.15	—	1.05	V	
			2.3	0.20	—	1.10		
			3.0	0.30	—	1.20		
			4.5	0.40	—	1.40		
			5.5	0.50	—	1.60		
High-level output voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -50\text{ }\mu\text{A}$	1.8	1.7	1.8	—	V
				3.0	2.9	3.0	—	
			$I_{OH} = -8\text{ mA}$	4.5	4.4	4.5	—	
				$I_{OH} = -16\text{ mA}$	3.0	2.58	—	
			4.5		3.94	—	—	
			Low-level output voltage	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 50\text{ }\mu\text{A}$	1.8	—
3.0	—	0.0					0.1	
4.5	—	0.0					0.1	
$I_{OL} = 8\text{ mA}$	3.0	—				—	0.36	
	$I_{OL} = 16\text{ mA}$	4.5				—	—	0.44
3-state output OFF-state leakage current		I_{OZ}	$V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = 0$ to 5.5 V	1.8 to 5.5	—	—	± 0.5	μA
Power-OFF leakage current	I_{OFF}	$V_{IN}/V_{OUT} = 5.5\text{ V}$	0	—	—	0.5	μA	
Input leakage current	I_{IN}	$V_{IN} = 5.5\text{ V}$ or GND	0 to 5.5	—	—	± 0.1	μA	
Quiescent supply current	I_{CC}	$V_{IN} = V_{CC}$ or GND	5.5	—	—	2.0	μA	

11.2. DC Characteristics (Unless otherwise specified, $T_a = -40$ to 85 °C)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Min	Max	Unit	
Positive threshold voltage	V_P	—	1.8	—	1.65	V	
			2.3	—	1.85		
			3.0	—	2.20		
			4.5	—	3.15		
			5.5	—	3.85		
Negative threshold voltage	V_N	—	1.8	0.15	—	V	
			2.3	0.45	—		
			3.0	0.90	—		
			4.5	1.35	—		
			5.5	1.65	—		
Hysteresis voltage	V_H	—	1.8	0.15	1.05	V	
			2.3	0.20	1.10		
			3.0	0.30	1.20		
			4.5	0.40	1.40		
			5.5	0.50	1.60		
High-level output voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -50 \mu A$	1.8	1.7	—	V
				3.0	2.9	—	
				4.5	4.4	—	
			$I_{OH} = -8 mA$	3.0	2.48	—	
				4.5	3.80	—	
Low-level output voltage	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 50 \mu A$	1.8	—	0.1	V
				3.0	—	0.1	
				4.5	—	0.1	
			$I_{OL} = 8 mA$	3.0	—	0.44	
				4.5	—	0.55	
3-state output OFF-state leakage current	I_{OZ}	$V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = 0$ to $5.5 V$	1.8 to 5.5	—	± 5.0	μA	
Power-OFF leakage current	I_{OFF}	$V_{IN}/V_{OUT} = 5.5 V$	0	—	5.0	μA	
Input leakage current	I_{IN}	$V_{IN} = 5.5 V$ or GND	0 to 5.5	—	± 1.0	μA	
Quiescent supply current	I_{CC}	$V_{IN} = V_{CC}$ or GND	5.5	—	20.0	μA	

11.3. DC Characteristics (Unless otherwise specified, $T_a = -40$ to 125 °C)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Min	Max	Unit	
Positive threshold voltage	V_P	—	1.8	—	1.65	V	
			2.3	—	1.85		
			3.0	—	2.20		
			4.5	—	3.15		
			5.5	—	3.85		
Negative threshold voltage	V_N	—	1.8	0.15	—	V	
			2.3	0.45	—		
			3.0	0.90	—		
			4.5	1.35	—		
			5.5	1.65	—		
Hysteresis voltage	V_H	—	1.8	0.15	1.05	V	
			2.3	0.20	1.10		
			3.0	0.30	1.20		
			4.5	0.40	1.40		
			5.5	0.50	1.60		
High-level output voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -50 \mu A$	1.8	1.7	—	V
				3.0	2.9	—	
				4.5	4.4	—	
			$I_{OH} = -8 mA$	3.0	2.40	—	
				4.5	3.70	—	
Low-level output voltage	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 50 \mu A$	1.8	—	0.1	V
				3.0	—	0.1	
				4.5	—	0.1	
			$I_{OL} = 8 mA$	3.0	—	0.55	
				4.5	—	0.65	
3-state output OFF-state leakage current	I_{OZ}	$V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = 0$ to $5.5 V$	1.8 to 5.5	—	± 20.0	μA	
Power-OFF leakage current	I_{OFF}	$V_{IN}/V_{OUT} = 5.5 V$	0	—	20.0	μA	
Input leakage current	I_{IN}	$V_{IN} = 5.5 V$ or GND	0 to 5.5	—	± 2.0	μA	
Quiescent supply current	I_{CC}	$V_{IN} = V_{CC}$ or GND	5.5	—	40.0	μA	

11.4. Timing Requirements (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$, Input: $t_r = t_f = 3\text{ ns}$)

Characteristics	Symbol	V_{CC} (V)	Limit	Unit
Minimum pulse width (CK)	$t_{w(L)}, t_{w(H)}$	2.5 ± 0.2	6.0	ns
		3.3 ± 0.3	5.0	
		5.0 ± 0.5	5.0	
Minimum setup time	t_s	2.5 ± 0.2	5.0	ns
		3.3 ± 0.3	4.5	
		5.0 ± 0.5	3.0	
Minimum hold time	t_h	2.5 ± 0.2	2.5	ns
		3.3 ± 0.3	2.0	
		5.0 ± 0.5	2.0	

11.5. Timing Requirements (Unless otherwise specified, $T_a = -40\text{ to }85\text{ }^\circ\text{C}$, Input: $t_r = t_f = 3\text{ ns}$)

Characteristics	Symbol	V_{CC} (V)	Limit	Unit
Minimum pulse width (CK)	$t_{w(L)}, t_{w(H)}$	2.5 ± 0.2	7.0	ns
		3.3 ± 0.3	5.5	
		5.0 ± 0.5	5.0	
Minimum setup time	t_s	2.5 ± 0.2	5.5	ns
		3.3 ± 0.3	4.5	
		5.0 ± 0.5	3.0	
Minimum hold time	t_h	2.5 ± 0.2	2.5	ns
		3.3 ± 0.3	2.0	
		5.0 ± 0.5	2.0	

11.6. Timing Requirements (Unless otherwise specified, $T_a = -40\text{ to }125\text{ }^\circ\text{C}$, Input: $t_r = t_f = 3\text{ ns}$)

Characteristics	Symbol	V_{CC} (V)	Limit	Unit
Minimum pulse width (CK)	$t_{w(L)}, t_{w(H)}$	2.5 ± 0.2	7.0	ns
		3.3 ± 0.3	5.5	
		5.0 ± 0.5	5.0	
Minimum setup time	t_s	2.5 ± 0.2	6.0	ns
		3.3 ± 0.3	4.5	
		5.0 ± 0.5	3.0	
Minimum hold time	t_h	2.5 ± 0.2	2.5	ns
		3.3 ± 0.3	2.0	
		5.0 ± 0.5	2.0	

11.7. AC Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$, Input: $t_r = t_f = 3\text{ ns}$)

Characteristics	Symbol	Note	Test Condition	V_{CC} (V)	C_L (pF)	Min	Typ.	Max	Unit
Propagation delay time (CK-Q)	t_{PLH}, t_{PHL}		—	2.5 ± 0.2	15	—	12.1	16.3	ns
					50	—	14.9	19.3	
				3.3 ± 0.3	15	—	7.1	12.7	
					50	—	9.2	16.2	
				5.0 ± 0.5	15	—	5.4	8.1	
					50	—	7.1	10.1	
3-state output enable time	t_{PZL}, t_{PZH}		$R_L = 1\text{ k}\Omega$	2.5 ± 0.2	15	—	9.4	15.9	ns
					50	—	12.3	18.8	
				3.3 ± 0.3	15	—	6.5	11.0	
					50	—	8.7	14.5	
				5.0 ± 0.5	15	—	4.5	7.6	
					50	—	6.2	9.6	
3-state output disable time	t_{PLZ}, t_{PHZ}		$R_L = 1\text{ k}\Omega$	2.5 ± 0.2	50	—	14.5	17.3	ns
				3.3 ± 0.3	50	—	10.9	14.0	
				5.0 ± 0.5	50	—	8.0	8.8	
Maximum clock frequency	f_{MAX}		—	2.5 ± 0.2	15	60	80	—	MHz
					50	50	65	—	
				3.3 ± 0.3	15	80	140	—	
					50	55	105	—	
				5.0 ± 0.5	15	130	185	—	
					50	85	140	—	
Output skew	t_{osLH}, t_{osHL}	(Note 1)	—	2.5 ± 0.2	50	—	—	2.0	ns
				3.3 ± 0.3	50	—	—	1.5	
				5.0 ± 0.5	50	—	—	1.0	
Input capacitance	C_{IN}		—			—	4	10	pF
Output capacitance	C_{OUT}		—			—	6	—	pF
Power dissipation capacitance	C_{PD}	(Note 2)	—			—	21	—	pF

Note 1: Parameter guaranteed by design. ($t_{osLH} = |t_{PLHM} - t_{PLHN}|$, $t_{osHL} = |t_{PHLM} - t_{PHLN}|$)

Note 2: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation.

$$I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/8 \text{ (per latch)}$$

And the total C_{PD} when n pcs. of latch operate can be gained by the following equation.

$$C_{PD} \text{ (total)} = 11 + 10 \times n$$

11.8. AC Characteristics
 (Unless otherwise specified, $T_a = -40$ to 85 °C, Input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Note	Test Condition	V_{CC} (V)	C_L (pF)	Min	Max	Unit
Propagation delay time (CK-Q)	t_{PLH}, t_{PHL}		—	2.5 ± 0.2	15	1.0	19.0	ns
					50	1.0	23.0	
				3.3 ± 0.3	15	1.0	15.0	
					50	1.0	18.5	
				5.0 ± 0.5	15	1.0	9.5	
					50	1.0	11.5	
3-state output enable time	t_{PZL}, t_{PZH}		$R_L = 1$ k Ω	2.5 ± 0.2	15	1.0	19.0	ns
					50	1.0	22.0	
				3.3 ± 0.3	15	1.0	13.0	
					50	1.0	16.5	
				5.0 ± 0.5	15	1.0	9.0	
					50	1.0	11.0	
3-state output disable time	t_{PLZ}, t_{PHZ}		$R_L = 1$ k Ω	2.5 ± 0.2	50	1.0	19.0	ns
				3.3 ± 0.3	50	1.0	16.0	
				5.0 ± 0.5	50	1.0	10.0	
Maximum clock frequency	f_{MAX}		—	2.5 ± 0.2	15	50	—	MHz
					50	40	—	
				3.3 ± 0.3	15	70	—	
					50	50	—	
				5.0 ± 0.5	15	110	—	
					50	75	—	
Output skew	$t_{oS LH}, t_{oS HL}$	(Note 1)	—	2.5 ± 0.2	50	—	2.0	ns
				3.3 ± 0.3	50	—	1.5	
				5.0 ± 0.5	50	—	1.0	
Input capacitance	C_{IN}		—			—	10	pF

Note 1: Parameter guaranteed by design. ($t_{oS LH} = |t_{PLHM} - t_{PLHN}|$, $t_{oS HL} = |t_{PHLM} - t_{PHLN}|$)

11.9. AC Characteristics
(Unless otherwise specified, $T_a = -40$ to 125 °C, Input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Note	Test Condition	V_{CC} (V)	C_L (pF)	Min	Max	Unit
Propagation delay time (CK-Q)	t_{PLH}, t_{PHL}		—	2.5 ± 0.2	15	1.0	21.0	ns
					50	1.0	25.5	
				3.3 ± 0.3	15	1.0	17.0	
					50	1.0	20.5	
				5.0 ± 0.5	15	1.0	11.0	
					50	1.0	13.0	
3-state output enable time	t_{PZL}, t_{PZH}		$R_L = 1$ k Ω	2.5 ± 0.2	15	1.0	21.5	ns
					50	1.0	24.5	
				3.3 ± 0.3	15	1.0	15.0	
					50	1.0	18.5	
				5.0 ± 0.5	15	1.0	10.0	
					50	1.0	12.0	
3-state output disable time	t_{PLZ}, t_{PHZ}		$R_L = 1$ k Ω	2.5 ± 0.2	50	1.0	20.5	ns
				3.3 ± 0.3	50	1.0	17.5	
				5.0 ± 0.5	50	1.0	11.0	
Maximum clock frequency	f_{MAX}		—	2.5 ± 0.2	15	40.0	—	MHz
					50	30.0	—	
				3.3 ± 0.3	15	60.0	—	
					50	40.0	—	
				5.0 ± 0.5	15	100.0	—	
					50	65.0	—	
Output skew	$t_{oS LH}, t_{oS HL}$	(Note 1)	—	2.5 ± 0.2	50	—	2.0	ns
				3.3 ± 0.3	50	—	1.5	
				5.0 ± 0.5	50	—	1.0	
Input capacitance	C_{IN}		—			—	10	pF

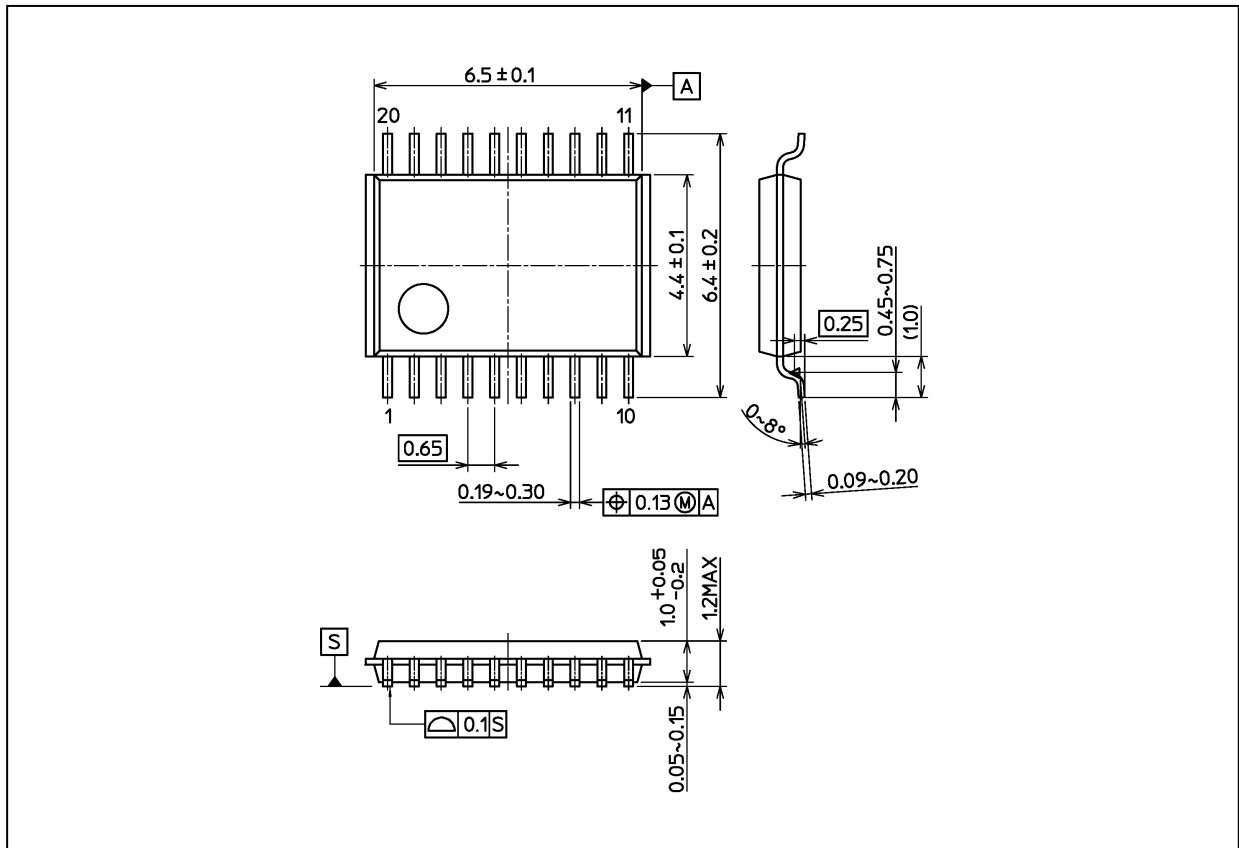
Note 1: Parameter guaranteed by design. ($t_{oS LH} = |t_{PLHM} - t_{PLHN}|$, $t_{oS HL} = |t_{PHLM} - t_{PHLN}|$)

11.10. Noise Characteristics (Unless otherwise specified, $T_a = 25$ °C, Input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Typ.	Max	Unit
Quiet output maximum dynamic V_{OL}	V_{OLP}	$C_L = 50$ pF	3.3	0.3	—	V
			5.0	0.7	—	
Quiet output minimum dynamic V_{OL}	V_{OLV}	$C_L = 50$ pF	3.3	-0.1	—	V
			5.0	-0.4	—	
Minimum high-level dynamic input voltage	V_{IHD}	$C_L = 50$ pF	5.0	—	3.5	V
Maximum low-level dynamic input voltage	V_{ILD}	$C_L = 50$ pF	5.0	—	1.5	V

Package Dimensions

Unit: mm



Weight: 0.071 g (typ.)

Package Name(s)
Nickname: TSSOP20B

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