

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74VHC9273P, TC74VHC9273FK

Octal D-Type Flip Flop with Clear

The TC74VHC9273 is an advanced high speed CMOS OCTAL D-TYPE FLIP FLOP fabricated with silicon gate C²MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

Information signals applied to D inputs are transferred to the Q outputs on the positive going edge of the clock pulse.

When the $\overline{\text{CLR}}$ input is held "L", the Q outputs are at a low logic level independent of the other inputs.

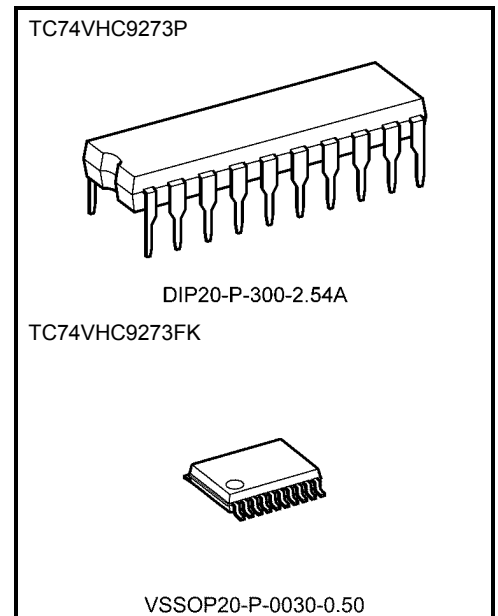
The $\overline{\text{CLR}}$ input and CK input have hysteresis between the positive-going and negative-going thresholds. Thus the TC74VHC9273 is capable of squaring up transitions of slowly changing input signals and provides an improved noise immunity.

It is easy to wire on the board because Input terminals are at the opposite side of Output terminals.

An input protection circuit ensures that 0 to 5.5 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

- High speed: $f_{\text{max}} = 195 \text{ MHz (typ.)}$ at $V_{\text{CC}} = 5 \text{ V}$
- Low power dissipation: $I_{\text{CC}} = 4 \mu\text{A (max)}$ at $T_a = 25^\circ\text{C}$
- Power down protection is provided on all inputs.
- Balanced propagation delays: $t_{\text{pLH}} \approx t_{\text{pHL}}$
- Wide operating voltage range: $V_{\text{CC (opr)}} = 2 \text{ to } 5.5 \text{ V}$
- Function compatible with 74VHC273
- Input terminals are at the opposite side of Output terminals



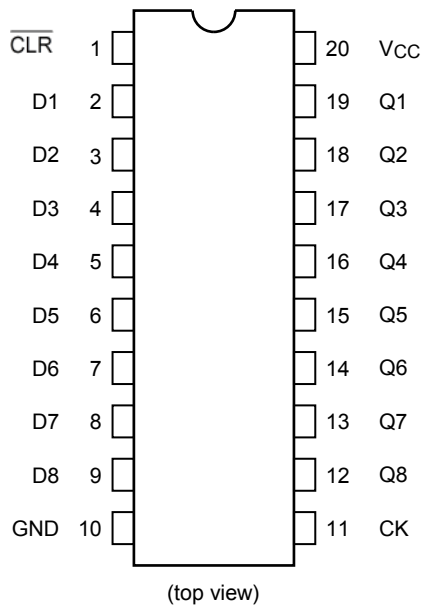
Weight

DIP20-P-300-2.54A : 1.30 g (typ.)

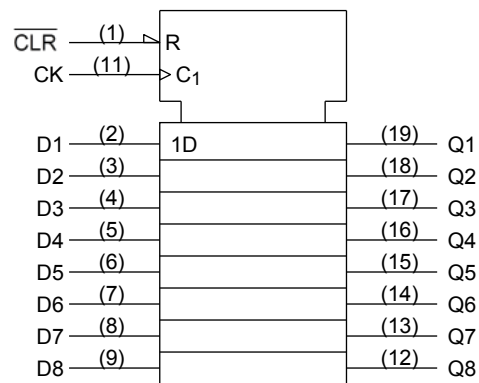
VSSOP20-P-0030-0.50 : 0.03 g (typ.)

Start of commercial production
2008-10

Pin Assignment



IEC Logic Symbol

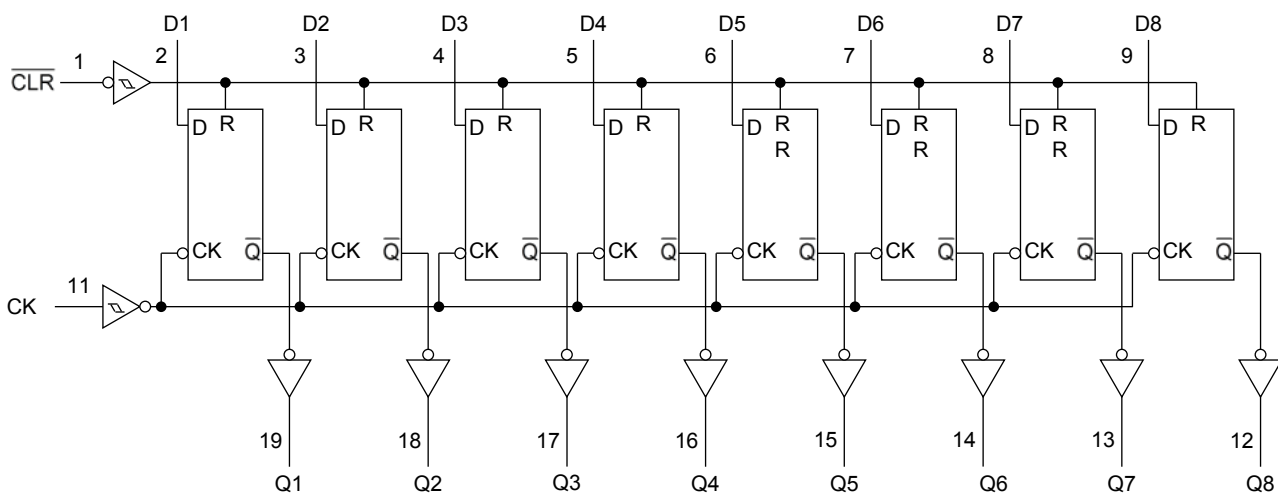


Truth Table

Inputs			Output	Function
$\overline{\text{CLR}}$	D	CK	Q	
L	X	X	L	Clear
H	L		L	—
H	H		H	—
H	X		Q_n	No Change

X: Don't care

System Diagram



Absolute Maximum Ratings (Note1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V _{CC}	-0.5 to 7.0	V
DC input voltage	V _{IN}	-0.5 to 7.0	V
DC output voltage	V _{OUT}	-0.5 to V _{CC} + 0.5	V
Input diode current	I _{IK}	-20	mA
Output diode current	I _{OK}	±20	mA
DC output current	I _{OUT}	±25	mA
DC V _{CC} /ground current	I _{CC}	±75	mA
Power dissipation	P _D	500 (DIP) (Note 2)/180(VSSOP)	mW
Storage temperature	T _{stg}	-65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: 500 mW in the range of T_a = -40 to 65°C. From T_a = 65 to 85°C a derating factor of -10 mW/°C shall be applied until 300 mW.

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V _{CC}	2.0 to 5.5	V
Input voltage	V _{IN}	0 to 5.5	V
Output voltage	V _{OUT}	0 to V _{CC}	V
Operating temperature	T _{opr}	-40 to 85	°C

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{CC} or GND.

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit	
				V _{CC} (V)	Min	Typ.	Max	Min		Max
Positive threshold voltage	V _P	—		3.0	—	—	2.20	—	2.20	V
				4.5	—	—	3.15	—	3.15	
				5.5	—	—	3.85	—	3.85	
Negative threshold voltage	V _N	—		3.0	0.90	—	—	0.90	—	V
				4.5	1.35	—	—	1.35	—	
				5.5	1.65	—	—	1.65	—	
Hysteresis voltage (CK, CLR)	V _H	—		3.0	0.30	—	1.20	0.30	1.20	V
				4.5	0.40	—	1.40	0.40	1.40	
				5.5	0.50	—	1.60	0.50	1.60	
High-level output voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -50 μA	2.0	1.9	2.0	—	1.9	—	V
				3.0	2.9	3.0	—	2.9	—	
				4.5	4.4	4.5	—	4.4	—	
			I _{OH} = -4 mA	3.0	2.58	—	—	2.48	—	
				4.5	3.94	—	—	3.80	—	
				I _{OH} = -8 mA	3.0	—	—	—	—	
Low-level output voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 50 μA	2.0	—	0.0	0.1	—	0.1	V
				3.0	—	0.0	0.1	—	0.1	
				4.5	—	0.0	0.1	—	0.1	
			I _{OL} = 4 mA	3.0	—	—	0.36	—	0.44	
				4.5	—	—	0.36	—	0.44	
				I _{OL} = 8 mA	3.0	—	—	—	—	
Input leakage current	I _{IN}	V _{IN} = 5.5 V or GND		0 to 5.5	—	—	±0.1	—	±1.0	μA
Quiescent supply current	I _{CC}	V _{IN} = V _{CC} or GND	5.5	—	—	4.0	—	40.0		

Timing Requirements (input: tr = tf = 3 ns)

Characteristics	Symbol	Test Condition		Ta = 25°C		Ta = -40 to 85°C	Unit	
				V _{CC} (V)	Typ.	Limit		Limit
Minimum pulse width (CK)	t _w (L)	—		3.3 ± 0.3	—	5.5	6.5	ns
	t _w (H)	—		5.0 ± 0.5	—	5.0	5.0	
Minimum pulse width (CLR)	t _w (L)	—		3.3 ± 0.3	—	5.0	6.0	ns
		—		5.0 ± 0.5	—	5.0	5.0	
Minimum set-up time	t _s	—		3.3 ± 0.3	—	6.0	7.0	ns
		—		5.0 ± 0.5	—	4.5	4.5	
Minimum hold time	t _h	—		3.3 ± 0.3	—	1.0	1.0	ns
		—		5.0 ± 0.5	—	1.0	1.0	
Minimum removal time (CLR)	t _{rem}	—		3.3 ± 0.3	—	2.5	2.5	ns
		—		5.0 ± 0.5	—	2.0	2.0	

AC Characteristics (input: $t_r = t_f = 3 \text{ ns}$)

Characteristics	Symbol	Test Condition	Ta = 25°C			Ta = -40 to 85°C		Unit		
			VCC (V)	CL (pF)	Min	Typ.	Max		Min	Max
Propagation delay time (CK-Q)	t_{pLH} t_{pHL}	—	3.3 ± 0.3	15	—	5.7	11.8	1.0	13.4	ns
				50	—	8.7	18.4	1.0	20.9	
			5.0 ± 0.5	15	—	4.2	7.7	1.0	8.8	
				50	—	6.5	12.1	1.0	13.8	
Propagation delay time (CLR-Q)	t_{pHL}	—	3.3 ± 0.3	15	—	5.9	12.3	1.0	14.0	ns
				50	—	8.6	18.0	1.0	20.6	
			5.0 ± 0.5	15	—	4.3	8.0	1.0	9.1	
				50	—	6.5	11.9	1.0	13.6	
Maximum clock frequency	f_{max}	—	3.3 ± 0.3	15	85	140	—	75	—	MHz
				50	50	75	—	45	—	
			5.0 ± 0.5	15	130	195	—	115	—	
				50	80	100	—	70	—	
Output to output skew	t_{osLH} t_{osHL}	(Note 1)	3.3 ± 0.3	50	—	—	1.5	—	1.5	ns
			5.0 ± 0.5	50	—	—	1.0	—	1.0	
Input capacitance	C_{IN}	—	—	—	4	10	—	10	pF	
Power dissipation capacitance	CPD	(Note 2)	—	—	11	—	—	—	pF	

Note 1: Parameter guaranteed by design.

$$t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|$$

Note 2: CPD is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

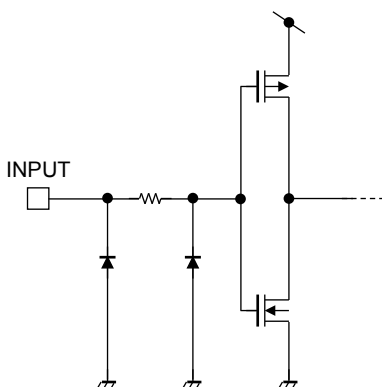
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = CPD \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per bit)}$$

And the total CPD when n pcs. of flip flop operate can be calculated by the following equation:

$$CPD \text{ (total)} = 7 + 4 \cdot n$$

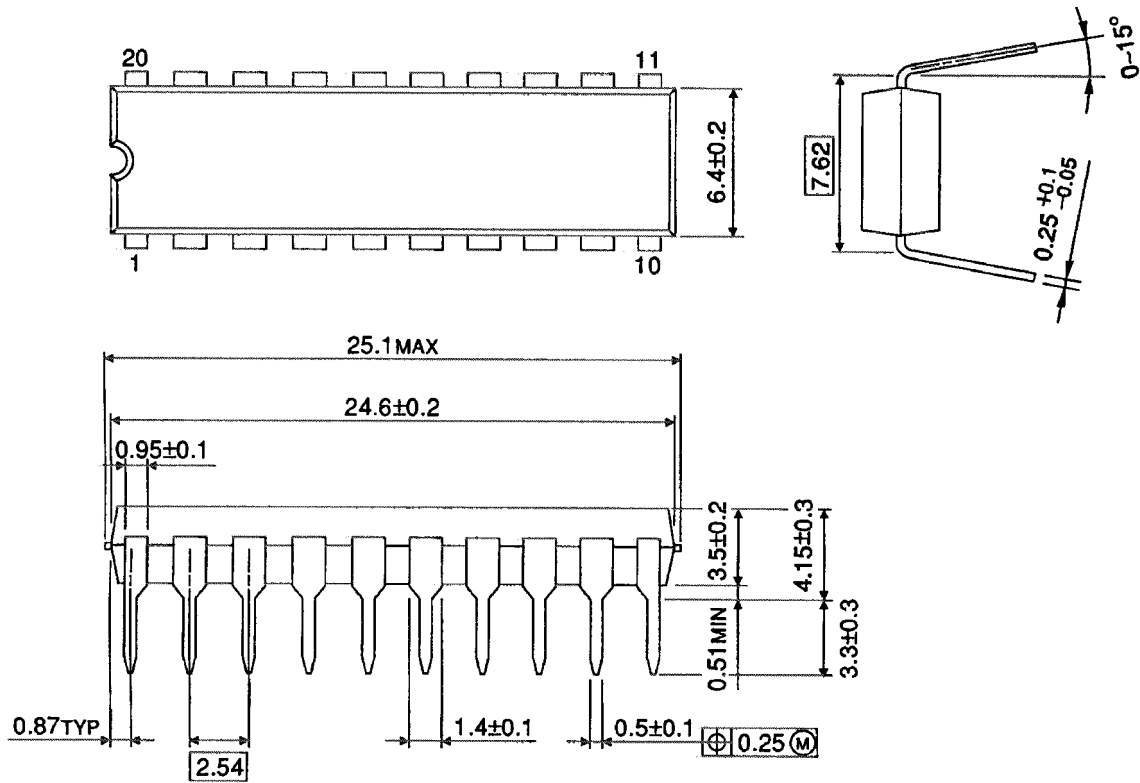
Input Equivalent Circuit



Package Dimensions

DIP20-P-300-2.54A

Unit : mm

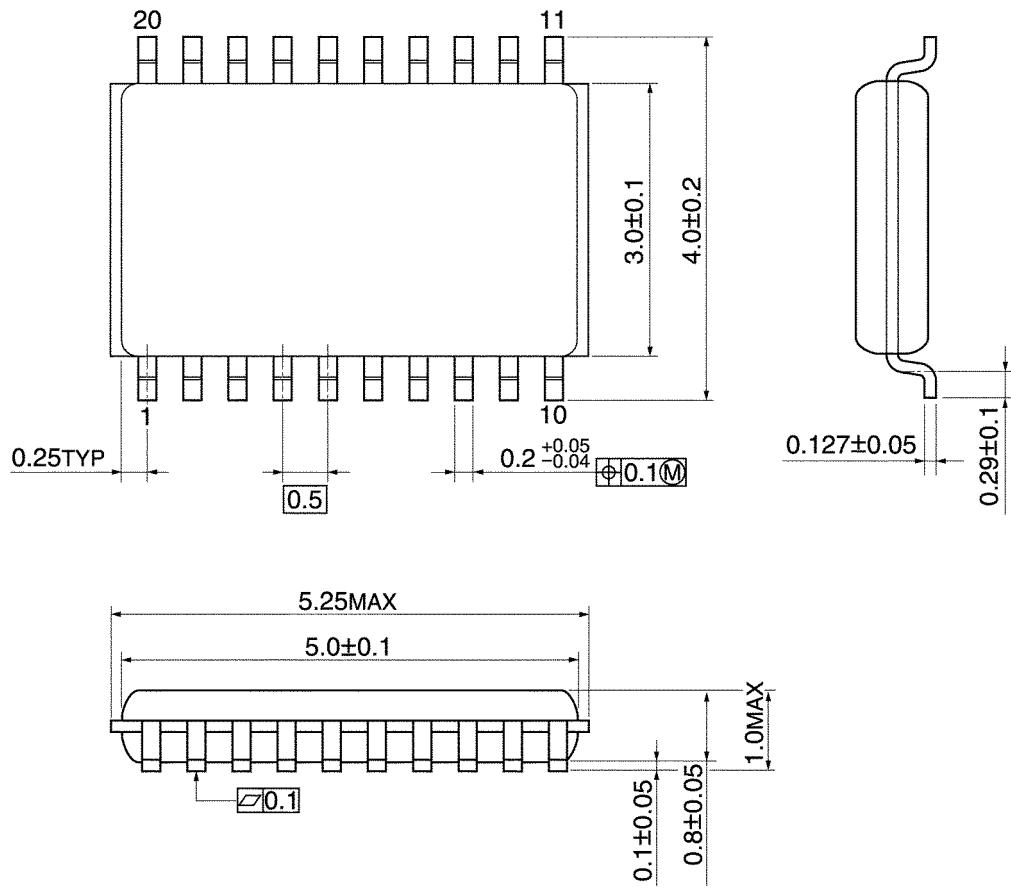


Weight: 1.30 g (typ.)

Package Dimensions

VSSOP20-P-0030-0.50

Unit: mm



Weight: 0.03 g (typ.)

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