TCK321G, TCK322G, TCK323G Application note / EVK user's guide

Contents

1. Introduction

The TCK32 series is 36V high voltage Power Multiplexer that is capable of switching outputs the dual power supply at safety. This product is not only switching by external signal, but also automatically switching that depends on input voltage by setting priority order in advance. Therefore this device operates in a stand-alone. In addition several functions (under voltage lock out, over voltage lock out, reverse current protection, rush current protection and thermal shut down function) for safety are built in. This device is available in small package WCSP16C. Thus it is ideal for portable applications that require high-density board assembly such as mobile phone and tablet PC.

Table 1-1 TCK32 series line up

Part number	package	VIN	IOUT	OVLO level	Input priority	Flag Operation	
						Monitored Input	Active Indication Level
TCK321G	WCSP16C	36V	2A	12.0V	VINA	VINA	Low
TCK322G				15.0V	VINA	VINA	Low
TCK323G				15.0V	VINA	VINB	Low

2. Application block diagram

Fugure2-1 shows charging block diagram with plural input system for mobile application. In this case, requires a switch to select either. TCK321/2/3G is valid as the switch.

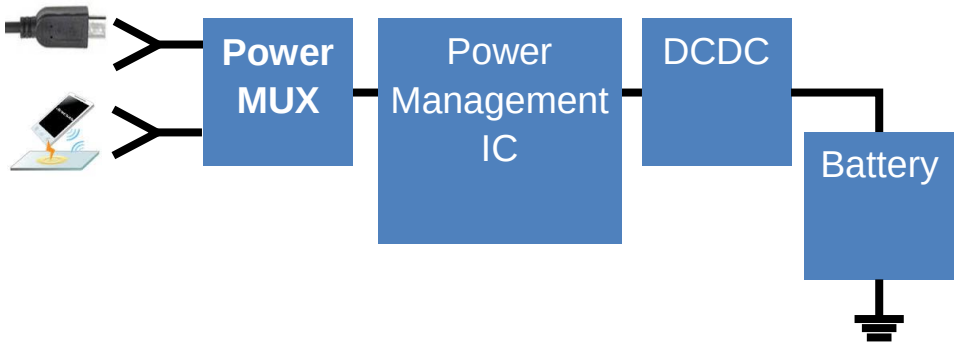


Figure 2-1 charging block diagram

3. Charging circuit with Power Multiplexer

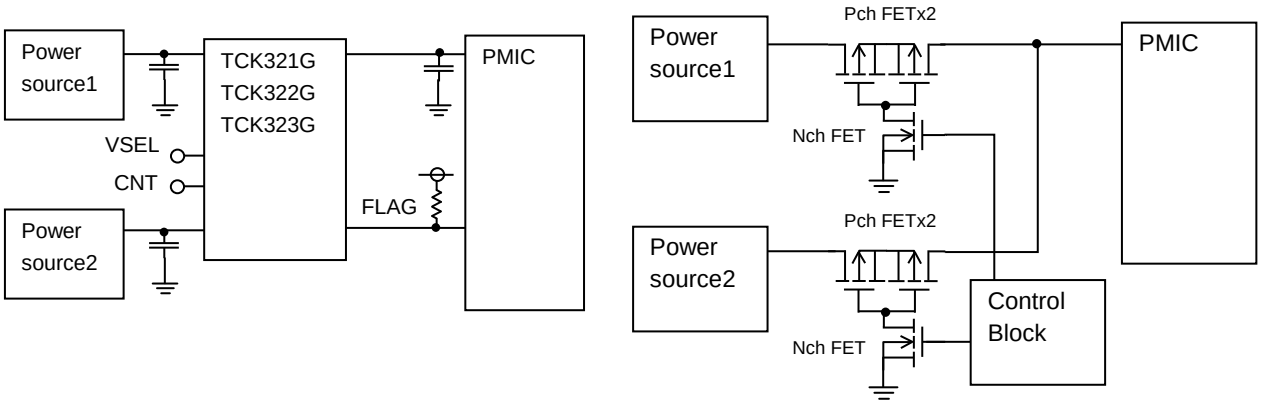
This section describes valid to use TCK321/2/3G solution. Compare to discrete solution. TCK321/2/3G is a one-chip solution. It can be easily design due to without external signal and additional components compare to discrete solution. Table 3-1 shows comparison table.

Table 3.1 Comparison for dual input solution

		TCK321/2/3G	Discrete solution (Pch FET×4 + Nch FET×2)*
Reference fig.		Figure 3-1	Figure 3-2
Output range		2.9V to 15V	1.8V to 12V (depend on FET)
Output current (DC)		2A	4A (depend on FET)
Useful	**Stand alone (Auto selection mode)**	OK	N/A
	Control by external signal	OK	OK
	Status FLAG output	OK	N/A
Function	**Over voltage lock out**	Built in	N/A
	Under voltage lock out	Built in	N/A
	Auto selection mode	Built in	N/A
	Thermal shut down	Built in	N/A
Power dissipation		Low	Very Low
ESD protection		High	Low
Mount area		Small	Large

This solution is example that consisted of following products.

Pch FET SSM6P49NU, Nch FET SSM6N15AFE



b) TCK321/2/3G solution

a) Discrete solution

Figure 3-1 block diagram for charge application

4. Main characteristics

4-1 OVLO (Over voltage lock out)

When an over voltage exceeding the OVLO detection voltage from the power supply during operation, main switch is OFF to protect system. OVLO state is released when the voltage fall to the prescribed voltage.

Conditions : CIN=1μF, CL=1μF, RL=50Ω

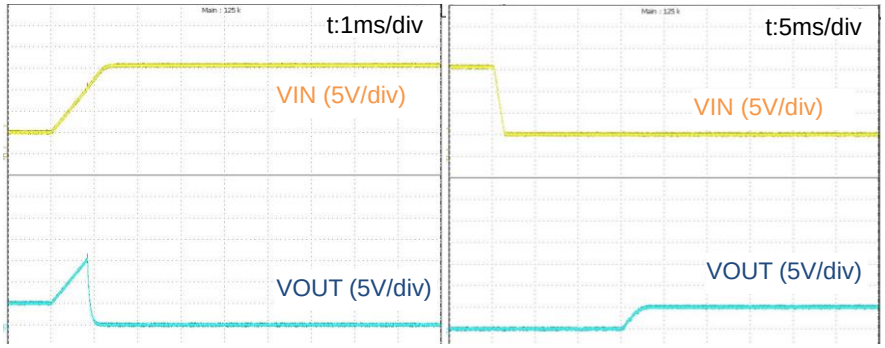


Figure 4-1 OVLO waveform (OVLO=15.0V typ.)

4-2 UVLO (Under voltage lock out)

When input voltage drops under UVLO detection voltage during operation, output is shutdown to prevent malfunction. UVLO state is released when the voltage rises more than the prescribed voltage.

Conditions : CIN=CL=1μF, RL=50Ω

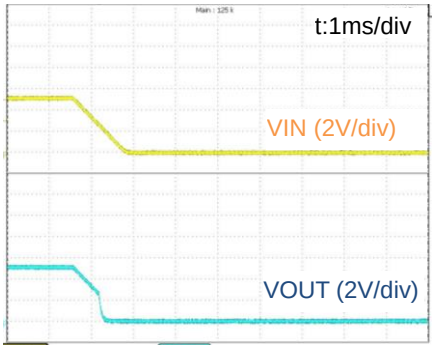


Figure 4-2 UVLO waveform (UVLO=2.9V typ.)

4-2 tHD (hold time) / Inrush current reducing

tHD is the OFF time which is provided to block irregular voltage from input voltage such as chattering. When detecting an input voltage in the between OVLO and UVLO, the internal FETs are turned on after a specified time.

ICs feature a soft start function. It is possible to establish a rise time that is not dependent on the input voltage.

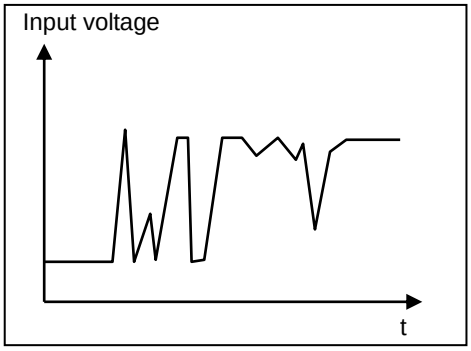


Figure 4-3 rising edge of switching in chattering input

Conditions : CIN=1μF, CL=1μF, RL=50Ω

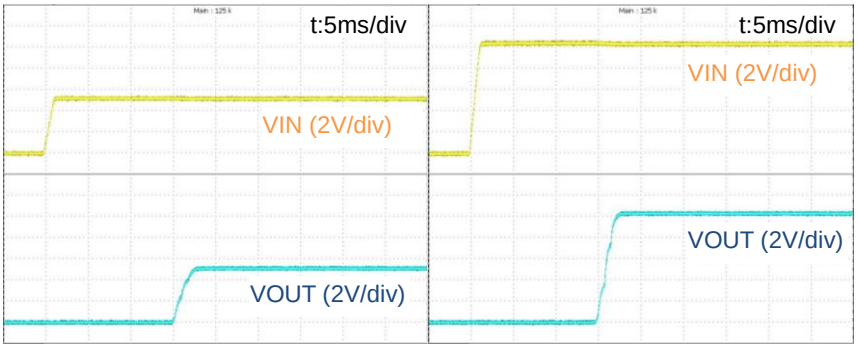


Figure 4-4 tHD/tr timing chart

Conditions : VIN=5V, CIN=1μF, CL=1μF, RL=50Ω

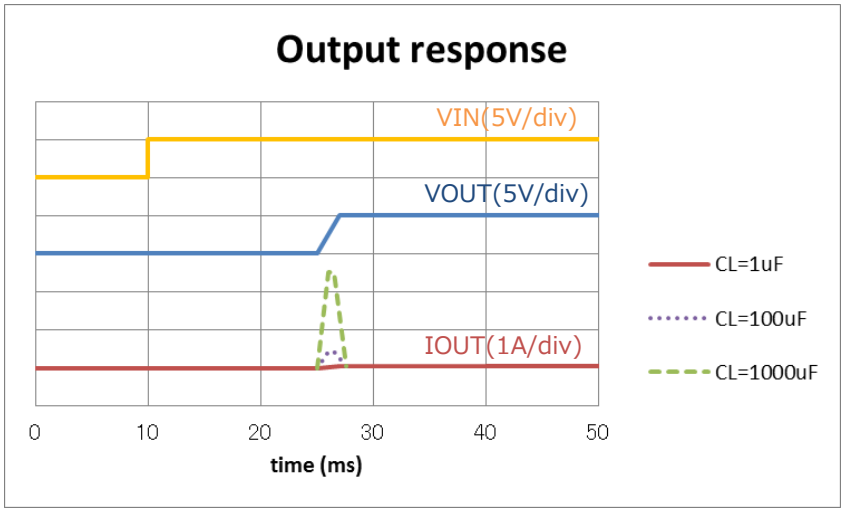


Figure 4-5 Output response

4-3 Auto selection mode

Auto select mode is a function that IC outputs regular input voltage automatically after judging whether a regular voltage of VINA or VINB. When regular voltages are input to VINA and VINB at the same time, IC outputs VINA voltage preferentially. FLAG signal is output the Low level VINA or VINB is selected. The behavior is different each product.

■TCK321/2G (FLAG outputs low level when VINA is selected)

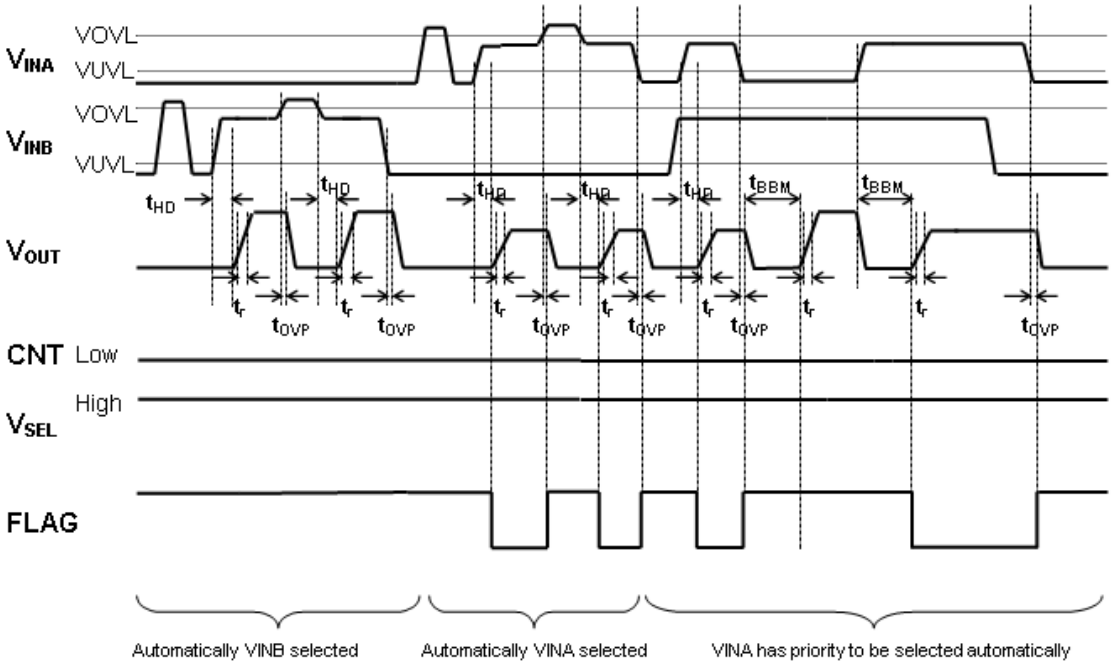


Figure 4-6 TCK321/2G timing chart in auto selection mode

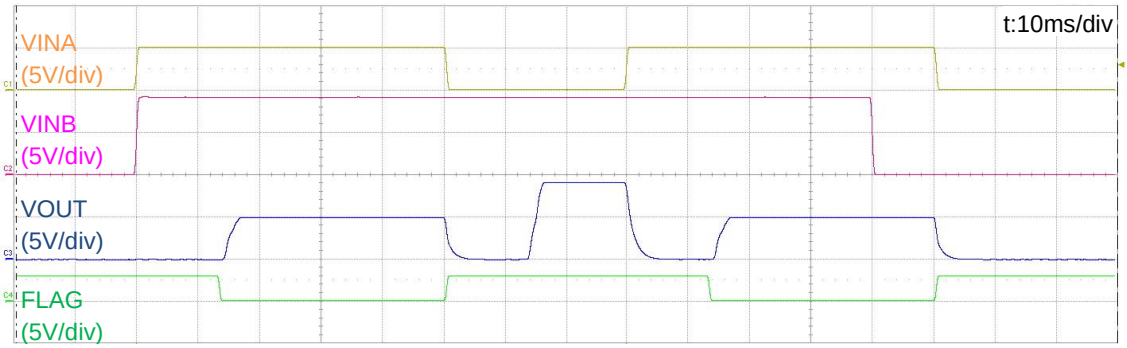


Figure 4-7 VINA has priority to be selected automatically

■TCK323G (FLAG outputs low level when VINB is selected)

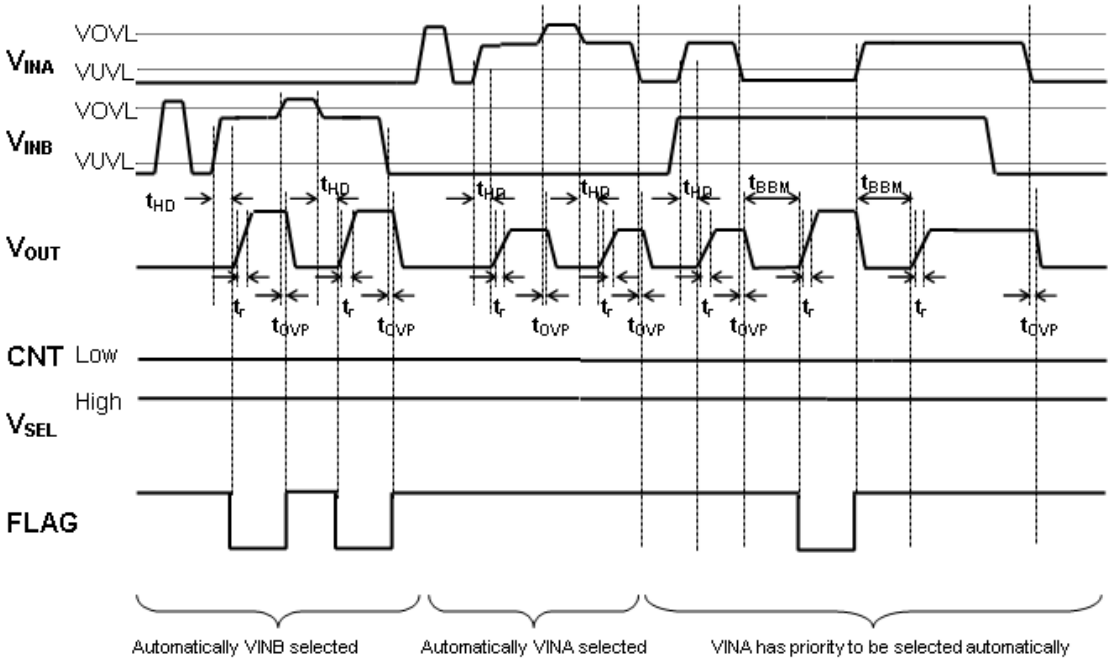


Figure 4-8 TCK323G timing chart in auto selection mode

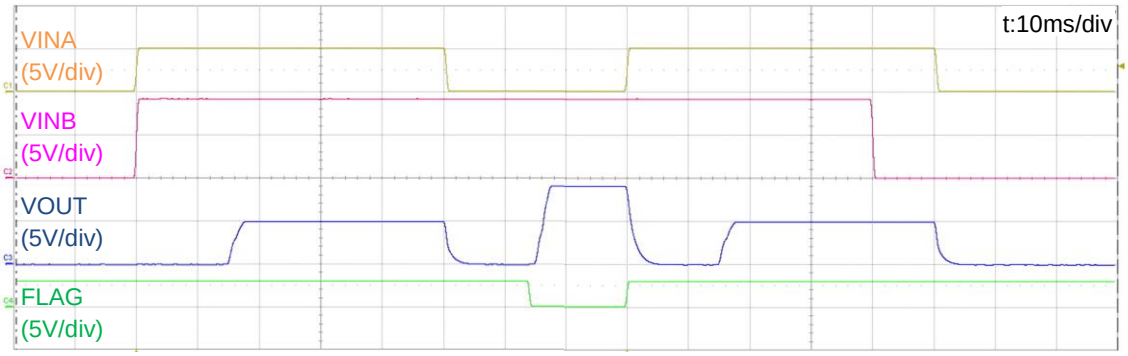


Figure 4-9 VINA has priority to be selected automatically

4-4 Manual selection mode

Manual select mode is a function that is selected by VSEL to output voltage.

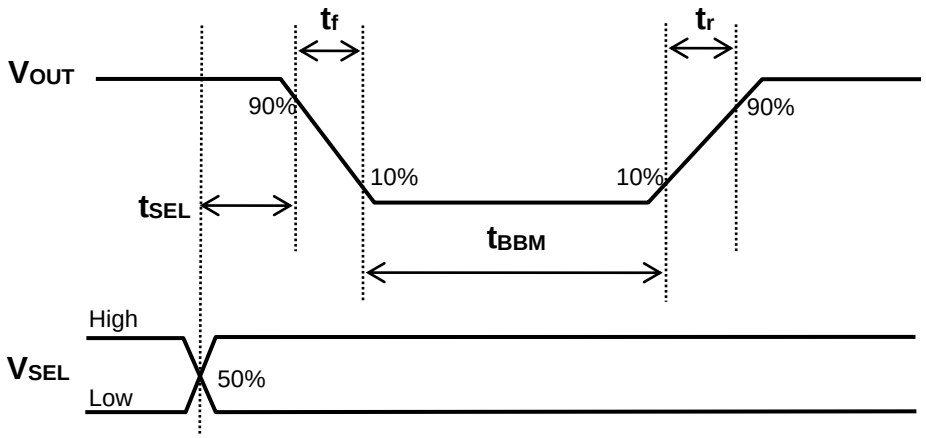


Figure 4-10 TCK321/2/3G timing chart in manual selection mode

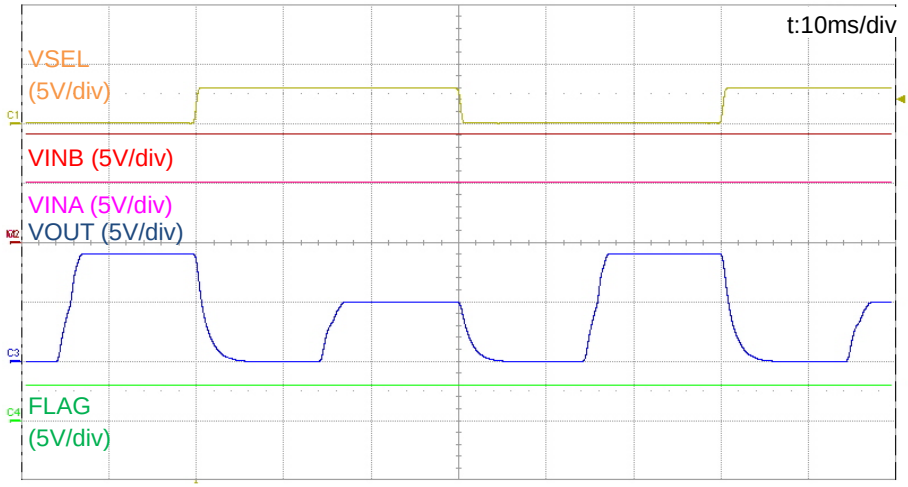


Figure 4-11 Manual selection mode

4-5 On resistance (Ron)

Figure4-12 shows a test result of On resistance. It effects on the power loss of the device and output voltage.

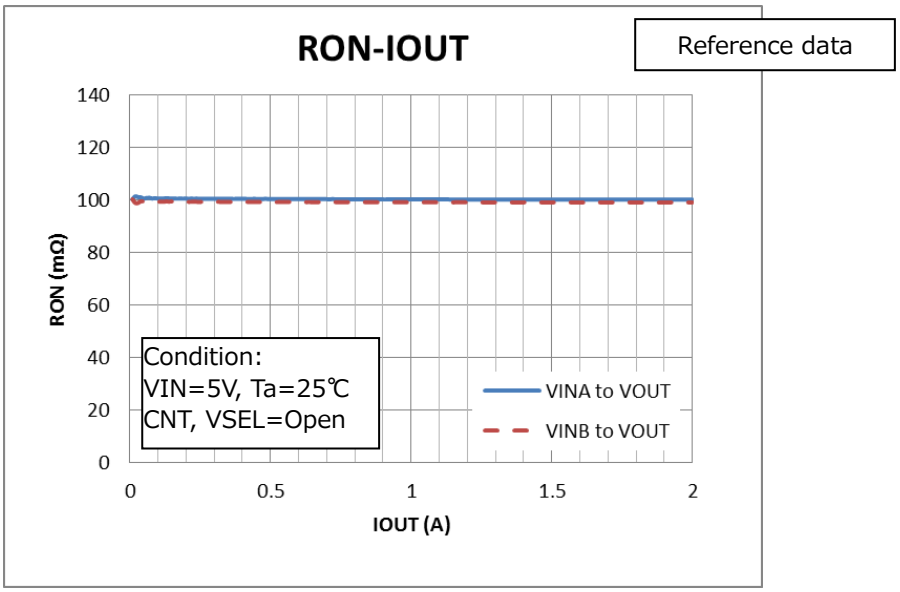


Figure 4-12 TCK321/2/3G RON-IOUT example

5. Evaluation board

The TCK321/2/3G EVALUATION KIT (EVK) helps designers evaluate the performance of the TCK32 series. Passive components and jumper are included in the EVK to evaluate easily. For the specification of the TCK321/2/3G, it is described in the data sheet. Please refer to it in conjunction with user guide.

Usage Precautions

・The input voltage, output voltage, output current and temperature conditions should be considered when selecting capacitors, inductors and resistors. These components should be evaluated on an actual system prototype for best selection.

• Parts of this product in the surrounding are examples of the representative, and the supply might become impossible. Please confirm latest information when using it.

Safety Precautions

・Do not touch the components and the device while the power is supplied. Contact to it may result in a burn or electrical shock.

・Do not touch the lead tips of a device. Some devices have leads with sharp tips. Contact to sharp tips may result in a puncture wound.

5-1 Schematic and BOM list

The schematic, Board Specification and BOM list for this EVK are shown in Fugure5-1, Table5-2 and Table5-1. Please refer to 5-2. SET UP for pin connection.

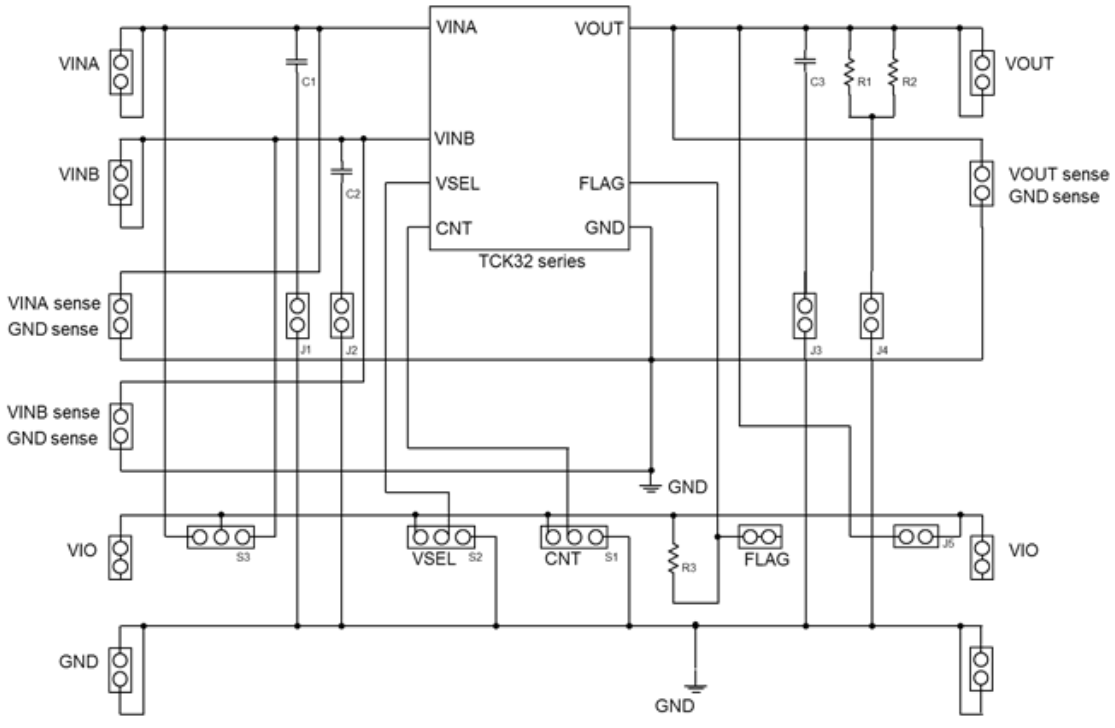


Figure 5-1 TCK321/2/3G EVK Schematic

Table 5-1 Board Specification

Content	Specification
Board size	45.72 x 66.04 mm (17 x 26 inch), t:1.6 mm
Copper foil	Double-sided board (18μm)
Quality of the material	Glass epoxy (FR-4)

Table 5-2 BOM list

Reference design	Value	Description	Size
C1, C2	1μF	Capacitor, 50V	3.2 x 1.6 mm
C3	1μF	Capacitor, 16V	1.6 x 0.8 mm
R1, R2	100Ω	Resistor, 5% 1/3W	3.2 x 1.6 mm
R3	10kΩ	Resistor, 1% 1/10W	1.6 x 0.8 mm
VINA/B, VOUT, GND, VIO, FLAG	-	Terminal, 2pin	-
VINA/B sense VOUT sense, GND sense	-	Terminal, 1pin	-
J1 to J5	-	Jumper, 2pin	2.54mm pitch
S1 to S3	-	Jumper, 3pin	2.54mm pitch
U1	-	IC, (TCK321/2/3G)	WCSP16 package
NA	NA	Shorting jumper (cap)	2.54mm pitch

5-2 Set up

This section describes how to properly set up and handling the jumper on the EVK. Please refer to the data sheet for test conditions.

INPUT (VINA, VINB)

VINA and VINB terminal are the input source connection. Connect the positive connection to the VINA or VINB terminal and the negative connection to the GND.

OUTPUT (VOUT)

VOUT terminal is the output connection of the EVK. Connect the positive connection of the load to the VOUT terminal and the negative connection to the GND terminal.

OUTPUT (FLAG)

FLAG terminal is the output connection to output flag signal depend on VIN level. FLAG terminal is pulled up to the VIO through R3.

VINA sense, VINB sense, VOUT sense and GND sense

These four terminals are used to measure the input or output voltage accurately by correcting the drop voltage of parasitic resistor. When the on resistance from VINA to VOUT is measured, it is calculated measuring the potential difference between VINA and VOUT sense terminal without influence of parasitic resistant.

S1 (CNT)

S1 terminal is used to select the input voltage of CNT. CNT pin in the center of S1 is connected to the device. Hi pin on the left side of S1 is connected to VIO terminal. Lo pin on the right side of S1 is connected to GND. Place a shorting jumper across Hi or Lo pin and CNT pin of S1 to select the operating state. Also, it is available even if CNT pin is left floating because it is internally connected to GND (Pull-down). In addition, it is possible to control operation by connecting CNT pin and a control signal source.

S2 (VSEL)

S2 terminal is used to select the input voltage of VSEL. VSEL pin on the center of S2 connected to the device. Hi pin on the left side of S2 is connected to VIO. Lo pin on the right side of S2 is connected to GND. Place a shorting jumper across the Hi or Lo pin and VSEL pin of S2 to select the operating state. Also, it is available even if VSEL pin is left floating because it is internally connected to voltage generator (Pull-up). In addition, it is possible to control operation by connecting VSEL pin and a control signal source.

VIO

VIO terminal is used to set the pull-up voltage of CNT, VSEL, and FLAG. The pull-up voltage is set to use an external power source. Or set to the same potential as VINA, VINB, or VOUT by shorting S3 or J5. VIO terminal is connected to Hi pin of S1to S2, a pin on the center of S3 and R3.

6. Operation Test

6-1 Impedance test (Ron)

This section describes RON measurement. Figure 6-1 shows a test setup for measuring on resistance. On resistance can be calculated IOUT and measurement result of the potential difference between VIN and VOUT sense. Test result of RON is showed at Figure 4-16.

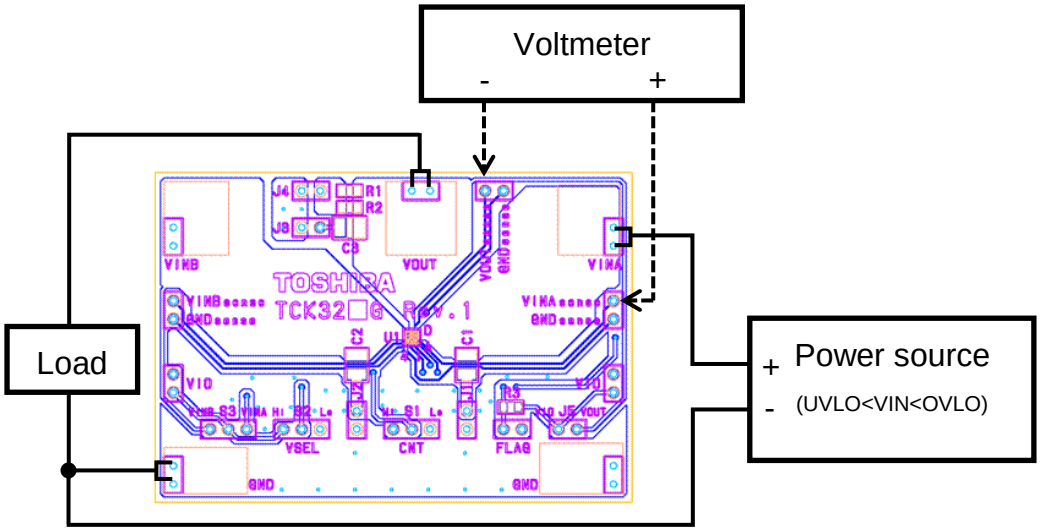


Figure 6-1 test circuit for RON

6-2 Output response (Auto select mode)

This section describes output response evaluation. TCK321/2/3G is equipped with two output response modes (manual select mode and Auto select mode). For details of each mode, please refer to 4.3 and 4.4. Figure 6-2 shows a test setup.

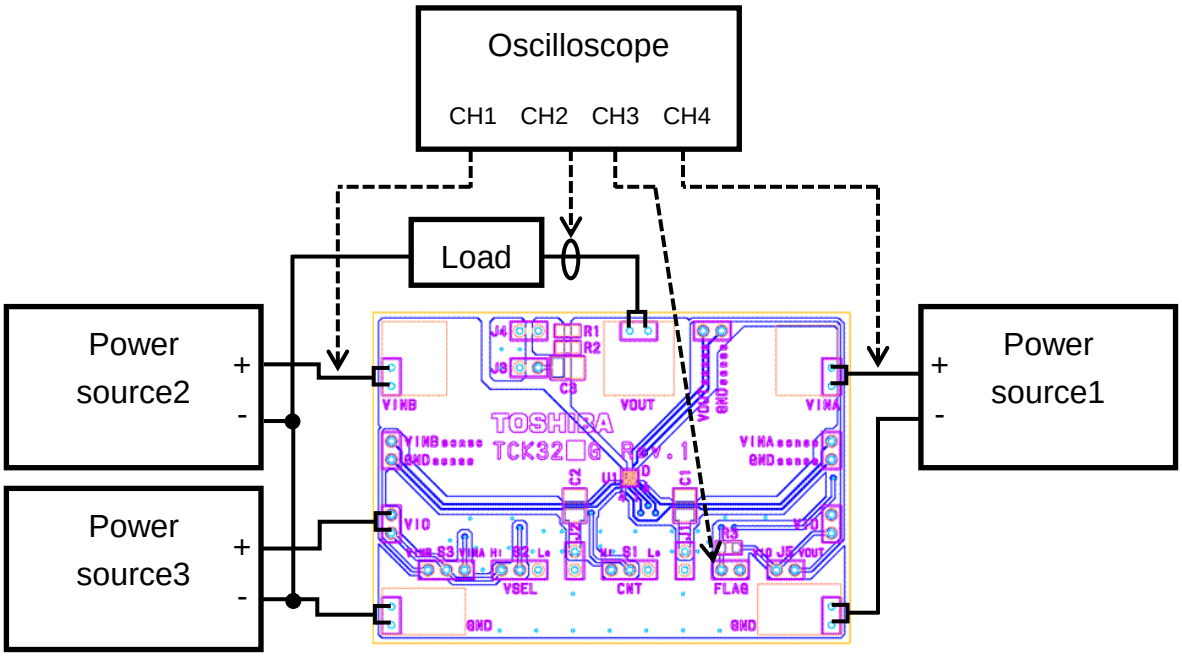


Figure 6-2 test circuit for Output response

7. Board Layout

This section provides the TCK321/2/3G EVK board layout.

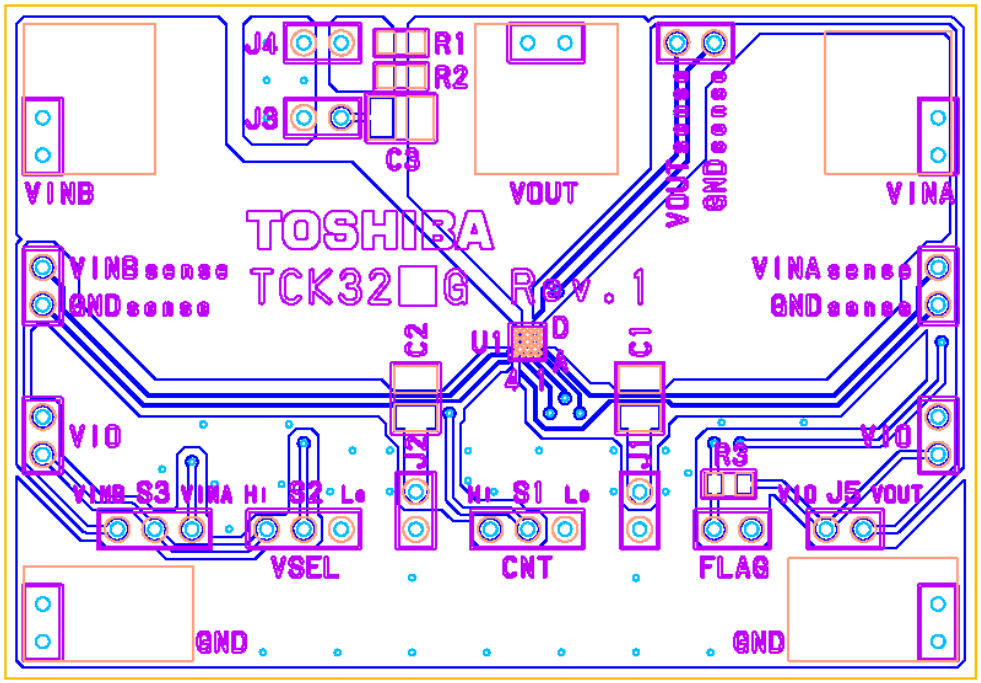


Figure 7-1 Top layer

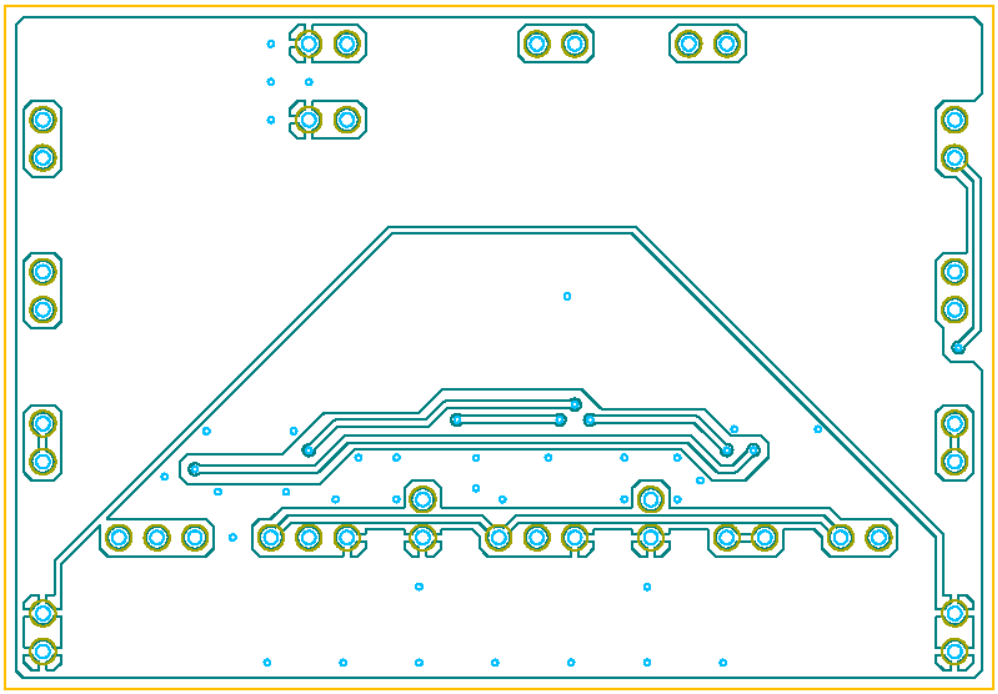


Figure 7-2 Bottom layer

PCB Layout Guideline

・All traces should be as short as possible to reduce influence of parasitic components.

・Capacitor of CIN and COUT must be placed as close as possible to the IC for stable power supply.

・It is possible to reduce the influence of parasitic and thermal impedance by taking widely IN, VOUT, and GND traces.

・It is possible to reduce the noise influence of the return current by dividing the power and small signal GND.

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