1. **General**

The DF2B7M3SL is a TVS diode (ESD protection diode) protects semiconductor devices used in mobile device interfaces and other applications to protect against static electricity and noise. The DF2B7M3SL provide to protect the latter part well by the low dynamic resistance, improve the system reliability level by the high $V_{ESD}$ performance. Furthermore, it is optimum for antenna application for the low capacitance performance.

The DF2B7M3SL is housed in an ultra-compact package (0.62 mm × 0.32 mm) to meet applications that require a small footprint.

2. **Applications**

Mobile Equipment
- Smartphones
- Tablets
- Notebook PCs
- Desktop PCs

Note: This product is designed for protection against electrostatic discharge (ESD) and is not intended for any other purpose, including, but not limited to, voltage regulation.

3. **Features**

1. Suitable for use with a 5 V signal line. ($V_{RWM} \leq 5.5 \text{ V}$)
2. Protects devices with its high ESD performance. ($V_{ESD} = \pm 12 \text{ kV (Contact), } V_{ESD} = \pm 15 \text{ kV (Air) @IEC61000-4-2}$)
3. Low dynamic resistance protects semiconductor devices from static electricity and noise. ($R_{DYN} = 0.7 \Omega \text{ (typ.)}$)
4. Compact package is suitable for use in high density board layouts such as in mobile devices. (0.62 mm × 0.32 mm size (Nickname: SL2))

4. **Packaging**
5. Example of Circuit Diagram

![Circuit Diagram]

6. Quick Reference Data

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Symbol</th>
<th>Note</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ.</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Working peak reverse voltage</td>
<td>(V_{RWM})</td>
<td>(Note 1)</td>
<td>(V_R = 0\ V, f = 1\ MHz)</td>
<td></td>
<td></td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>Total capacitance</td>
<td>(C_t)</td>
<td></td>
<td>(V_R = 0\ V, f = 5\ GHz)</td>
<td>0.1</td>
<td>0.2</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>Dynamic resistance</td>
<td>(R_{DYN})</td>
<td>(Note 2)</td>
<td></td>
<td>0.1</td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>Electrostatic discharge voltage</td>
<td>(V_{ESD})</td>
<td>(Note 3)</td>
<td></td>
<td>0</td>
<td>0.7</td>
<td>12</td>
<td>kV</td>
</tr>
</tbody>
</table>

Note 1: Recommended operating condition.
Note 2: TLP parameters: \(Z_0 = 50\ Ω\), \(t_p = 100\ ns\), \(t_r = 300\ ps\), averaging window: \(t_1 = 30\ ns\) to \(t_2 = 60\ ns\), extraction of dynamic resistance using least squares fit of TLP characteristics between \(I_{PP1} = 8\ A\) and \(I_{PP2} = 16\ A\).
Note 3: Criterion: No damage to devices.
6.1. ESD Clamp Waveform (Note)

![ESD Clamp Waveform](image)

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

6.2. Clamp Voltage - Peak Pulse Current ($V_C - I_{PP}$) (Note)

![Clamp Voltage - Peak Pulse Current](image)

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.
7. Absolute Maximum Ratings (Note) (Unless otherwise specified, $T_a = 25^\circ C$)

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Symbol</th>
<th>Note</th>
<th>Rating</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Electrostatic discharge voltage (IEC61000-4-2) (Contact)</td>
<td>$V_{\text{ESD}}$</td>
<td>(Note 1)</td>
<td>±12</td>
<td>kV</td>
</tr>
<tr>
<td>Electrostatic discharge voltage (IEC61000-4-2) (Air)</td>
<td>$P_{\text{PK}}$</td>
<td></td>
<td>±15</td>
<td></td>
</tr>
<tr>
<td>Peak pulse power (tp = 8/20 µs)</td>
<td>$I_{\text{PP}}$</td>
<td>(Note 2)</td>
<td>50</td>
<td>W</td>
</tr>
<tr>
<td>Peak pulse current (tp = 8/20 µs)</td>
<td>$T_j$</td>
<td></td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>Storage temperature</td>
<td>$T_{\text{stg}}$</td>
<td></td>
<td>-55 to 150</td>
<td>°C</td>
</tr>
</tbody>
</table>

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: According to IEC61000-4-2.
Note 2: According to IEC61000-4-5.

8. Electrical Characteristics (Unless otherwise specified, $T_a = 25^\circ C$)

- $V_{\text{RWM}}$: Working peak reverse voltage
- $V_{\text{BR}}$: Reverse breakdown voltage
- $I_{\text{BR}}$: Reverse breakdown current
- $V_{\text{C}}$: Clamp voltage
- $I_{\text{PP}}$: Peak pulse current
- $R_{\text{DYN}}$: Dynamic resistance

![Fig. 8.1 Definitions of Electrical Characteristics](image)

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Symbol</th>
<th>Note</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ.</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Working peak reverse voltage</td>
<td>$V_{\text{RWM}}$</td>
<td>(Note 1)</td>
<td>$V_R = 0 \text{ V}, f = 1 \text{ MHz}$</td>
<td>—</td>
<td>—</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>Total capacitance</td>
<td>$C_t$</td>
<td></td>
<td>$V_R = 0 \text{ V}, f = 5 \text{ GHz}$</td>
<td>—</td>
<td>0.1</td>
<td>0.2</td>
<td>pF</td>
</tr>
<tr>
<td>Dynamic resistance</td>
<td>$R_{\text{DYN}}$</td>
<td>(Note 2)</td>
<td>$I_{\text{IR}} = 1 \text{ mA}$</td>
<td>6</td>
<td>11</td>
<td>—</td>
<td>V</td>
</tr>
<tr>
<td>Reverse breakdown voltage</td>
<td>$V_{\text{BR}}$</td>
<td></td>
<td>$V_{\text{RWM}} = 5.5 \text{ V}$</td>
<td>—</td>
<td>—</td>
<td>0.5</td>
<td>µA</td>
</tr>
<tr>
<td>Reverse current</td>
<td>$I_{\text{R}}$</td>
<td></td>
<td>$I_{\text{PP}} = 1 \text{ A}$</td>
<td>—</td>
<td>13</td>
<td>—</td>
<td>V</td>
</tr>
<tr>
<td>Clamp voltage</td>
<td>$V_{\text{C}}$</td>
<td>(Note 3)</td>
<td>$I_{\text{PP}} = 2.5 \text{ A}$</td>
<td>—</td>
<td>15.5</td>
<td>20</td>
<td></td>
</tr>
</tbody>
</table>

Note 1: Recommended operating condition.
Note 2: TLP parameters: $Z_0 = 50 \Omega$, tp = 100 ns, tr = 300 ps, averaging window: $t_1 = 30 \text{ ns to } t_2 = 60 \text{ ns}$, extraction of dynamic resistance using least squares fit of TLP characteristics between $I_{\text{PP1}} = 8 \text{ A}$ and $I_{\text{PP2}} = 16 \text{ A}$.
Note 3: Based on IEC61000-4-5 8/20 µs pulse.
9. Characteristics Curves (Note)

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.
10. Internal Circuit (Note)

![Internal Circuit Diagram]

1: Pin 1
2: Pin 2

Note: Connect Pin 2 to GND when using Pin 1 for I/O.
Connect Pin 1 to GND when using Pin 2 for I/O.

11. Marking (Top view)

![Marking Diagram]

Pin 1 mark

12. Land Pattern Dimensions (for reference only)

![Land Pattern Dimensions Diagram]

Unit: mm
Package Dimensions

Unit: mm

Weight: 0.2 mg (typ.)

Nickname: SL2

Package Name(s)

BOTTOM VIEW

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