Application Processor Lite *ApP Lite*

TZ1000 Series

Reference Manual

MCU Processor and core peripherals

Revision 1.2

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TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

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Preface

This document provides the specification for the MCU Processor and core peripherals designed for the TZ1000 Series.

Intended Audience

This document is intended for the following users.

Driver software developers.

System designers

Conventions in this document

- The following notational conventions apply to numbers:
  Hexadecimal number: 0xABC
  Decimal number: 123 or 0d123 (only. when it should be explicitly indicated that the number is decimal)
  Binary number: 0b111 (It is possible to omit the "0b" when the number of bit can be distinctly understood from a sentence.)
- Low active signals are indicated with a name suffixed with "_N".
- A signal is asserted when it goes to its active level while it is deasserted when it goes to its inactive level.
- A set of multiple signals may be referred to as [m:n].
  Example: S[3:0] indicates four signals, S3, S2, S1 and S0, collectively.
- In the text, register names are enclosed in brackets *[ ]*.
  Example: *[ABCD]*
- A set of multiple registers, fields or bits of the same type may be described collectively using "n".
  Example: *[XYZ1], [XYZ2], and [XYZ3] to [XYZn]*
  A range of register bits are referred to as [m:n].
  Example: [3:0] indicates a range from bit 3 to bit 0.
- Values set in registers are indicated using either a hexadecimal or binary number.
- Example: *[ABCD]*.EFG = 0x01 (hexadecimal), *[XYZn]*.VW = 1 (binary)
- Words and bytes are defined as follows:
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Register bit attributes are defined as follows:
  R: Read-only
  W: Write-only
  W1C: Clear by write of 1 (a write of "1" clears the corresponding bit to 0)
  W1S: Set by write of 1 (a write of "1" sets the corresponding bit to 1)
  R/W: Read/Write
  R/W0C: Read/Clear by write of 0
  R/W1C: Read/Clear by write of 1
  R/W1S: Read/Set by write of 1
  RS/WC: Set by read/Clear by write (set after a read and cleared after a data write)
- Registers only support word access unless otherwise specified.
- Any registers defined as Reserved in the text must not be rewritten. Also, any values read from such registers should not be used.
- Any bits for which default values are defined as "-" would return undefined values if read.
- When a data is written to a register containing both writable and read-only (R) bit fields, its default values should be written to read-only (R) bit fields. For any bit fields with default values defined as "-", refer to the definitions of the relevant register.
- Default values should be written to any reserved bit fields in a write-only register. For any bit fields with default values defined as "-", refer to the definitions of the relevant register.

1. Features

1.1. About the Cortex®-M4 processor and core peripherals

The Arm® Cortex®-M4 processor is a high performance 32-bit processor designed for the microcontroller market. It offers significant benefits to developers, including:

- -outstanding processing performance combined with fast interrupt handling
- -enhanced system debug with extensive breakpoint and trace capabilities
- -efficient processor core, system and memories
- -ultra-low power consumption with integrated sleep mode and an optional deep sleep mode
- -platform security robustness, with optional integrated *Memory Protection Unit* (MPU).

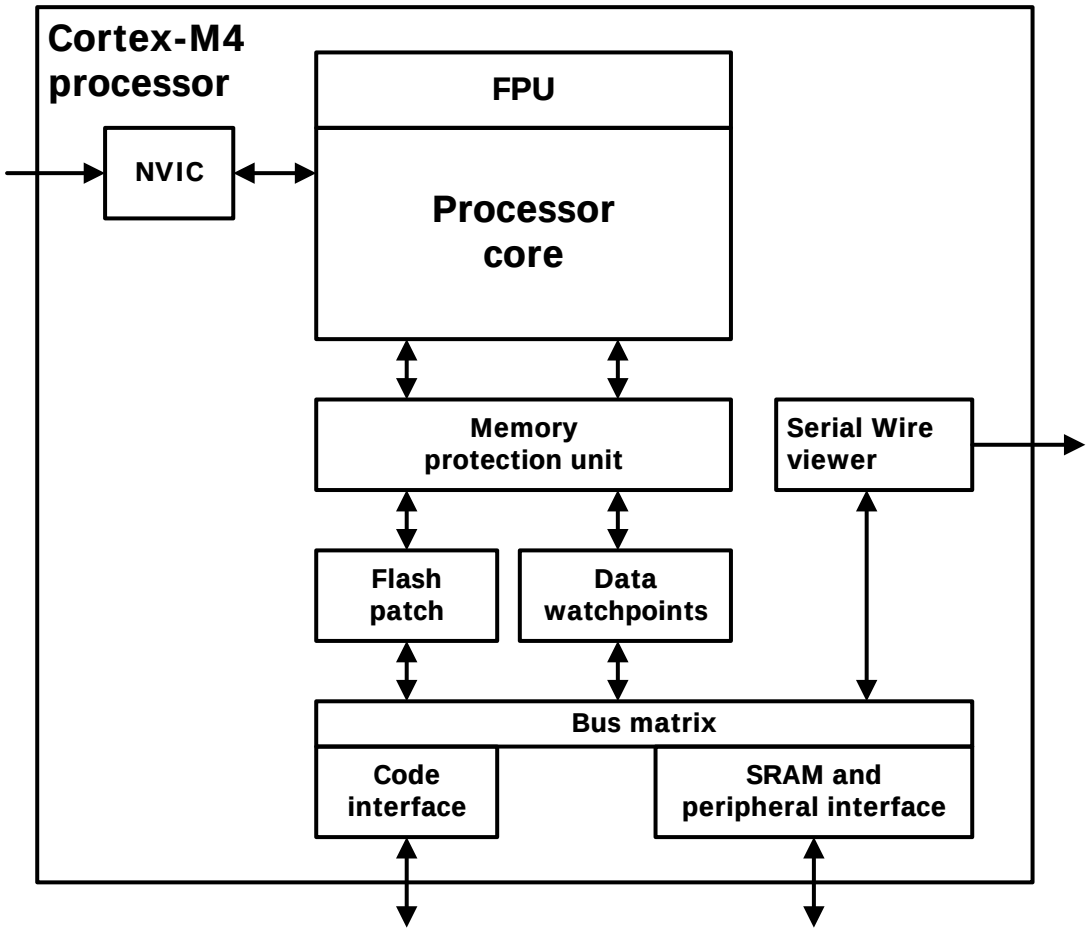

Figure 1.1 Cortex®-M4 implementation

The Cortex®-M4 processor is built on a high-performance processor core, with a 3-stage pipeline Harvard architecture, making it ideal for demanding embedded applications. The processor delivers exceptional power efficiency through an efficient instruction set and extensively optimized design, providing high-end processing hardware including optional IEEE754-compliant single-precision floating-point computation, a range of single-cycle and SIMD multiplication and multiply with accumulate capabilities, saturating arithmetic and dedicated hardware division.

To facilitate the design of cost-sensitive devices, the Cortex®-M4 processor implements tightly coupled system components that reduce processor area while significantly improving interrupt handling and system debug capabilities. The Cortex®-M4 processor implements a version of the Arm® Thumb® instruction set based on Thumb®-2 technology, ensuring high code density and reduced program memory requirements. The Cortex®-M4 instruction set provides the exceptional performance expected of a modern 32-bit architecture, with the high code density of 8-bit and 16-bit

microcontrollers.

The Cortex®-M4 processor closely integrates a configurable *Nested Vectored Interrupt Controller* (NVIC), to deliver industry-leading interrupt performance. The NVIC includes a *Non Maskable Interrupt* (NMI) that can provide up to 256 interrupt priority levels. The tight integration of the processor core and NVIC provides fast execution of *Interrupt Service Routines* (ISRs), dramatically reducing the interrupt latency. This is achieved through the hardware stacking of registers, and the ability to suspend load-multiple and store-multiple operations. Interrupt handlers do not require wrapping in assembler code, removing any code overhead from the ISRs. A tail-chain optimization also significantly reduces the overhead when switching from one ISR to another.

To optimize low-power designs, the NVIC integrates with the sleep modes, that includes an optional deep sleep function. This enables the entire device to be rapidly powered down while still retaining program state.

1.1.1. System-level interface

The Cortex®-M4 processor provides multiple interfaces using Arm® AMBA® technology to provide high speed, low latency memory accesses. It supports unaligned data accesses and implements atomic bit manipulation that enables faster peripheral controls, system spinlocks and thread-safe Boolean data handling.

The Cortex®-M4 processor has an optional *Memory Protection Unit* (MPU) that permits control of individual regions in memory, enabling applications to utilize multiple privilege levels, separating and protecting code, data and stack on a task-by-task basis. Such requirements are becoming critical in many embedded applications such as automotive.

1.1.2. Integrated configurable debug

The Cortex®-M4 processor can implement a complete hardware debug solution. This provides high system visibility of the processor and memory through either a traditional JTAG port or a 2-pin *Serial Wire Debug* (SWD) port that is ideal for microcontrollers and other small package devices.

For system trace the processor integrates an *Instrumentation Trace Macrocell* (ITM) alongside data watch points and a profiling unit. To enable simple and cost-effective profiling of the system events these generate, a *Serial Wire Viewer* (SWV) can export a stream of software-generated messages, data trace, and profiling information through a single pin.

The optional *Embedded Trace Macrocell*™ (ETM) delivers unrivalled instruction trace capture in an area far smaller than traditional trace units, enabling many low cost MCUs to implement full instruction trace for the first time.

The optional *Flash Patch and Breakpoint Unit* (FPB) provides up to eight hardware breakpoint comparators that debuggers can use. The comparators in the FPB also provide remap functions of up to eight words in the program code in the CODE memory region. This enables applications stored on a non-erasable, ROM-based microcontroller to be patched if a small programmable memory, for example flash, is available in the device. During initialization, the application in ROM detects, from the programmable memory, whether a patch is required. If a patch is required, the application programs the FPB to remap a number of addresses. When those addresses are accessed, the accesses are redirected to a remap table specified in the FPB configuration, which means the program in the non-modifiable ROM can be patched.

1.1.3. Cortex®-M4 processor features and benefits summary

- tight integration of system peripherals reduces area and development costs
- Thumb® instruction set combines high code density with 32-bit performance
- optional IEEE754-compliant single-precision FPU
- code-patch ability for ROM system updates
- power control optimization of system components
- integrated sleep modes for low power consumption
- fast code execution permits slower processor clock or increases sleep mode time
- hardware division and fast digital-signal-processing orientated multiply accumulate
- saturating arithmetic for signal processing
- deterministic, high-performance interrupt handling for time-critical applications
- optional *Memory Protection Unit* (MPU) for safety-critical applications
- extensive implementation-defined debug and trace capabilities:

Serial Wire Debug and Serial Wire Trace reduce the number of pins required for debugging, tracing, and code profiling.

1.1.4. Cortex®-M4 core peripherals

These are:

Nested Vectored Interrupt Controller

The NVIC is an embedded interrupt controller that supports low latency interrupt processing.

System Control Block

The *System Control Block* (SCB) is the programmers model interface to the processor. It provides system implementation information and system control, including configuration, control, and reporting of system exceptions.

System timer

The system timer, SysTick, is a 24-bit count-down timer. Use this as a Real Time Operating System (RTOS) tick timer or as a simple counter.

Memory Protection Unit

The *Memory Protection Unit* (MPU) improves system reliability by defining the memory attributes for different memory regions. It provides up to eight different regions, and an optional predefined background region.

Floating-point Unit

The *Floating-Point Unit* (FPU) provides IEEE754-compliant operations on single-precision, 32-bit, floating-point values.

2. Cortex®-M4 with FPU configuration options

Table 2.1 Cortex®-M4 with FPU configuration options

Configuration options	Values	Description
Number of interrupts	80	Specifies the number of user interrupts.
Interrupt priority width	3	Specifies the bits of interrupt priority. At 3, there are 8 levels of priority.
Inclusion of MPU	1	Specifies whether an MPU is present. Setting this parameter to 1 includes the MPU.
FPU present or not	1	Specifies whether a Floating Point Unit (FPU) is present. Setting this parameter to 1 includes the FPU.
Bit banding present or not	1	Specifies whether bit-banding is supported.
Constant AHB control information during wait-stated transfers	1	Specifies whether the external AHB-Lite buses maintain control information during wait stated transfers. 1 => This ensures that once transfers are issued during a wait-stated response they are never retracted or modified and the original transfer is honoured.
Debug support level	3	Specifies the level of debug support: 3 => Full debug with data matching. All debug functionality is present including data matching for watch point generation.
Trace support level	1	Specifies the level of trace support: 1 => Standard trace. ITM, TPIU, and DWT triggers and counters are present. ETM and HTM port are not present.
Reset all registers	1	Specifies whether all synchronous state or only architecturally required state is reset. 1 => resets all synchronous state.
JTAG-DP inclusion	1	Enables or disables the JTAG portion of the debug port. This switches between an SW-DP and an SWJ-DP. The default setting at 1, enables the JTAG portion, creating an SWJ-DP.
Architectural clock gating instantiated	1	Specifies whether architectural clock gates are included to minimize dynamic power dissipation.
WIC present or not	0	Specifies whether a WIC is present. Setting this parameter to 0 not includes the WIC.

3. Cortex®-M4 with FPU interrupts map

Table 3.1 Interrupt Request Signal Map

No.	Module	Description
0	gpio0	GPIO_0 Interrupt
1	gpio0	GPIO_1 Interrupt
2	gpio0	GPIO_2 Interrupt
3	gpio0	GPIO_3 Interrupt
4	gpio0	GPIO_4 Interrupt
5	gpio0	GPIO_5 Interrupt
6	gpio0	GPIO_6 Interrupt
7	gpio0	GPIO_7 Interrupt
8	gpio1	GPIO_8 Interrupt
9	gpio1	GPIO_9 Interrupt
10	gpio1	GPIO_10 Interrupt
11	gpio1	GPIO_11 Interrupt
12	gpio1	GPIO_12 Interrupt
13	gpio1	GPIO_13 Interrupt
14	gpio1	GPIO_14 Interrupt
15	gpio1	GPIO_15 Interrupt
16	gpio2	GPIO_16 Interrupt
17	gpio2	GPIO_17 Interrupt
18	gpio2	GPIO_18 Interrupt
19	gpio2	GPIO_19 Interrupt
20	gpio2	GPIO_20 Interrupt
21	gpio2	GPIO_21 Interrupt
22	gpio2	GPIO_22 Interrupt
23	gpio2	GPIO_23 Interrupt
24	gpio3	GPIO_24 Interrupt
25	gpio3	GPIO_25 Interrupt
26	gpio3	GPIO_26 Interrupt
27	gpio3	GPIO_27 Interrupt
28	gpio3	GPIO_28 Interrupt
29	gpio3	GPIO_29 Interrupt
30	gpio3	GPIO_30 Interrupt
31	gpio3	GPIO_31 Interrupt
32	spim0	SPI0 Interrupt
33	spim1	SPI1 Interrupt
34	spim2	SPI2 Interrupt
35	spim3	SPI3 Interrupt
36	i2c0	I2C0 Interrupt
37	i2c1	I2C1 Interrupt
38	i2c2	I2C2 Interrupt
39	rtclv	RTC Interrupt
40	uart0	uart0 Interrupt
41	uart1	uart1 Interrupt
42	uart2	uart2 Interrupt
43	usb2fs	USB2FS Interrupt
44	sramc	SRAM M2M Transfer complete Interrupt
45	sramc	SRAM M2M Transfer error Interrupt
46	spic	Quad SPI Interrupt (NOR Flash)
47	aesa	AES Engine Interrupt
48	sdmac	DMAC ch0 Interrupt
49	sdmac	DMAC ch1 Interrupt
50	sdmac	DMAC ch2 Interrupt

No.	Module	Description
51	sdmac	DMAC ch3 Interrupt
52	sdmac	DMAC ch4 Interrupt
53	sdmac	DMAC ch5 Interrupt
54	sdmac	DMAC ch6 Interrupt
55	sdmac	DMAC ch7 Interrupt
56	adcc12	adcc12 Interrupt
57	adcc24	adcc24 Interrupt
58	-	Reserved
59	wdt	wdt Interrupt
60	tmr	tmr1 Interrupt
61	tmr	tmr2 Interrupt
62	-	Reserved
63	-	Reserved
64	advtmr	advtmr0 Interrupt
65	advtmr	advtmr1 Interrupt
66	advtmr	advtmr2 Interrupt
67	advtmr	advtmr3 Interrupt
68	advtmr	advtmr0 capture Interrupt
69	advtmr	advtmr1 capture Interrupt
70	advtmr	advtmr2 capture Interrupt
71	advtmr	advtmr3 capture Interrupt
72	advtmr	advtmr0 compare Interrupt
73	advtmr	advtmr1 compare Interrupt
74	advtmr	advtmr2 compare Interrupt
75	advtmr	advtmr3 compare Interrupt
76	pmulv	pmulv wake up Interrupt
77	pmulv	pmulv Brown Out Interrupt
78	cpu	cpu debug interrupt
79	cpu	fpu exception Interrupt

Table 3.2 The difference of Interrupts by package

No.	Module	Description	TZ1041	TZ1011/TZ1031	TZ1021
24	gpio3	GPIO_24 Interrupt	-	Magnetometer (TZ1011 only)	external PIN
25	gpio3	GPIO_25 Interrupt	-	-	external PIN
26	gpio3	GPIO_26 Interrupt	-	6-axis Sensor (Acc. & Gyro.)	external PIN
27	gpio3	GPIO_27 Interrupt	-	-	external PIN
28	gpio3	GPIO_28 Interrupt	-	-	external PIN
29	gpio3	GPIO_29 Interrupt	BLE	BLE	external PIN
30	gpio3	GPIO_30 Interrupt	BLE	BLE	external PIN
31	gpio3	GPIO_31 Interrupt	-	-	external PIN
-					
34	spim2	SPI2 Interrupt	-	external device	external device
35	spim3	SPI3 Interrupt	-	6-axis Sensor (Acc. & Gyro.)	external device
-					
38	i2c2	I2C2 Interrupt	-	Magnetometer (TZ1011 only), external devices	external devices
-					
42	uart2	uart2 Interrupt	BLE	BLE	external device

3.1. CPU Interrupts

3.1.1. cpu debug interrupt

When debugger is connected, Internal Interrupt signal is asserted. Refer to 5.6 Debugger detection for details.

3.1.2. fpu exception Interrupt

When an FPU exception occurs, Internal Interrupt signal is asserted. It is possible to mask or unmask the interrupts for each factor of an FPU exception by setting the gconf.*[CPU_FPUIRQEN]* register.

FPU (exception status)	gconf (interrupt enable)
[FPSCR].IDC	***[CPU_FPUIRQEN]***.IDE
[FPSCR].IXC	***[CPU_FPUIRQEN]***.IXE
[FPSCR].UFC	***[CPU_FPUIRQEN]***.UFE
[FPSCR].OFC	***[CPU_FPUIRQEN]***.OFE
[FPSCR].DZC	***[CPU_FPUIRQEN]***.DZE
[FPSCR].IOC	***[CPU_FPUIRQEN]***.IOE

4. Address map

Table 4.1 MCU Processor and core peripherals Register map

Register Name	Type	Width	Reset Value	Address Offset
ITM_STIM	RW	32	-	0x0 0000-
ITM_TER	RW	32	0x0000 0000	0x0 0E00
ITM_TPR	RW	32	0x0000 0000	0x0 0E40
ITM_TCR	RW	32	0x0000 0000	0x0 0E80
ITM_PID4	RO	32	0x0000 0004	0x0 0FD0
ITM_PID5	RO	32	0x0000 0000	0x0 0FD4
ITM_PID6	RO	32	0x0000 0000	0x0 0FD8
ITM_PID7	RO	32	0x0000 0000	0x0 0FDC
ITM_PID0	RO	32	0x0000 0001	0x0 0FE0
ITM_PID1	RO	32	0x0000 00B0	0x0 0FE4
ITM_PID2	RO	32	0x0000 003B	0x0 0FE8
ITM_PID3	RO	32	0x0000 0000	0x0 0FEC
ITM_CID0	RO	32	0x0000 000D	0x0 0FF0
ITM_CID1	RO	32	0x0000 00E0	0x0 0FF4
ITM_CID2	RO	32	0x0000 0005	0x0 0FF8
ITM_CID3	RO	32	0x0000 00B1	0x0 0FFC
DWT_CTRL	RW	32	0x4000 0000	0x0 1000
DWT_CYCCNT	RW	32	0x0000 0000	0x0 1004
DWT_CPICNT	RW	32	-	0x0 1008
DWT_EXCCNT	RW	32	-	0x0 100C
DWT_SLEEPCNT	RW	32	-	0x0 1010
DWT_LSUCNT	RW	32	-	0x0 1014
DWT_FOLDCNT	RW	32	-	0x0 1018
DWT_PCSR	RW	32	-	0x0 101C
DWT_COMP0	RW	32	-	0x0 1020
DWT_MASK0	RW	32	-	0x0 1024
DWT_FUNCTION0	RW	32	0x0000 0000	0x0 1028
DWT_COMP1	RW	32	-	0x0 1030
DWT_MASK1	RW	32	-	0x0 1034
DWT_FUNCTION1	RW	32	0x0000 0000	0x0 1038
DWT_COMP2	RW	32	-	0x0 1040
DWT_MASK2	RW	32	-	0x0 1044
DWT_FUNCTION2	RW	32	0x0000 0000	0x0 1048
DWT_COMP3	RW	32	-	0x0 1050
DWT_MASK3	RW	32	-	0x0 1054
DWT_FUNCTION3	RW	32	0x0000 0000	0x0 1058
DWT_PID4	RO	32	0x0000 0004	0x0 1FD0
DWT_PID5	RO	32	0x0000 0000	0x0 1FD4
DWT_PID6	RO	32	0x0000 0000	0x0 1FD8
DWT_PID7	RO	32	0x0000 0000	0x0 1FDC
DWT_PID0	RO	32	0x0000 0002	0x0 1FE0
DWT_PID1	RO	32	0x0000 00B0	0x0 1FE4
DWT_PID2	RO	32	0x0000 003B	0x0 1FE8
DWT_PID3	RO	32	0x0000 0000	0x0 1FEC
DWT_CID0	RO	32	0x0000 000D	0x0 1FF0
DWT_CID1	RO	32	0x0000 00E0	0x0 1FF4
DWT_CID2	RO	32	0x0000 0005	0x0 1FF8
DWT_CID3	RO	32	0x0000 00B1	0x0 1FFC
FP_CTRL	RW	32	0x0000 0260	0x0 2000
FP_REMAP	RW	32	-	0x0 2004
FP_COMP0	RW	32	0x0000 0000	0x0 2008
FP_COMP1	RW	32	0x0000 0000	0x0 200C
FP_COMP2	RW	32	0x0000 0000	0x0 2010

Register Name	Type	Width	Reset Value	Address Offset
FP_COMP3	RW	32	0x0000 0000	0x0 2014
FP_COMP4	RW	32	0x0000 0000	0x0 2018
FP_COMP5	RW	32	0x0000 0000	0x0 201C
FP_COMP6	RW	32	0x0000 0000	0x0 2020
FP_COMP7	RW	32	0x0000 0000	0x0 2024
FP_PID4	RO	32	0x0000 0004	0x0 2FD0
FP_PID5	RO	32	0x0000 0000	0x0 2FD4
FP_PID6	RO	32	0x0000 0000	0x0 2FD8
FP_PID7	RO	32	0x0000 0000	0x0 2FDC
FP_PID0	RO	32	0x0000 0003	0x0 2FE0
FP_PID1	RO	32	0x0000 00B0	0x0 2FE4
FP_PID2	RO	32	0x0000 002B	0x0 2FE8
FP_PID3	RO	32	0x0000 0000	0x0 2FEC
FP_CID0	RO	32	0x0000 000D	0x0 2FF0
FP_CID1	RO	32	0x0000 00E0	0x0 2FF4
FP_CID2	RO	32	0x0000 0005	0x0 2FF8
FP_CID3	RO	32	0x0000 00B1	0x0 2FFC
ICTR	RO	32	0x0000 0002	0x0 E004
ACTLR	RW	32	0x0000 0000	0x0 E008
SYST_CSR	RW	32	0x0000 0004	0x0 E010
SYST_RVR	RW	32	-	0x0 E014
SYST_CVR	RW	32	-	0x0 E018
SYST_CALIB	RO	32	0xC000 0000	0x0 E01C
NVIC_ISER0	RW	32	0x0000 0000	0x0 E100
NVIC_ISER1	RW	32	0x0000 0000	0x0 E104
NVIC_ISER2	RW	32	0x0000 0000	0x0 E108
NVIC_ICER0	RW	32	0x0000 0000	0x0 E180
NVIC_ICER1	RW	32	0x0000 0000	0x0 E184
NVIC_ICER2	RW	32	0x0000 0000	0x0 E188
NVIC_ISPR0	RW	32	0x0000 0000	0x0 E200
NVIC_ISPR1	RW	32	0x0000 0000	0x0 E204
NVIC_ISPR2	RW	32	0x0000 0000	0x0 E208
NVIC_ICPR0	RW	32	0x0000 0000	0x0 E280
NVIC_ICPR1	RW	32	0x0000 0000	0x0 E284
NVIC_ICPR2	RW	32	0x0000 0000	0x0 E288
NVIC_IABR0	RO	32	0x0000 0000	0x0 E300
NVIC_IABR1	RO	32	0x0000 0000	0x0 E304
NVIC_IABR2	RO	32	0x0000 0000	0x0 E308
NVIC_IPR0	RW	32	0x0000 0000	0x0 E400
NVIC_IPR1	RW	32	0x0000 0000	0x0 E404
NVIC_IPR2	RW	32	0x0000 0000	0x0 E408
NVIC_IPR3	RW	32	0x0000 0000	0x0 E40C
NVIC_IPR4	RW	32	0x0000 0000	0x0 E410
NVIC_IPR5	RW	32	0x0000 0000	0x0 E414
NVIC_IPR6	RW	32	0x0000 0000	0x0 E418
NVIC_IPR7	RW	32	0x0000 0000	0x0 E41C
NVIC_IPR8	RW	32	0x0000 0000	0x0 E420
NVIC_IPR9	RW	32	0x0000 0000	0x0 E424
NVIC_IPR10	RW	32	0x0000 0000	0x0 E428
NVIC_IPR11	RW	32	0x0000 0000	0x0 E42C
NVIC_IPR12	RW	32	0x0000 0000	0x0 E430
NVIC_IPR13	RW	32	0x0000 0000	0x0 E434
NVIC_IPR14	RW	32	0x0000 0000	0x0 E438
NVIC_IPR15	RW	32	0x0000 0000	0x0 E43C
NVIC_IPR16	RW	32	0x0000 0000	0x0 E440
NVIC_IPR17	RW	32	0x0000 0000	0x0 E444
NVIC_IPR18	RW	32	0x0000 0000	0x0 E448
NVIC_IPR19	RW	32	0x0000 0000	0x0 E44C

Register Name	Type	Width	Reset Value	Address Offset
SCS_CPUID	RO	32	0x410F C241	0x0 ED00
SCS_ICSR	RW	32	0x0000 0000	0x0 ED04
SCS_VTOR	RW	32	0x0000 0000	0x0 ED08
SCS_AIRCR	RW	32	0xFA05 0000	0x0 ED0C
SCS_SCR	RW	32	0x0000 0000	0x0 ED10
SCS_CCR	RW	32	0x0000 0000	0x0 ED14
SCS_SHPR1	RW	32	0x0000 0000	0x0 ED18
SCS_SHPR2	RW	32	0x0000 0000	0x0 ED1C
SCS_SHPR3	RW	32	0x0000 0000	0x0 ED20
SCS_SHCRS	RW	32	0x0000 0000	0x0 ED24
SCS_CFSR	RW	32	0x0000 0000	0x0 ED28
SCS_HFSR	RW	32	0x0000 0000	0x0 ED2C
DFSR	RW	32	0x0000 0000	0x0 ED30
SCS_MMAR	RW	32	-	0x0 ED34
SCS_BFAR	RW	32	-	0x0 ED38
SCS_AFSR	RW	32	0x0000 0000	0x0 ED3C
SCS_ID_PFR0	RO	32	0x0000 0030	0x0 ED40
SCS_ID_PFR1	RO	32	0x0000 0200	0x0 ED44
SCS_ID_DFR0	RO	32	0x0010 0000	0x0 ED48
SCS_ID_AFR0	RO	32	0x0000 0000	0x0 ED4C
SCS_ID_MMFR0	RO	32	0x0010 0030	0x0 ED50
SCS_ID_MMFR1	RO	32	0x0000 0000	0x0 ED54
SCS_ID_MMFR2	RO	32	0x0100 0000	0x0 ED58
SCS_ID_MMFR3	RO	32	0x0000 0000	0x0 ED5C
SCS_ID_ISAR0	RO	32	0x0114 1110	0x0 ED60
SCS_ID_ISAR1	RO	32	0x0211 2000	0x0 ED64
SCS_ID_ISAR2	RO	32	0x2123 2231	0x0 ED68
SCS_ID_ISAR3	RO	32	0x0111 1131	0x0 ED6C
SCS_ID_ISAR4	RO	32	0x0131 0132	0x0 ED70
CPACR	RW	32	0x0000 0000	0x0 ED88
MPU_TYPE	RO	32	0x0000 0800	0x0 ED90
MPU_CTRL	RW	32	0x0000 0000	0x0 ED94
MPU_RNR	RW	32	0x0000 0000	0x0 ED98
MPU_RBAR	RW	32	0x0000 0000	0x0 ED9C
MPU_RASR	RW	32	0x0000 0000	0x0 EDA0
MPU_RBAR_A1	RW	32	0x0000 0000	0x0 EDA4
MPU_RASR_A1	RW	32	0x0000 0000	0x0 EDA8
MPU_RBAR_A2	RW	32	0x0000 0000	0x0 EDAC
MPU_RASR_A2	RW	32	0x0000 0000	0x0 EDB0
MPU_RBAR_A3	RW	32	0x0000 0000	0x0 EDB4
MPU_RASR_A3	RW	32	0x0000 0000	0x0 EDB8
DHCSR	RW	32	0x0000 0000	0x0 EDF0
DCRSR	RW	32	0x0000 0000	0x0 EDF4
DCRDR	RW	32	0x0000 0000	0x0 EDF8
DEMCR	RW	32	0x0000 0000	0x0 EDFC
STIR	RW	32	0x0000 0000	0x0 EF00
FPCCR	RW	32	0xC000 0000	0x0 EF34
FPCAR	RW	32	0x0000 0000	0x0 EF38
FPDSCR	RW	32	0x0000 0000	0x0 EF3C
MVFR0	RO	32	0x1011 0021	0x0 EF40
MVFR1	RO	32	0x1100 0011	0x0 EF44
SCS_PERIPHERAL_ID4	RO	32	0x0000 0004	0x0 EFD0
SCS_PERIPHERAL_ID0	RO	32	0x0000 000C	0x0 EFE0
SCS_PERIPHERAL_ID1	RO	32	0x0000 00B0	0x0 EFE4
SCS_PERIPHERAL_ID2	RO	32	0x0000 000B	0x0 EFE8
SCS_PERIPHERAL_ID3	RO	32	0x0000 0000	0x0 EFEC
SCS_COMPONENT_ID0	RO	32	0x0000 000D	0x0 EFF0
SCS_COMPONENT_ID1	RO	32	0x0000 00E0	0x0 EFF4

Register Name	Type	Width	Reset Value	Address Offset
SCS_COMPONENT_ID2	RO	32	0x0000 0005	0x0 EFF8
SCS_COMPONENT_ID3	RO	32	0x0000 00B1	0x0 EFFC
TPIU_SSPSR	RO	32	-	0x4 0000
TPIU_CSPSR	RW	32	0x0000 0001	0x4 0004
TPIU_ACPR	RW	32	0x0000 0000	0x4 0010
TPIU_SPPR	RW	32	0x0000 0001	0x4 00F0
TPIU_FFSR	RO	32	0x0000 0008	0x4 0300
TPIU_FFCR	RW	32	0x0000 0102	0x4 0304
TPIU_FSCR	RO	32	0x0000 0000	0x4 0308
TPIU_TRIGGER	RO	32	0x0000 0000	0x4 0EE8
TPIU_FIFO_DATA0	RO	32	0x0000 0000	0x4 0EEC
TPIU_ITATBCTR2	RO	32	0x0000 0000	0x4 0EF0
TPIU_ITATBCTR0	RO	32	0x0000 0000	0x4 0EF8
TPIU_FIFO_DATA1	RO	32	0x0000 0000	0x4 0EFC
TPIU_ITCTRL	RW	32	0x0000 0000	0x4 0F00
TPIU_CLAIMSET	RW	32	0x0000 000F	0x4 0FA0
TPIU_CLAIMCLR	RW	32	0x0000 0000	0x4 0FA4
TPIU_DEVID	RO	32	0x0000 0CA0	0x4 0FC8
TPIU_DEVTYPE	RO	32	0x0000 0011	0x4 0FCC
TPIU_PID4	RO	32	0x0000 0004	0x4 0FD0
TPIU_PID5	RO	32	0x0000 0000	0x4 0FD4
TPIU_PID6	RO	32	0x0000 0000	0x4 0FD8
TPIU_PID7	RO	32	0x0000 0000	0x4 0FDC
TPIU_PID0	RO	32	0x0000 00A1	0x4 0FE0
TPIU_PID1	RO	32	0x0000 00B9	0x4 0FE4
TPIU_PID2	RO	32	0x0000 000B	0x4 0FE8
TPIU_PID3	RO	32	0x0000 0000	0x4 0FEC
TPIU_CID0	RO	32	0x0000 000D	0x4 0FF0
TPIU_CID1	RO	32	0x0000 0090	0x4 0FF4
TPIU_CID2	RO	32	0x0000 0005	0x4 0FF8
TPIU_CID3	RO	32	0x0000 00B1	0x4 0FFC
SCS	RO	32	0xFFF0 F003	0xF F000
DWT	RO	32	0xFFF0 2003	0xF F004
FPB	RO	32	0xFFF0 3003	0xF F008
ITM	RO	32	0xFFF0 1003	0xF F00C
TPIU	RO	32	0xFFF4 1003	0xF F010
ETM	RO	32	0xFFF4 2002	0xF F014
END_MARKER	RO	32	0x0000 0000	0xF F018
SYSTEM_ACCESS	RO	32	0x0000 0001	0xF FFCC
PERIPHERAL_ID4	RO	32	0x0000 0004	0xF FFD0
PERIPHERAL_ID5	RO	32	0x0000 0000	0xF FFD4
PERIPHERAL_ID6	RO	32	0x0000 0000	0xF FFD8
PERIPHERAL_ID7	RO	32	0x0000 0000	0xF FFDC
PERIPHERAL_ID0	RO	32	0x0000 00C4	0xF FFE0
PERIPHERAL_ID1	RO	32	0x0000 00B4	0xF FFE4
PERIPHERAL_ID2	RO	32	0x0000 000B	0xF FFE8
PERIPHERAL_ID3	RO	32	0x0000 0000	0xF FFEC
COMPONENT_ID0	RO	32	0x0000 000D	0xF FFF0
COMPONENT_ID1	RO	32	0x0000 0010	0xF FFF4
COMPONENT_ID2	RO	32	0x0000 0005	0xF FFF8
COMPONENT_ID3	RO	32	0x0000 00B1	0xF FFFC

5. Debug

5.1. Features

- Serial Wire Debug Port (SW-DP) or JTAG Debug Port (SWJ-DP) debug access.
- Flash Patch and Breakpoint (FPB) unit for implementing breakpoints and code patches
- Data Watch point and Trace (DWT) unit for implementing watch points, data tracing, and system profiling.
- Instrumentation Trace Macrocell (ITM) for support of printf() style debugging.
- Trace Port Interface Unit (TPIU) for bridging to a Trace Port Analyzer (TPA), including Single Wire Output (SWO) mode.
- Debugger Detection function

5.2. Overview

The TZ1000 Series core has Arm® Cortex®-M4 CoreSight™ debug components. The supported interfaces are Serial Wire debug ports (2 pins) / JTAG debug Port (5 pins). The Pins of Serial wire debug ports are multiplexed with some of the five JTAG debug ports. The integrated debug functions of CoreSight™ are Instruction Break, Code Patch, Data access break point and Trace port interface.

Debugger Hot Plugging makes core debugging in low power mode by generating interrupt or wake up signal when debugger is connected.

Debugger accessibility is restricted by setting internal register for code and data security.

Figure 5.1 shows the block diagram of Core and debug components.

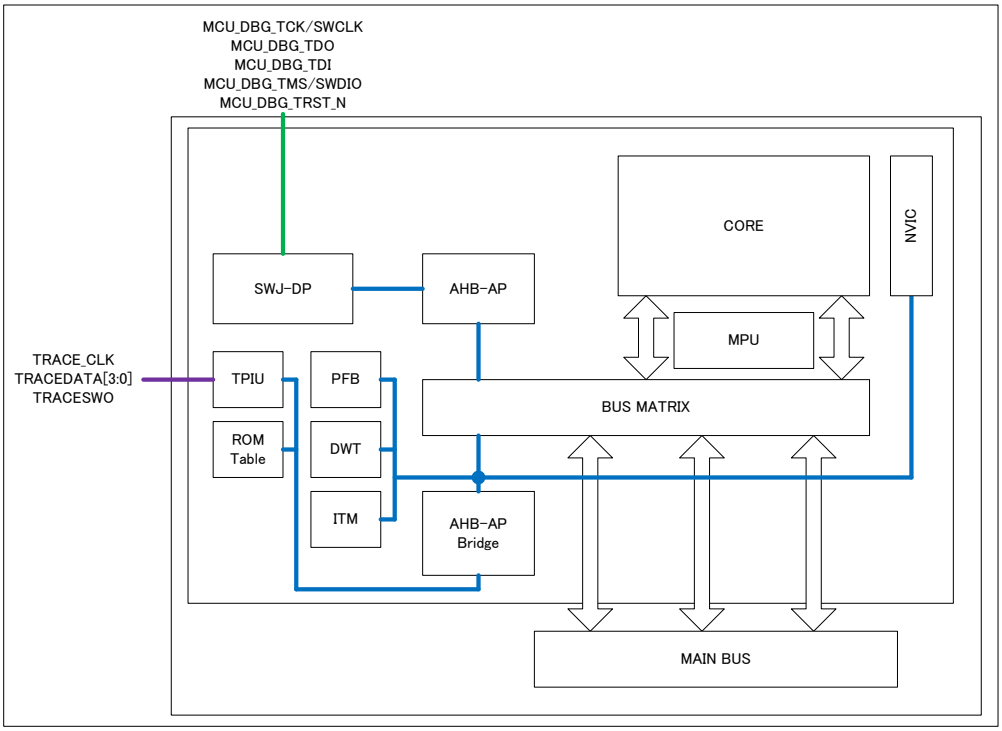

Figure 5.1 Block diagram of Core and debug components

For more information on Arm® debug components, refer to:

- Armv7-M Architecture Reference Manual
- Arm Debug Interface v5 Architecture Specification
- Arm CoreSight Components Technical Reference Manual
- Arm Cortex-M4 Technical Reference Manual

5.3. Pin-out and debug port

JTAG pins (MCU_DBG_TCK, MCU_DBG_TDO, MCU_DBG_TDI, MCU_DBG_TMS, MCU_DBG_TRST_N) are dedicated to JTAG debug port or Serial Wire debug port. Trace Interface signals (TRACECLK, TRACEDATA[3:0]) are multiplexed with Other functional pins (MCU_SPIM0_MISO, MCU_GPIO8, MCU_GPIO9, MCU_GPIO10, MCU_GPIO11).

Table 5.1 I/O Lines Description

Pin Name	direction	Pull up/down	JTAG Debug Port	Serial Wire debug Port
MCU_DBG_TCK	Input	Pull-down	Debug Clock	Serial Wire Clock
MCU_DBG_TDO	Output	-	Debug Data Out	Trace asynchronous Data Output
MCU_DBG_TDI	Input	Pull-up	Debug Data In	NA
MCU_DBG_TMS	Input/output	Pull-up	Debug Mode Select	Serial Wire Input/Output Data
MCU_DBG_TRST_N	Input	Pull-up	Reset	Reset

Table 5.2 I/O Lines for Trace port

Pin Name	Trace Port
MCU_SPIM0_MISO	TRACECLK
MCU_GPIO8	TRACEDATA[0]
MCU_GPIO9	TRACEDATA[1]
MCU_GPIO10	TRACEDATA[2]
MCU_GPIO11	TRACEDATA[3]

After MCU_DBG_TRST_N de-assertion, the SWJ-DP of CoreSight™ interface is in JTAG mode. but it can be switched to the Serial Wire mode by the specific sequence of MCU_DBG_TCK and MCU_DBG_TMS.

5.4. Power mode

When the TZ1000 Series is in Active, Sleep0/1/2(sleeping) mode, debugger connection is available. When Sleep0/1/2(deep sleep), WAIT and WAIT-RETENTION mode, debugger connection is available if debugger detection function is enable. When Retention, RTC, STOP mode, debugger connection is NOT available.

When debugger is connection, the TZ1000 Series returns to Active mode immediately from low-power mode if debugger detection is enable.

5.5. Debug Feature

5.5.1. The Serial Wire/JTAG Debug Port (SWJ-DP)

The SWJ-DP provides a mechanism to select between Serial Wire and JTAG Data Link protocols. This enables the JTAG-DP and SW-DP to share pins.

SWJ-DP is a combined JTAG-DP and SW-DP that enables a probe to connect to the target using either the Serial Wire protocol or JTAG. To make efficient use of package pins, the Serial Wire interface shares, or overlays, the JTAG pins use an auto detect mechanism that switch between JTAG-DP and SW-DP depending on which prove is connected. A special sequence on the MCU_DBG_TMS pin is used to switch between JTAG-DP and SW-DP. When the switching sequence has been transmitted to the SWJ-DP, it behaves as a dedicated JTAG-DP or SW-DP depending upon which sequence had been performed.

After MCU_TRST_N de-assertion, the SWJ-DP of CoreSight™ interface is in JTAG mode. The following sequence changes to SW-DP mode.

(1) Send more than 50 MCU_DBG_CLK cycles with MCU_DBG_TMS =1.
(2) Send the 16-bit sequence on MCU_DBG_TMS = 0111100111100111
(3) Send more than 50 MCU_CBG_CLK cycles with MCU_DBG_TMS =1

Note: PMULV.CPU_DEBUG.CPU_DEBUG bit is 0, JTAG connection is rejected.

5.5.2. The Flash Patch and Breakpoint (FPB)

The Flash Patch and Breakpoint (FPB) unit can support:

- remapping specific literal locations from the Code region of system memory to addresses in the SRAM region
- remapping specific instruction addresses from the Code region of system memory to addresses in the SRAM region
- breakpoint functionality on instruction fetches.

5.5.3. The Data Watch point and Trace (DWT)

The Data Watch point and Trace (DWT) unit provides the following:

- comparators, that support:
  watch points, that cause the processor to enter Debug state or take a Debug Monitor exception
  data tracing
  PC value tracing
  cycle count matching.
- additional PC sampling:
  PC sample trace output as a result of a cycle count event
  external PC sampling using a PC sample register.
- exception trace
- performance profiling counters.

5.5.4. The Instrumentation Trace Macrocell (ITM)

The Instrumentation Trace Macrocell (ITM) provides a memory-mapped register interface that applications can use to write logging or event words to a trace sink, for example to the optional external Trace Port Interface Unit (TPIU). The ITM also provides control of timestamp packets, and generation of Local timestamp packets.

5.5.5. The Trace Port Interface Unit (TPIU)

To provide external visibility, an implementation typically includes a Trace Port Interface Unit (TPIU). This can be either the Armv7-M TPIU described in this section, or the full CoreSight™ TPIU.

The Armv7-M TPIU provides one or both**:**

- an asynchronous Serial Wire Output (SWO)
- a parallel trace port with a single or multi-pin data path, a clock pin, and optionally a control pin.

5.6. Debugger detection

The TZ1000 Series supports debugger detection and wake up in Active, Sleep0/1/2 and WAIT mode. When debugger is connected and MCU_DBG_TCK is toggled, Internal Interrupt and wake up signals are asserted at GCONF.CPU_DEBUGIN.CPU_DEBUGIN is set to one and the interrupt is enable or wake up is enable, the TZ1000 Series returns to Active mode from the state of each power mode (Sleep0/1/2, Wait).

The following shows the timing of signal detection and return timing.

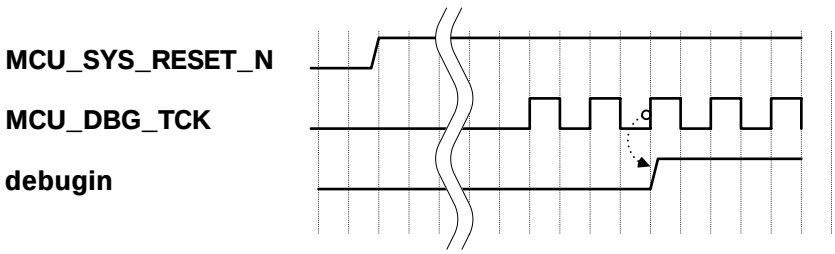

Figure 5.2 Debugger Hot Plugging Detection Timings Diagram

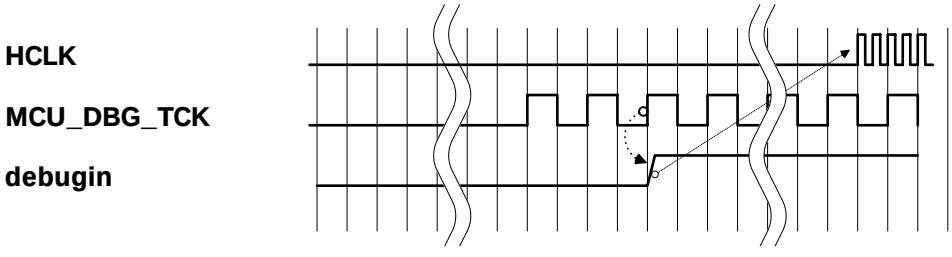

Figure 5.3 Return timing from sleep/wait mode by Debugger Hot Plugging

5.7. Trace signal output enable

When Trace function is used, it is necessary to operate Trace signal in the CPU_TRACE_OE bit of the following register.

- Enable for the TRACECLK/TRACEDATA of the CPU

GCONF register	Bit name	value
OE_CTRL	CPU_TRACE_OE	0x00001***

Note: Bits 12 of the OE_CTRL register correspond with the CPU TRACECLK/TRACEDATA.

Note: "*" shows the signal which also controls another function.

5.8. PMU initialization setting when connecting a debugger

After the SYSRESETREQ (***[CTRL_CDBGPWRUPREQ]***.CDBGPWRUPREQ_EN = 1b1) execution by the debugger, setting procedure to initialize PMU is as follows. For the SYSRESETREQ operation in the debugger connection, refer to 4.1.9.7 of the latest PMU Reference Manual (TZ1000_E_RM203_MCU_PMU).

No.	Control Overview	PMU register or Waiting time	Address	Write value	Read operation
1	Check the status of PMU hardware sequencer	**-**	-	-	-
	Power Domain control	***[POWERDOMAIN_CTRL]***	0x40000710	-	Polling until read value is 0x00000000
	Voltage Mode transition	***[MOVE_VOLTAGE_START]***	0x40000700	-	Polling until “read value & 0x00000001” is 0x00000000.
2	Initialize DCDC	**-**	-	-	-
	Initialize an external clock	***[CG_OFF_HARDMACRO]***	0x400001c0	0x00010000	-
	soft start disable, external clock mode	***[CONFIG_DCDC_LVREG_1]***	0x40000528	0x80040000	-
3	Trimming value setting for clock source	**-**	-	-	-
	Set the trimming value for SiOSC4M ModeA	***[EFUSE_SiOSC4M]***	0x400005e4	-	(write back “read value” to ***[OVERRIDE_EFUSE_SiOSC4M]***)
	-	***[SELECT_EFUSE]***	0x400005c0	0x00001000	-
	-	***[CONFIG_SiOSC4M]***	0x40002108	0x00000011	-
	-	***[OVERRIDE_EFUSE_SiOSC4M]***	0x40002188	Read value of ***[EFUSE_SiOSC4M]***	-
	-	***[CONFIG_SiOSC4M]***	0x40002108	0x00000001	-
4	Initialize Voltage Mode (ModeA) with PMU hardware sequencer	**-**	-	-	-
	-	***[WAITTIME_DVSCTL]***	0x40000748	0x00a01e1e	-
	-	***[MOVE_POWER_VOLTAGE_MODE]***	0x40000704	0x00000000	-
	-	***[MOVE_VOLTAGE_START]***	0x40000700	0x00000001	-
	Check the completion of transition	***[MOVE_VOLTAGE_START]***	0x40000700	-	Polling until read value is 0x00000000
	-	***[VOLTAGEMODE_SETTING]***	0x40000730	0x00000000	-
5	Initialize CSM (SiOSC4M)	**-**	-	-	-
	MAIN	***[CSM_MAIN]***	0x40000404	0x00000000	-
	CPUTRC	***[CSM_CPUTRC]***	0x40000408	0x00000000	-
	CPUST	***[CSM_CPUST]***	0x4000040c	0x00000000	-
	UART0	***[CSM_UART0]***	0x40000414	0x00000000	-
	UART1	***[CSM_UART1]***	0x40000418	0x00000000	-
	UART2	***[CSM_UART2]***	0x4000041c	0x00000000	-
	ADCC12A	***[CSM_ADCC12A]***	0x40000420	0x00000000	-
	ADCC24A	***[CSM_ADCC24A]***	0x40000424	0x00000000	-
6	Set prescaler excluding the USBI to divide-by-1	***[PRESCAL_MAIN]***	0x40000484	0x00111111	-
	-	***[PRESCAL_CPUST]***	0x4000048c	0x00000001	-
	-	***[PRESCAL_UART0]***	0x40000494	0x00000001	-
	-	***[PRESCAL_UART1]***	0x40000498	0x00000001	-
	-	***[PRESCAL_UART2]***	0x4000049c	0x00000001	-

	-	***[PRESCAL_ADCC12A]***	0x400004a0	0x00000001	-
	-	***[PRESCAL_ADCC24A]***	0x400004a4	0x00000001	-
7	Initialize PLL & start	**-**	-	-	-
	(1) Check the status of OSC12M	***[CONFIG_OSC12M].OSC12M_EN***	0x40000500	-	If “read value” is 0b1 then go to (3), else if “read value” is 0b0 then go to (2)
	(2) Start the OSC12M	***[CONFIG_OSC12M]***	0x40000500	0x00000001	-
	-	Wait 10ms	-	-	-
	(3) Check the status of PPLL PSW	***[PSW_PLL]***	0x40002444	-	If “read value” is 0b11 then go to (5), else if “read value” is 0b00 then go to (4).
	(4) Control PPLL PSW (On)	***[PSW_PLL]***	0x40002444	0x00000001	-
	-	***[PSW_PLL]***	0x40002444	0x00000003	-
	(5) Check the status of PPLL ISO	***[ISO_PLL]***	0x40002544	-	If “read value” is 0b00 then go to (7), else if “read value” is 0b11 then go to (6).
	(6) Control PPLL ISO (Off)	***[ISO_PLL]***	0x40002544	0x00000000	-
	(7) Change PLL Frequency & start	***[CONFIG_PLL_0]***	0x40000508	0x80000001	-
	-	***[CONFIG_PLL_1]***	0x4000050c	0x00000093	-
	-	Wait 100us	-	-	-
	-	***[CONFIG_PLL_0]***	0x40000508	0x00000000	-
	-	Wait 100us	-	-	-
8	Initialize CSM_USBI (PLL)	***[CSM_USBI]***	0x40000410	0x00000000	-
9	Set prescaler USBI to divide-by-1	***[PRESCAL_USBI]***	0x40000490	0x00000001	-
10	Initialize PU clock/reset (stop clock, asserts reset)	***[SRST_ON_PU]***	0x4000032c	0x0000000d	-
	-	***[SRST_ON_PU]***	0x4000032c	0x00000010	-
	-	***[CG_ON_POWERDOMAIN]***	0x40000000	0x00000100	-
11	Initialize PU ISO (On)	***[ISO_PU]***	0x40002520	0x00000003	-
12	Initialize PU, IO_USB, ACC, MAG, GYRO PSW (Off)	***[PSW_IO_USB]***	0x40002450	0x00000000	-
	-	***[PSW_PU]***	0x40002420	0x00000000	-
	-	***[PSW_HARDMACRO]***	0x40002454	0x00000000	-
13	Initialize prescaler USBI (stop)	***[PRESCAL_USBI]***	0x40000490	0x00000000	-
14	Initialize CSM_MAIN		-	-	-
	Check the value of efuse_CSM_MAIN	***[EFUSE_BOOTSEQ]. EFUSE_SEL_CSM_MAIN***	0x400005e0	-	If “read value” is 0b00 then go to 14a else if “read value” is 0b01 then go to 14b else if “read value” is 0b1x then go to 14c
14a	After starting OSC12M & PLL, change CSM_MAIN	**-**	-	-	-
	(1) Check the status of OSC12M	***[CONFIG_OSC12M].OSC12M_EN***	0x40000500	-	If “read value” is 0b1 then go to (3) else if “read value” is 0b0 then go to (2)
	(2) Start OSC12M	***[CONFIG_OSC12M]***	0x40000500	0x00000001	-
	-	Wait 10ms	-	-	-
	(3) Check the status of PPLL	***[PSW_PLL]***	0x40002444	-	If “read value” is 0b11 then go to (5)

	PSW				else if “read value” is 0b00 then go to (4)
	(4) Control PPLL PSW (On)	***[PSW_PLL]***	0x40002444	0x00000001	-
		[PSW_PLL]	0x40002444	0x00000003	-
	(5) Check the status of PPLL ISO	***[ISO_PLL]***	0x40002544	-	If “read value” is 0b00 then go to (7) else if “read value” is 0b11 then go to (6)
	(6) Control PPLL ISO (Off)	***[ISO_PLL]***	0x40002544	0x00000000	-
	(7) Check the status of PLL	***[CONFIG_PLL_0].PLL_BP***	0x40000508	-	If “read value” is 0b0 then go to (9) else if “read value” is 0b1 then go to (8)
	(8) Start PLL	***[CONFIG_PLL_0]***	0x40000508	0x00000001	-
	-	Wait 100us	-	-	-
	-	***[CONFIG_PLL_0]***	0x40000508	0x00000000	-
	-	Wait 100us	-	-	-
	(9) Change CSM_MAIN	***[CSM_MAIN]***	0x40000404	0x00000002	-
	(10) go to No.15	**-**	-	-	-
14b	After starting OSC12M, change CSM_MAIN. Then, stop PLL	**-**	-	-	-
	(1) Check the status of OSC12M	***[CONFIG_OSC12M].OSC12M_EN***	0x40000500	-	If “read value” is 0b1 then go to (3) else if “read value” is 0b0 then go to (2)
	(2) Start OSC12M	***[CONFIG_OSC12M]***	0x40000500	0x00000001	-
		Wait 10ms	-	-	-
	(3) Change CSM_MAIN	***[CSM_MAIN]***	0x40000404	0x00000001	-
	(4) Check the status of PLL	***[CONFIG_PLL_0].PLL_BP***	0x40000508	-	If “read value” is 0b0 then go to (5) else if “read value” is 0b1 then go to (6)
	(5) Stop PLL	***[CONFIG_PLL_0]***	0x40000508	0x00000001	-
	(6) Check the status of PPLL ISO	***[ISO_PLL]***	0x40002544	-	If “read value” is 0b00 then go to (7) else if “read value” is 0b11 then go to (8)
	(7) Control PPLL ISO (On)	***[ISO_PLL]***	0x40002544	0x00000003	-
	(8) Check the status of PPLL PSW	***[PSW_PLL]***	0x40002444	-	If “read value” is 0b11 then go to (9) else if “read value” is 0b00 then (b) is finished (go to No.15)
	(9) Control PPLL PSW (Off)	***[PSW_PLL]***	0x40002444	0x00000000	-
	(10) go to No.15	**-**	-	-	-
14c	After changing CSM_MAIN, stop OSC12M & PLL.	**-**	-	-	-
	(1) Change CSM_MAIN	***[CSM_MAIN]***	0x40000404	0x00000000	-
	(2) Check the status of OSC12M	***[CONFIG_OSC12M].OSC12M_EN***	0x40000500	-	If “read value” is 0b1 then go to (3) else if “read value” is 0b0 then (c) is finished (go to No.15)
	(3) Stop OSC12M	***[CONFIG_OSC12M]***	0x40000500	0x00000000	-
	(4) Check the status of PLL	***[CONFIG_PLL_0].PLL_BP***	0x40000508	-	If “read value” is 0b0 then go to (5) else if “read value” is 0b1 then go to (6)
	(5) Stop PLL	***[CONFIG_PLL_0]***	0x40000508	0x00000001	-
	(6) Check the status of PPLL ISO	***[ISO_PLL]***	0x40002544	-	If “read value” is 0b00 then go to (7) else if “read value” is 0b11 then go to (8)

	(7) Control PPLL ISO (On)	***[ISO_PLL]***	0x40002544	0x00000003	-
	(8) Check the status of PPLL PSW	***[PSW_PLL]***	0x40002444	-	If “read value” is 0b11 then go to (9) else if “read value” is 0b00 then (c) is finished (go to No.15)
	(9) Control PPLL PSW (Off)	***[PSW_PLL]***	0x40002444	0x00000000	-
	(10) go to No.15	**-**	-	-	-
15	Transition to Power-On the following Power domain in numerical order.	**-**	-	-	-
	-	***[WAITTIME_LDOF]***	0x40000740	0x001e001e	-
	-	***[WAITTIME_PSW]***	0x40000744	0x000f000f	-
	(1) PP1, PA24, PA12	***[POWERDOMAIN_CTRL_MODE]***	0x40000714	0x00000000	-
	-	***[POWERDOMAIN_CTRL]***	0x40000710	0x00000e00	-
	-	***[POWERDOMAIN_CTRL_STATUS]***	0x40000718	-	Polling until “read value & 0xffff3003” is 0x00000000.
	(2) PD, PF, PS0	***[POWERDOMAIN_CTRL_MODE]***	0x40000714	0x00000000	-
	-	***[POWERDOMAIN_CTRL]***	0x40000710	0x000000a4	-
	-	***[POWERDOMAIN_CTRL_STATUS]***	0x40000718	-	Polling until “read value & 0xfffffc33” is 0x00000000.
	-	Wait 1200us(1500us-300us)	-	-	-
	(3) PS2, PE	***[POWERDOMAIN_CTRL_MODE]***	0x40000714	0x00000000	-
	-	***[POWERDOMAIN_CTRL]***	0x40000710	0x00000012	-
	-	***[POWERDOMAIN_CTRL_STATUS]***	0x40000718	-	Polling until “read value & 0xffffff3f” is 0x00000000.
	(4) PS1	***[POWERDOMAIN_CTRL_MODE]***	0x40000714	0x00000000	-
	-	***[POWERDOMAIN_CTRL]***	0x40000710	0x00000008	-
	-	***[POWERDOMAIN_CTRL_STATUS]***	0x40000718	-	Polling until “read value” is 0x00000000.
16	Assert Power domain reset other than PM (with initialization)	***[SRST_ON_POWERDOMAIN]***	0x40000020	0xfffffffe	-
17	Assert PM domain reset (with initialization)	***[SRST_ON_PM_0]***	0x40000300	0xfeffffff	-
	-	***[SRST_ON_PM_1]***	0x40000304	0xffffffff	-
	-	***[SRST_ON_PM_2]***	0x40000308	0xffffffff	-
18	Initialize PP1, PA24, PA12, PU, PD, PE domain clock (stop)	***[CG_ON_POWERDOMAIN]***	0x40000000	0x00000f82	-
19	Initialize PM domain clock (stop)	***[CG_ON_PM_0]***	0x40000100	0x00500000	-
	-	***[CG_ON_PM_1]***	0x40000104	0xffffffff	-
	-	***[CG_ON_PM_2]***	0x40000108	0xffffffff	-
20	Initialize cpu_traceclk (stop)	***[CG_ON_PC_SCRT]***	0x40001124	0x00000004	-
	-		-	-	-
21	Initialize PM IO STBX	***[CTRL_IO_AON_2]***	0x40002308	0x00000000	-
	-	***[CTRL_IO_AON_3]***	0x4000230c	0x00000000	-
22	Initialize PP1 IO RESX, LATI, STBX	***[CTRL_IO_AON_6]***	0x40002318	0x00000000	-

	-	***[CTRL_IO_AON_5]***	0x40002314	0x00000000	-
	-	***[CTRL_IO_AON_4]***	0x40002310	0x00000001	-
23	Initialize PS2, PS1, PS0, PF domain clock (supply)	***[CG_OFF_POWERDOMAIN]***	0x40000004	0x0000003c	-
24	Initialize PF domain reset (deassert)	***[SRST_OFF_POWERDOMAIN]***	0x40000024	0x00000020	-
25	Initialize PM domain clock (supply)	***[CG_OFF_PM_0]***	0x40000180	0x08800000	-
26	Initialize PM domain reset (deassert)	***[SRST_OFF_PM_0]***	0x40000380	0x09000000	-
27	Initialize Power domain below in numerical order (Power Off)	**-**	-	-	-
	(1) PA24, PA12	***[POWERDOMAIN_CTRL_MODE]***	0x40000714	0x00144004	-
	-	***[POWERDOMAIN_CTRL]***	0x40000710	0x00000600	-
	-	***[POWERDOMAIN_CTRL_STATUS]***	0x40000718		Polling until “read value” is 0x00140000.
	(2) PD, PE	***[POWERDOMAIN_CTRL_MODE]***	0x40000714	0x00144004	-
	-	***[POWERDOMAIN_CTRL]***	0x40000710	0x00000082	-
	-	***[POWERDOMAIN_CTRL_STATUS]***	0x40000718		Polling until “read value” is 0x00144004.
28	Initialize prescaler other than USBI (divide-by-1 or Stop)	***[PRESCAL_MAIN]***	0x40000484	0x00000011	-
	-	***[PRESCAL_CPUST]***	0x4000048c	0x00000001	-
	-	***[PRESCAL_UART0]***	0x40000494	0x00000000	-
	-	***[PRESCAL_UART1]***	0x40000498	0x00000000	-
	-	***[PRESCAL_UART2]***	0x4000049c	0x00000000	-
	-	***[PRESCAL_ADCC12A]***	0x400004a0	0x00000000	-
	-	***[PRESCAL_ADCC24A]***	0x400004a4	0x00000000	-
29	Initialize ADPLL (stop)	***[CONFIG_ADPLL_0]***	0x40000510	0x00007008	-
	-	***[CONFIG_ADPLL_1]***	0x40000514	0x00000000	-
30	Initialize PADPLL ISO (On)	***[ISO_ADPLL]***	0x40002548	0x00000003	-
31	Initialize PADPLL PSW (Off)	***[PSW_ADPLL]***	0x40002448	0x00000000	-
32	Initialize 32kHz reference clock in VDD12 Power Domain (Stop)	***[CG_ON_REFCLK]***	0x40000148	0xffffffff	-
33	Initialize rtchv reset (assert)	***[SRST_ON_PA]***	0x40002020	0xffffffff	-
	-	Wait 100us	-	-	-
34	Initialize rtchv clock (stop)	***[CG_ON_PA]***	0x40002000	0xffffffff	-
	-	Wait 100us	-	-	-
35	Initialize CSM_RTC (OSC32K)	***[CSM_RTC]***	0x40002080	0x00000000	-
36	Initialize 32kHz clock source (stop)	***[CONFIG_OSC32K]***	0x40002100	0x00000000	-
	-	***[CONFIG_SiOSC32K]***	0x40002104	0x00000000	-
37	Initialize Hard macro settings	***[SELECT_EFUSE]***	0x400005c0	0x00000000	-
	-	***[OVERRIDE_EFUSE_OSC12M]***	0x40000580	0x00000000	-
	-	***[OVERRIDE_EFUSE_OSC32K]***	0x40002180	0x00000000	-

	-	***[OVERRIDE_EFUSE_SiOSC32K]***	0x40002184	0x00000000	-
	-	***[OVERRIDE_EFUSE_BGR_0]***	0x40002190	0x00000000	-
	-	***[OVERRIDE_EFUSE_BGR_1]***	0x40002194	0x00000000	-
	-	***[CONFIG_DCDC_LVREG_1]***	0x40000528	0x00000000	-
	-	***[CONFIG_SiOSC4M]***	0x40002108	0x00000011	-
	-	***[OVERRIDE_EFUSE_SiOSC4M]***	0x40002188	0x00000000	-
	-	***[CONFIG_SiOSC4M]***	0x40002108	0x00000001	-
38	Initialize the other PMU registers	***[DCG_POWERDOMAIN]***	0x40000010	0x00000000	-
	-	***[CLKREQ_CONFIG_PE]***	0x40000290	0x00020002	-
	-	***[POWERDOMAIN_CTRL_MODE_FOR_WAIT]***	0x40000720	0xffffffff	-
	-	***[POWERDOMAIN_CTRL_MODE_FOR_WRET]***	0x40000724	0x00a8abf8	-
	-	***[POWERDOMAIN_CTRL_MODE_FOR_RET]***	0x40000728	0x00a8aaa8	-
	-	***[POWERMODE_SLEEP_CG_ON]***	0x40000780	0x00000000	-
	-	***[POWERMODE_SLEEP_PRESCAL]***	0x40000790	0x00000000	-
	-	***[RTCLV_RSYNC_SETTING]***	0x400020c0	0x00000000	-
	-	***[BROWNOUTMODE]***	0x40002210	0x00000000	-
	-	***[IRQ_SETTING_0]***	0x40002700	0x00000000	-
	-	***[IRQ_SETTING_1]***	0x40002704	0x00000000	-
	-	***[IRQ_STATUS]***	0x40002708	0xffffffff	-
	-	***[WAKEUP_EN]***	0x4000270c	0x00000000	-
	-	***[CTRL_MODETRAN]***	0x40000400	0x00000000	-

6. Details of Registers

6.1. ITM_STIM

ITM_STIM			
Description	Stimulus Port registers		
Address Region	cm4	**Type:**	RW
Offset	0x0 0000-		
Physical address View0	0xE000 0000- 0xE000 007C		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	STIMULUS	Write: STIMULUS[31:0] Data write to the stimulus port FIFO, for forwarding as a software event packet Read: FIFOREADY[0] Indicates whether the stimulus port FIFO can accept data. 0: Stimulus port FIFO full, or port disabled. 1: Stimulus port FIFO can accept at least one word. This bit is UNKNOWN after a Power-on reset.	RW modify	-

6.2. ITM_TER

ITM_TER			
Description	Trace Enable Register		
Address Region	cm4	**Type:**	RW
Offset	0x0 0E00		
Physical address View0	0xE000 0E00		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	STIMENA	For bit STIMENA[n], in register ITM_TER: 0 = Stimulus port (n) disabled 1 = Stimulus port (n) enabled	RW modify	0x0000 0000

6.3. ITM_TPR

ITM_TPR			
Description	ITM Trace Privilege Register		
Address Region	cm4	**Type:**	RW
Offset	0x0 0E40		
Physical address View0	0xE000 0E40		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**

31:4	Reserved	-	-	-
3:0	PRIVMASK	Bit mask to enable tracing on ITM stimulus ports: bit [0] = stimulus ports [7:0] bit [1] = stimulus ports [15:8] bit [2] = stimulus ports [23:16] bit [3] = stimulus ports [31:24].	RW modify	0x0

6.4. ITM_TCR

ITM_TCR			
Description	Trace Control Register		
Address Region	cm4	**Type:**	RW
Offset	0x0 0E80		
Physical address View0	0xE000 0E80		
Physical address View1	-		

Bit field Details

Bits	Name	Description	Access	Reset
31:24	Reserved	-	-	-
23	BUSY	Indicates whether the ITM is currently processing events: 0: ITM is not processing any events. 1: ITM events present and being drained.	RO	0
22:16	TraceBusID	Identifier for multi-source trace stream formatting. If multi-source trace is in use, the debugger must write a non-zero value to this field. On a Power-on reset, the value of this field is UNKNOWN.	RW modify	0x00
15:12	Reserved	-	-	-
11:10	GTSFREQ	Global timestamp frequency. Defines how often the ITM generates a global timestamp, based on the global timestamp clock frequency, or disables generation of global timestamps. The possible values are: 0b00: Disable generation of global timestamps. 0b01: Generate timestamp request whenever the ITM detects a change in global timestamp counter bits [47:7]. This is approximately every 128 cycles. 0b10: Generate timestamp request whenever the ITM detects a change in global timestamp counter bits [47:13]. This is approximately every 8192 cycles. 0b11: Generate a timestamp after every packet, if the output FIFO is empty. A Power-on reset clears this field to zero. If the implementation does not support global timestamping then these bits are reserved, RAZ/WI.	RW	0b00
9:8	TSPrescale	Local timestamp prescaler, used with the trace packet reference clock. The	RW	0b00

		possible values are: 0b00: No prescaling. 0b01: Divide by 4. 0b10: Divide by 16. 0b11: Divide by 64. If implemented, a Power-on reset clears this field to zero. If the processor does not implement the timestamp prescaler then these bits are reserved, RAZ/WI.		
7:5	Reserved	-	-	-
4	SWOENA	Enables asynchronous clocking of the time stamp counter: 0: Time stamp counter uses the processor system clock. 1: Time stamp counter uses asynchronous clock from the TPIU interface. The time stamp counter is held in reset while the output line is idle. Which clocking modes are implemented is IMPLEMENTATION DEFINED. If the implementation does not support both modes this bit is either RAZ or RAO, to indicate the implemented mode. When this is a RW bit, on a Power-on reset, the value of this bit is UNKNOWN	RW	0
3	TXENA	Enables forwarding of hardware event packet from the DWT unit to the TPIU: 0 = Disabled. 1 = Enabled. A Power-on reset clears this bit to 0.	RW	0
2	SYNCENA	Enables Synchronization packet transmission for a synchronous TPIU: 0: Disabled. 1: Enabled. A Power-on reset clears this bit to 0. Note If a debugger sets this bit to 1 it must also configure DWT_CTRL.SYNCTAP for the correct synchronization speed, see Control register	RW	0
1	TSENA	Enables Local timestamp generation: 0: Disabled. 1: Enabled. A Power-on reset clears this bit to 0.	RW	0
0	ITMENA	Enables the ITM: 0: Disabled. 1: Enabled. This is the master enable for the ITM block. A debugger must set this bit to 1 to permit writes to all Stimulus Port registers. A Power-on reset clears this bit to 0.	RW	0

6.5. ITM_PID4

ITM_PID4				
Description	ITM components Peripheral ID4			
Address Region	cm4	**Type:**	RO	
Offset	0x0 0FD0			
Physical address View0	0xE000 0FD0			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	ITM_PID4	Peripheral ID4	RO	0x0000 0004

6.6. ITM_PID5

ITM_PID5				
Description	ITM components Peripheral ID5			
Address Region	cm4	**Type:**	RO	
Offset	0x0 0FD4			
Physical address View0	0xE000 0FD4			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	ITM_PID5	Peripheral ID5	RO	0x0000 0000

6.7. ITM_PID6

ITM_PID6				
Description	ITM components Peripheral ID6			
Address Region	cm4	**Type:**	RO	
Offset	0x0 0FD8			
Physical address View0	0xE000 0FD8			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	ITM_PID6	Peripheral ID6	RO	0x0000 0000

6.8. ITM_PID7

ITM_PID7				
Description	ITM components Peripheral ID7			
Address Region	cm4	**Type:**	RO	
Offset	0x0 0FDC			
Physical address View0	0xE000 0FDC			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	ITM_PID7	Peripheral ID7	RO	0x0000 0000

6.9. ITM_PID0

ITM_PID0				
Description	ITM components Peripheral ID0			
Address Region	cm4	**Type:**	RO	
Offset	0x0 0FE0			
Physical address View0	0xE000 0FE0			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	ITM_PID0	Peripheral ID0	RO	0x0000 0001

6.10. ITM_PID1

ITM_PID1				
Description	ITM components Peripheral ID1			
Address Region	cm4	**Type:**	RO	
Offset	0x0 0FE4			
Physical address View0	0xE000 0FE4			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	ITM_PID1	Peripheral ID1	RO	0x0000 00B0

6.11. ITM_PID2

ITM_PID2				
Description	ITM components Peripheral ID2			
Address Region	cm4	**Type:**	RO	
Offset	0x0 0FE8			
Physical address View0	0xE000 0FE8			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	ITM_PID2	Peripheral ID2	RO	0x0000 003B

6.12. ITM_PID3

ITM_PID3				
Description	ITM components Peripheral ID3			
Address Region	cm4	**Type:**	RO	
Offset	0x0 0FEC			
Physical address View0	0xE000 0FEC			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	ITM_PID3	Peripheral ID3	RO	0x0000 0000

6.13. ITM_CID0

ITM_CID0				
Description	ITM components Component ID0			
Address Region	cm4	**Type:**	RO	
Offset	0x0 0FF0			
Physical address View0	0xE000 0FF0			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	ITM_CID0	Component ID0	RO	0x0000 000D

6.14. ITM_CID1

ITM_CID1			
Description	ITM components Component ID1		
Address Region	cm4	**Type:**	RO
Offset	0x0 0FF4		
Physical address View0	0xE000 0FF4		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	ITM_CID1	Component ID1	RO	0x0000 00E0

6.15. ITM_CID2

ITM_CID2			
Description	ITM components Component ID2		
Address Region	cm4	**Type:**	RO
Offset	0x0 0FF8		
Physical address View0	0xE000 0FF8		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	ITM_CID2	Component ID2	RO	0x0000 0005

6.16. ITM_CID3

ITM_CID3			
Description	ITM components Component ID3		
Address Region	cm4	**Type:**	RO
Offset	0x0 0FFC		
Physical address View0	0xE000 0FFC		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	ITM_CID3	Component ID3	RO	0x0000 00B1

6.17. DWT_CTRL

DWT_CTRL			
Description	Control Register		
Address Region	cm4	**Type:**	RW
Offset	0x0 1000		
Physical address View0	0xE000 1000		
Physical address View1	-		

Bit field Details

Bits	Name	Description	Access	Reset
31:28	NUMCOMP	Number of comparators implemented. A value of zero indicates no comparator support.	RO	0x4
27	NOTRCPKT	Shows whether the implementation supports trace sampling and exception tracing: 0 = Trace sampling and exception tracing supported. 1 = Trace sampling and exception tracing not supported. If this bit is RAZ, the NOCYCCNT bit must also RAZ.	RO	0
26	NOEXTTRIG	Shows whether the implementation includes external match signals, CMPMATCH[N]: 0 = CMPMATCH[N] supported. 1 = CMPMATCH[N] not supported.	RO	0
25	NOCYCCNT	Shows whether the implementation supports a cycle counter: 0 = Cycle counter supported. 1 = Cycle counter not supported.	RO	0
24	NOPRFCNT	Shows whether the implementation supports the profiling counters: 0 = Supported. 1 = Not supported.	RO	0
23	Reserved	-	-	-
22	CYCEVTENA	Enables POSTCNT underflow Event counter packets generation: 0 = No POSTCNT underflow packets generated. 1 = POSTCNT underflow packets generated, if PCSAMPLENA set to 0. This bit is UNK/SBZP if the NOTRCPKT bit is RAO or the NOCYCCNT bit is RAO.	RW modify	0
21	FOLDEVTENA	Enables generation of the Folded-instruction counter overflow event: 0 = Disabled. 1 = Enabled. This bit is UNK/SBZP if the NOPRFCNT bit is RAO.	RW modify	0
20	LSUEVTENA	Enables generation of the LSU counter overflow event. 0 = Disabled. 1 = Enabled. This bit is UNK/SBZP if the NOPRFCNT bit is RAO.	RW modify	0

19	SLEEPEVTENA	Enables generation of the Sleep counter overflow event. 0 = Disabled. 1 = Enabled. This bit is UNK/SBZP if the NOPRFCNT bit is RAO.	RW modify	0
18	EXCEVTENA	Enables generation of the Exception overhead counter overflow event: 0 = Disabled. 1 = Enabled. This bit is UNK/SBZP if the NOPRFCNT bit is RAO.	RW modify	0
17	CPIEVTENA	Enables generation of the CPI counter overflow event: 0 = Disabled. 1 = Enabled. This bit is UNK/SBZP if the NOPRFCNT bit is RAO.	RW modify	0
16	EXCTRCENA	Enables generation of exception trace: 0 = Disabled. 1 = Enabled. This bit is UNK/SBZP if the NOTRCPKT bit is RAO.	RW modify	0
15:13	Reserved	-	-	-
12	PCSAMPLENA	Enables use of POSTCNT counter as a timer for Periodic PC sample packet generation: 0 = No Periodic PC sample packets generated. 1 = Periodic PC sample packets generated. This bit is UNK/SBZP if the NOTRCPKT bit is RAO or the NOCYCCNT bit is RAO.	RW modify	0
11:10	SYNCTAP	Selects the position of the synchronization packet counter tap on the CYCCNT counter. This determines the Synchronization packet rate: 0b00 = Disabled. No Synchronization packets. 0b01 = Synchronization counter tap at CYCCNT[24] 0b10 = Synchronization counter tap at CYCCNT[26] 0b11 = Synchronization counter tap at CYCCNT[28] This field is UNK/SBZP if the NOCYCCNT bit is RAO.	RW modify	0b00
9	CYCTAP	Selects the position of the POSTCNT tap on the CYCCNT counter: 0 = POSTCNT tap at CYCCNT[6] 1 = POSTCNT tap at CYCCNT[10] This bit is UNK/SBZP if the NOCYCCNT bit is RAO.	RW modify	0
8:5	POSTINIT	Initial value for the POSTCNT counter. This field is UNK/SBZP if the NOCYCCNT bit is RAO. Note This field was previously called POSTCNT. The changed name gives a better indication of its function.	RW modify	0x0
4:1	POSTPRESET	Reload value for the POSTCNT	RW	0x0

		counter. This field is UNK/SBZP if the NOCYCCNT bit is RAO.	modify	
0	CYCCNTENA	Enables CYCCNT: 0 = Disabled 1 = Enabled This bit is UNK/SBZP if the NOCYCCNT bit is RAO.	RW modify	0

6.18. DWT_CYCCNT

DWT_CYCCNT			
Description	Cycle Count Register		
Address Region	cm4	**Type:**	RW
Offset	0x0 1004		
Physical address View0	0xE000 1004		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	CYCCNT	Incrementing cycle counter value. When enabled, CYCCNT increments on each processor clock cycle. On overflow, CYCCNT wraps to zero.	RW modify	0x0000 0000

6.19. DWT_CPICNT

DWT_CPICNT			
Description	CPI Count Register		
Address Region	cm4	**Type:**	RW
Offset	0x0 1008		
Physical address View0	0xE000 1008		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:0	CPICNT	The base CPI counter. Counts additional cycles required to execute multi-cycle instructions, except those recorded by DWT_LSUCNT, and counts any instruction fetch stalls.	RW modify	-

6.20. DWT_EXCCNT

DWT_EXCCNT			
Description	Exception Overhead Count Register		
Address Region	cm4	**Type:**	RW
Offset	0x0 100C		
Physical address View0	0xE000 100C		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:0	EXCCNT	The exception overhead counter. Counts the total cycles spent in exception processing.	RW modify	-

6.21. DWT_SLEEPCNT

DWT_SLEEPCNT			
Description	Sleep Count Register		
Address Region	cm4	**Type:**	RW
Offset	0x0 1010		
Physical address View0	0xE000 1010		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:0	SLEEPCNT	Sleep counter. Counts the total number of cycles that the processor is sleeping.	RW modify	-

6.22. DWT_LSUCNT

DWT_LSUCNT			
Description	LSU Count Register		
Address Region	cm4	**Type:**	RW
Offset	0x0 1014		
Physical address View0	0xE000 1014		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:0	LSUCNT	Load-store counter. Increments on any additional cycles required to execute load or store instructions.	RW modify	-

6.23. DWT_FOLDCNT

DWT_FOLDCNT			
Description	Folded-instruction Count Register		
Address Region	cm4	**Type:**	RW
Offset	0x0 1018		
Physical address View0	0xE000 1018		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:0	FOLDCNT	Folded-instruction counter. Increments on each instruction that takes 0 cycles.	RW modify	-

6.24. DWT_PCSR

DWT_PCSR			
Description	Program Counter Sample Register		
Address Region	cm4	**Type:**	RW
Offset	0x0 101C		
Physical address View0	0xE000 101C		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	EIASAMPLE	Executed Instruction Address sample value	RW modify	-

6.25. DWT_COMP0

DWT_COMP0			
Description	Comparator Register0		
Address Region	cm4	**Type:**	RW
Offset	0x0 1020		
Physical address View0	0xE000 1020		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	COMP	Reference value for comparison.	RW modify	-

6.26. DWT_MASK0

DWT_MASK0					
Description	Mask Register0				
Address Region	cm4		**Type:**	RW	
Offset	0x0 1024				
Physical address View0	0xE000 1024				
Physical address View1	-				
Bit field Details					
Bits	**Name**	**Description**		**Access**	**Reset**
31:5	Reserved	-		-	-
4:0	MASK	The size of the ignore mask, 0-31 bits, applied to address range matching. The maximum mask size is IMPLEMENTATION DEFINED. A debugger can write 0b11111 to this field and then read the register back to determine the maximum mask size supported.		RW modify	-

6.27. DWT_FUNCTION0

DWT_FUNCTION0					
Description	Function Register0				
Address Region	cm4		**Type:**	RW	
Offset	0x0 1028				
Physical address View0	0xE000 1028				
Physical address View1	-				
Bit field Details					
Bits	**Name**	**Description**		**Access**	**Reset**
31:25	Reserved	-		-	-
24	MATCHED	Comparator match: 0 = No match. 1 = Match. A value of 1 indicates that the operation defined by the FUNCTION field occurred since the last read of the register Reading the register clears this bit to 0.		RW modify	0
23:20	Reserved	-		-	-
19:16	DATAVADDR1	When the DATAVMATCH and LNK1ENA bits are both 1, this field can hold the comparator number of a second comparator to use for linked address comparison. The DWT unit ignores the value of this field unless the LNK1ENA bit is RAO and the DATAVMATCH bit is set to 1.If LNK1ENA is RAZ, this field is RAZ/WI.		RW modify	0x0
15:12	DATAVADDR0	When the DATAVMATCH bit is set to 1 this field can hold the comparator number of a comparator to use for linked address comparison. The DWT unit ignores the value of this field if the DATAVMATCH bit is set to 0.		RW modify	0x0

11:10	DATAVSIZE	For data value matching, specifies the size of the required data comparison: 0b00 = Byte 0b01 = Half word 0b10 = Word. The value 0b11 is reserved. Using this value means behavior is UNPREDICTABLE.	RW modify	0b00
9	LNK1ENA	Indicates whether the implementation supports use of a second linked comparator: 0 = Second linked comparator not supported. 1 = Second linked comparator supported. When LNK1ENA is RAO, the DATAVADDR1 field specifies the comparator to use as the second linked comparator.	RW modify	0
8	DATAVMATCH	Enables data value comparison, if supported: 0 = Perform address comparison. 1 = Perform data value comparison. For comparator 0, when the CYCMATCH is set to 1, DATAVMATCH must be set to 0 for it to perform cycle count comparison. If the implementation does not support data value comparison this bit is RAZ/WI.	RW modify	0
7	CYCMATCH	DWT_FUNCTION0 only. If the implementation supports cycle counting, enable cycle count comparison for comparator 0: 0 = No comparison is performed. 1 = Compare DWT_COMP0 with the cycle counter, DWT_CYCCNT. If DWT_CTRL.NOCYCCNT is RAZ then this bit is UNK/SBZP.	RW modify	0
6	Reserved	-	-	-
5	EMITRANGE	If the implementation supports trace sampling, enables generation of Data trace address offset packets, that hold Daddr[15:0]: 0 = Data trace address offset packets disabled 1 = Enable Data trace address offset packet generation. If DWT_CTRL.NOTRCPKT is RAZ then this bit is UNK/SBZP.	RW modify	0
4	Reserved	-	-	-
3:0	FUNCTION	Selects action taken on comparator match: 0b0000 = Disabled or LinkAddr() This field resets to zero.	RW modify	0x0

6.28. DWT_COMP1

DWT_COMP1			
Description	Comparator Register1		
Address Region	cm4	**Type:**	RW
Offset	0x0 1030		
Physical address View0	0xE000 1030		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	COMP	Reference value for comparison.	RW modify	-

6.29. DWT_MASK1

DWT_MASK1			
Description	Mask Register1		
Address Region	cm4	**Type:**	RW
Offset	0x0 1034		
Physical address View0	0xE000 1034		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:5	Reserved	-	-	-
4:0	MASK	The size of the ignore mask, 0-31 bits	RW modify	-

6.30. DWT_FUNCTION1

DWT_FUNCTION1			
Description	Function Register1		
Address Region	cm4	**Type:**	RW
Offset	0x0 1038		
Physical address View0	0xE000 1038		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:25	Reserved	-	-	-
24	MATCHED		RW modify	0
23:20	Reserved	-	-	-
19:16	DATAVADDR1		RW modify	0x0
15:12	DATAVADDR0		RW modify	0x0
11:10	DATAVSIZE		RW modify	0x0
9	LNK1ENA		RW modify	0

8	DATAVMATCH		RW modify	0
7:6	Reserved	-	-	-
5	EMITRANGE		RW modify	0
4	Reserved	-	-	-
3:0	FUNCTION		RW modify	0x0

6.31. DWT_COMP2

DWT_COMP2				
Description	Comparator Register2			
Address Region	cm4	**Type:**	RW	
Offset	0x0 1040			
Physical address View0	0xE000 1040			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	COMP	Reference value for comparison.	RW modify	-

6.32. DWT_MASK2

DWT_MASK2				
Description	Mask Register2			
Address Region	cm4	**Type:**	RW	
Offset	0x0 1044			
Physical address View0	0xE000 1044			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:5	Reserved	-	-	-
4:0	MASK	The size of the ignore mask, 0-31 bits	RW modify	-

6.33. DWT_FUNCTION2

DWT_FUNCTION2				
Description	Function Register2			
Address Region	cm4	**Type:**	RW	
Offset	0x0 1048			
Physical address View0	0xE000 1048			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:25	Reserved	-	-	-
24	MATCHED		RW	0

			modify	
23:20	Reserved	-	-	-
19:16	DATAVADDR1		RW modify	0x0
15:12	DATAVADDR0		RW modify	0x0
11:10	DATAVSIZE		RW modify	0b00
9	LNK1ENA		RW modify	0
8	DATAVMATCH		RW modify	0
7:6	Reserved	-	-	-
5	EMITRANGE		RW modify	0
4	Reserved	-	-	-
3:0	FUNCTION		RW modify	0x0

6.34. DWT_COMP3

DWT_COMP3			
Description	Comparator Register3		
Address Region	cm4	**Type:**	RW
Offset	0x0 1050		
Physical address View0	0xE000 1050		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	COMP	Reference value for comparison.	RW modify	-

6.35. DWT_MASK3

DWT_MASK3			
Description	Mask Register3		
Address Region	cm4	**Type:**	RW
Offset	0x0 1054		
Physical address View0	0xE000 1054		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:5	Reserved	-	-	-
4:0	MASK	The size of the ignore mask, 0-31 bits	RW modify	-

6.36. DWT_FUNCTION3

DWT_FUNCTION3			
Description	Function Register3		
Address Region	cm4	**Type:**	RW
Offset	0x0 1058		
Physical address View0	0xE000 1058		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:25	Reserved	-	-	-
24	MATCHED		RW modify	0
23:20	Reserved	-	-	-
19:16	DATAVADDR1		RW modify	0x0
15:12	DATAVADDR0		RW modify	0x0
11:10	DATAVSIZE		RW modify	0b00
9	LNK1ENA		RW modify	0
8	DATAVMATCH		RW modify	0
7:6	Reserved	-	-	-
5	EMITRANGE		RW modify	0
4	Reserved	-	-	-
3:0	FUNCTION		RW modify	0x0

6.37. DWT_PID4

DWT_PID4			
Description	DWT components Peripheral ID4		
Address Region	cm4	**Type:**	RO
Offset	0x0 1FD0		
Physical address View0	0xE000 1FD0		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	DWT_PID4	Peripheral ID4	RO	0x0000 0004

6.38. DWT_PID5

DWT_PID5				
Description	DWT components Peripheral ID5			
Address Region	cm4	**Type:**	RO	
Offset	0x0 1FD4			
Physical address View0	0xE000 1FD4			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	DWT_PID5	Peripheral ID5	RO	0x0000 0000

6.39. DWT_PID6

DWT_PID6				
Description	DWT components Peripheral ID6			
Address Region	cm4	**Type:**	RO	
Offset	0x0 1FD8			
Physical address View0	0xE000 1FD8			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	DWT_PID6	Peripheral ID6	RO	0x0000 0000

6.40. DWT_PID7

DWT_PID7				
Description	DWT components Peripheral ID7			
Address Region	cm4	**Type:**	RO	
Offset	0x0 1FDC			
Physical address View0	0xE000 1FDC			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	DWT_PID7	Peripheral ID7	RO	0x0000 0000

6.41. DWT_PID0

DWT_PID0				
Description	DWT components Peripheral ID0			
Address Region	cm4	**Type:**	RO	
Offset	0x0 1FE0			
Physical address View0	0xE000 1FE0			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	DWT_PID0	Peripheral ID0	RO	0x0000 0002

6.42. DWT_PID1

DWT_PID1				
Description	DWT components Peripheral ID1			
Address Region	cm4	**Type:**	RO	
Offset	0x0 1FE4			
Physical address View0	0xE000 1FE4			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	DWT_PID1	Peripheral ID1	RO	0x0000 00B0

6.43. DWT_PID2

DWT_PID2				
Description	DWT components Peripheral ID2			
Address Region	cm4	**Type:**	RO	
Offset	0x0 1FE8			
Physical address View0	0xE000 1FE8			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	DWT_PID2	Peripheral ID2	RO	0x0000 003B

6.44. DWT_PID3

DWT_PID3				
Description	DWT components Peripheral ID3			
Address Region	cm4	**Type:**	RO	
Offset	0x0 1FEC			
Physical address View0	0xE000 1FEC			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	DWT_PID3	Peripheral ID3	RO	0x0000 0000

6.45. DWT_CID0

DWT_CID0				
Description	DWT components Component ID0			
Address Region	cm4	**Type:**	RO	
Offset	0x0 1FF0			
Physical address View0	0xE000 1FF0			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	DWT_CID0	Component ID0	RO	0x0000 000D

6.46. DWT_CID1

DWT_CID1				
Description	DWT components Component ID1			
Address Region	cm4	**Type:**	RO	
Offset	0x0 1FF4			
Physical address View0	0xE000 1FF4			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	DWT_CID1	Component ID1	RO	0x0000 00E0

6.47. DWT_CID2

DWT_CID2				
Description	DWT components Component ID2			
Address Region	cm4	**Type:**	RO	
Offset	0x0 1FF8			
Physical address View0	0xE000 1FF8			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	DWT_CID2	Component ID2	RO	0x0000 0005

6.48. DWT_CID3

DWT_CID3				
Description	DWT components Component ID3			
Address Region	cm4	**Type:**	RO	
Offset	0x0 1FFC			
Physical address View0	0xE000 1FFC			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	DWT_CID3	Component ID3	RO	0x0000 00B1

6.49. FP_CTRL

FP_CTRL				
Description	Flash Patch Control Register			
Address Region	cm4	**Type:**	RW	
Offset	0x0 2000			
Physical address View0	0xE000 2000			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:15	Reserved	-	-	-
14:12	NUM_CODE_6_4	The most significant bits of NUM_CODE, the number of instruction address comparators, see bits [7:4].	RO	0b000
11:8	NUM_LIT	The number of literal address comparators supported. If this field is zero, the implementation does not support literal comparators.	RO	0x2
7:4	NUM_CODE_3_0	The least significant bits of NUM_CODE, the number of instruction address comparators. If NUM_CODE[6:0] is zero, the implementation does not support any instruction address comparators.	RO	0x6

3:2	Reserved	-	-	-
1	KEY	On any write to FP_CTRL, the FPB unit ignores the write unless this bit is 1. This bit is RAZ.	RW modify	0
0	ENABLE	Enable bit for the FPB: 0 = FPB disabled 1 = FPB enabled. A Power-on reset clears this bit to 0.	RW modify	0

6.50. FP_REMAP

FP_REMAP			
Description	Flash Patch Remap register		
Address Region	cm4	**Type:**	RW
Offset	0x0 2004		
Physical address View0	0xE000 2004		
Physical address View1	-		

Bit field Details

Bits	Name	Description	Access	Reset
31:30	Reserved	-	-	-
29	RMPSPT	Indicates whether the FPB unit supports flash patch remap: 0 = Remapping not supported. The FPB only supports breakpoint functionality. 1 = Hard-wired remap to SRAM region	RO	-
28:5	COMP	If the FPB supports flash patch remap, this field: • holds bits [28:5] of the base address in SRAM to which the FPB remaps the address • has an UNKNOWN value on reset. If the FPB only supports breakpoint functionality this field is UNK/SBZP.	RW modify	-
4	Reserved	-	-	-
3:0	Reserved	-	-	-

6.51. FP_COMP0

FP_COMP0			
Description	Flash Patch Comparator Register0		
Address Region	cm4	**Type:**	RW
Offset	0x0 2008		
Physical address View0	0xE000 2008		
Physical address View1	-		

Bit field Details

Bits	Name	Description	Access	Reset
31:30	REPLACE	Defines the behavior when the COMP address is matched: 0b00 = Remap to remap address 0b01 = Breakpoint on lower half word, upper is unaffected 0b10 = Breakpoint on upper half word, lower is unaffected 0b11 = Breakpoint on both lower and upper half words. The reset value of this field is UNKNOWN.	RW modify	0b00
29	Reserved	-	-	-
28:2	COMP	Bits [28:2] of the address to compare with addresses from the Code memory region. Bits [31:29] and [1:0] of the address for comparison are zero. If a match occurs: • for an instruction address comparator, the REPLACE field defines the required action • for a literal address comparator, the FPB remaps the access, see Flash Patch Remap register. The reset value of this field is UNKNOWN.	RW modify	0x000 0000
1	Reserved	-	-	-
0	ENABLE	Enable bit for this comparator: 0 = Comparator disabled. 1 = Comparator enabled. A Power-on reset clears this bit to 0.	RW modify	0

6.52. FP_COMP1

FP_COMP1					
Description	Flash Patch Comparator Register1				
Address Region	cm4		**Type:**	RW	
Offset	0x0 200C				
Physical address View0	0xE000 200C				
Physical address View1	-				
Bit field Details					
Bits	**Name**	**Description**		**Access**	**Reset**
31:30	REPLACE	Defines the behavior when the COMP address is matched:		RW modify	0b00
29	Reserved	-		-	-
28:2	COMP	Compare with addresses from the Code memory region.		RW modify	0x000 0000
1	Reserved	-		-	-
0	ENABLE	Enable bit for this comparator:		RW modify	0

6.53. FP_COMP2

FP_COMP2					
Description	Flash Patch Comparator Register2				
Address Region	cm4		**Type:**	RW	
Offset	0x0 2010				
Physical address View0	0xE000 2010				
Physical address View1	-				
Bit field Details					
Bits	**Name**	**Description**		**Access**	**Reset**
31:30	REPLACE	Defines the behavior when the COMP address is matched:		RW modify	0x0
29	Reserved	-		-	-
28:2	COMP	Compare with addresses from the Code memory region.		RW modify	0x000 0000
1	Reserved	-		-	-
0	ENABLE	Enable bit for this comparator:		RW modify	0

6.54. FP_COMP3

FP_COMP3				
Description	Flash Patch Comparator Register3			
Address Region	cm4	**Type:**	RW	
Offset	0x0 2014			
Physical address View0	0xE000 2014			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:30	REPLACE	Defines the behavior when the COMP address is matched:	RW modify	0b00
29	Reserved	-	-	-
28:2	COMP	Compare with addresses from the Code memory region.	RW modify	0x000 0000
1	Reserved	-	-	-
0	ENABLE	Enable bit for this comparator:	RW modify	0

6.55. FP_COMP4

FP_COMP4				
Description	Flash Patch Comparator Register4			
Address Region	cm4	**Type:**	RW	
Offset	0x0 2018			
Physical address View0	0xE000 2018			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:30	REPLACE	Defines the behavior when the COMP address is matched:	RW modify	0b00
29	Reserved	-	-	-
28:2	COMP	Compare with addresses from the Code memory region.	RW modify	0x000 0000
1	Reserved	-	-	-
0	ENABLE	Enable bit for this comparator:	RW modify	0

6.56. FP_COMP5

FP_COMP5			
Description	Flash Patch Comparator Register5		
Address Region	cm4	**Type:**	RW
Offset	0x0 201C		
Physical address View0	0xE000 201C		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:30	REPLACE	Defines the behavior when the COMP address is matched:	RW modify	0b00
29	Reserved	-	-	-
28:2	COMP	Compare with addresses from the Code memory region.	RW modify	0x000 0000
1	Reserved	-	-	-
0	ENABLE	Enable bit for this comparator:	RW modify	0

6.57. FP_COMP6

FP_COMP6			
Description	Flash Patch Comparator Register6		
Address Region	cm4	**Type:**	RW
Offset	0x0 2020		
Physical address View0	0xE000 2020		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:30	REPLACE	Defines the behavior when the COMP address is matched:	RW modify	0b00
29	Reserved	-	-	-
28:2	COMP	Compare with addresses from the Code memory region.	RW modify	0x000 0000
1	Reserved	-	-	-
0	ENABLE	Enable bit for this comparator:	RW modify	0

6.58. FP_COMP7

FP_COMP7			
Description	Flash Patch Comparator Register7		
Address Region	cm4	**Type:**	RW
Offset	0x0 2024		
Physical address View0	0xE000 2024		
Physical address View1	-		

Bit field Details

Bits	Name	Description	Access	Reset
31:30	REPLACE	Defines the behavior when the COMP address is matched:	RW modify	0b00
29	Reserved	-	-	-
28:2	COMP	Compare with addresses from the Code memory region.	RW modify	0x000 0000
1	Reserved	-	-	-
0	ENABLE	Enable bit for this comparator:	RW modify	0

6.59. FP_PID4

FP_PID4			
Description	FP components Peripheral ID4		
Address Region	cm4	**Type:**	RO
Offset	0x0 2FD0		
Physical address View0	0xE000 2FD0		
Physical address View1	-		

Bit field Details

Bits	Name	Description	Access	Reset
31:0	FP_PID4	Peripheral ID4	RO	0x0000 0004

6.60. FP_PID5

FP_PID5			
Description	FP components Peripheral ID5		
Address Region	cm4	**Type:**	RO
Offset	0x0 2FD4		
Physical address View0	0xE000 2FD4		
Physical address View1	-		

Bit field Details

Bits	Name	Description	Access	Reset
31:0	FP_PID5	Peripheral ID5	RO	0x0000 0000

6.61. FP_PID6

FP_PID6				
Description	FP components Peripheral ID6			
Address Region	cm4	**Type:**	RO	
Offset	0x0 2FD8			
Physical address View0	0xE000 2FD8			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	FP_PID6	Peripheral ID6	RO	0x0000 0000

6.62. FP_PID7

FP_PID7				
Description	FP components Peripheral ID7			
Address Region	cm4	**Type:**	RO	
Offset	0x0 2FDC			
Physical address View0	0xE000 2FDC			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	FP_PID7	Peripheral ID7	RO	0x0000 0000

6.63. FP_PID0

FP_PID0				
Description	FP components Peripheral ID0			
Address Region	cm4	**Type:**	RO	
Offset	0x0 2FE0			
Physical address View0	0xE000 2FE0			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	FP_PID0	Peripheral ID0	RO	0x0000 0003

6.64. FP_PID1

FP_PID1				
Description	FP components Peripheral ID1			
Address Region	cm4	**Type:**	RO	
Offset	0x0 2FE4			
Physical address View0	0xE000 2FE4			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	FP_PID1	Peripheral ID1	RO	0x0000 00B0

6.65. FP_PID2

FP_PID2				
Description	FP components Peripheral ID2			
Address Region	cm4	**Type:**	RO	
Offset	0x0 2FE8			
Physical address View0	0xE000 2FE8			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	FP_PID2	Peripheral ID2	RO	0x0000 002B

6.66. FP_PID3

FP_PID3				
Description	FP components Peripheral ID3			
Address Region	cm4	**Type:**	RO	
Offset	0x0 2FEC			
Physical address View0	0xE000 2FEC			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	FP_PID3	Peripheral ID3	RO	0x0000 0000

6.67. FP_CID0

FP_CID0				
Description	FP components Component ID0			
Address Region	cm4	**Type:**	RO	
Offset	0x0 2FF0			
Physical address View0	0xE000 2FF0			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	FP_CID0	Component ID0	RO	0x0000 000D

6.68. FP_CID1

FP_CID1				
Description	FP components Component ID1			
Address Region	cm4	**Type:**	RO	
Offset	0x0 2FF4			
Physical address View0	0xE000 2FF4			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	FP_CID1	Component ID1	RO	0x0000 00E0

6.69. FP_CID2

FP_CID2				
Description	FP components Component ID2			
Address Region	cm4	**Type:**	RO	
Offset	0x0 2FF8			
Physical address View0	0xE000 2FF8			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	FP_CID2	Component ID2	RO	0x0000 0005

6.70. FP_CID3

FP_CID3				
Description	FP components Component ID3			
Address Region	cm4	**Type:**	RO	
Offset	0x0 2FFC			
Physical address View0	0xE000 2FFC			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	FPB_CID3	Component ID3	RO	0x0000 00B1

6.71. ICTR

ICTR				
Description	Interrupt Controller Type Register			
Address Region	cm4	**Type:**	RO	
Offset	0x0 E004			
Physical address View0	0xE000 E004			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:4	Reserved	-	-	-
3:0	INTLINESNUM	Total number of interrupt lines in groups of 32: 0b0000 = 0...32 0b0001 = 33...64 0b0010 = 65...96 0b0011 = 97...128 0b0100 = 129...160 0b0101 = 161...192 0b0110 = 193...224 0b0111 = 225...256	RO	0x2

6.72. ACTLR

ACTLR			
Description	Auxiliary Control Register		
Address Region	cm4	**Type:**	RW
Offset	0x0 E008		
Physical address View0	0xE000 E008		
Physical address View1	-		

Bit field Details

Bits	Name	Description	Access	Reset
31:10	Reserved	-	-	-
9	DISOOFP	Disables floating point instructions completing out of order with respect to integer instructions.	RW modify	0
8	DISFPCA	Disable automatic update of CONTROL.FPCA.	RW modify	0
7:3	Reserved	-	-	-
2	DISFOLD	When set to 1, disables IT folding.	RW modify	0
1	DISDEFWBUF	When set to 1, disables write buffer use during default memory map accesses. This causes all Bus Faults to be precise Bus Faults but decreases performance because any store to memory must complete before the processor can execute the next instruction.	RW modify	0
0	DISMCYCINT	When set to 1, disables interruption of load multiple and store multiple instructions. This increases the interrupt latency of the processor because any LDM or STM must complete before the processor can stack the current state and enter the interrupt handler.	RW modify	0

6.73. SYST_CSR

SYST_CSR			
Description	SysTick Control and Status Register		
Address Region	cm4	**Type:**	RW
Offset	0x0 E010		
Physical address View0	0xE000 E010		
Physical address View1	-		

Bit field Details

Bits	Name	Description	Access	Reset
31:17	Reserved	-	-	-
16	COUNTFLAG	Returns 1 if timer counted to 0 since last time this was read.	RW modify	0
15:3	Reserved	-	-	-
2	CLKSOURCE	Indicates the clock source: 0 = external clock 1 = processor clock	RW modify	1
1	TICKINT	Enables SysTick exception request: 0 = counting down to zero does not assert the SysTick exception request 1 = counting down to zero to asserts the SysTick exception request. Software can use COUNTFLAG to determine if SysTick has ever counted to zero.	RW modify	0
0	ENABLE	Enables the counter: 0 = counter disabled 1 = counter enabled.	RW modify	0

6.74. SYST_RVR

SYST_RVR			
Description	SysTick Reload Value Register		
Address Region	cm4	**Type:**	RW
Offset	0x0 E014		
Physical address View0	0xE000 E014		
Physical address View1	-		

Bit field Details

Bits	Name	Description	Access	Reset
31:24	Reserved	-	-	-
23:0	RELOAD	Value to load into the SYST_CVR register when the counter is enabled and when it reaches 0	RW modify	-

6.75. SYST_CVR

SYST_CVR			
Description	SysTick Current Value Register		
Address Region	cm4	**Type:**	RW
Offset	0x0 E018		
Physical address View0	0xE000 E018		
Physical address View1	-		

Bit field Details

Bits	Name	Description	Access	Reset
31:24	Reserved	-	-	-
23:0	CURRENT	Reads return the current value of the SysTick counter. A write of any value clears the field to 0, and also clears the SYST_CSR COUNTFLAG bit to 0.	RW modify	-

6.76. SYST_CALIB

SYST_CALIB			
Description	SysTick Calibration Value Register		
Address Region	cm4	**Type:**	RO
Offset	0x0 E01C		
Physical address View0	0xE000 E01C		
Physical address View1	-		

Bit field Details

Bits	Name	Description	Access	Reset
31	NOREF	Indicates whether the device provides a reference clock to the processor: 0 = reference clock provided 1 = no reference clock provided. If your device does not provide a reference clock, the SYST_CSR.CLKSOURCE bit reads-as-one and ignores writes.	RO	1
30	SKEW	Indicates whether the TENMS value is exact: 0 = TENMS value is exact 1 = TENMS value is inexact, or not given. An inexact TENMS value can affect the suitability of SysTick as a software real time clock.	RO	1
29:24	Reserved	-	-	-
23:0	TENMS	Reload value for 10ms (100Hz) timing, subject to system clock skew errors. If the value reads as zero, the calibration value is not known.	RO	0x00 0000

6.77. NVIC_ISER0

NVIC_ISER0			
Description	Interrupt Set-enable Register 0		
Address Region	cm4	**Type:**	RW
Offset	0x0 E100		
Physical address View0	0xE000 E100		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	SETENA	Interrupt set-enable bits. Write: 0 = no effect 1 = enable interrupt. Read: 0 = interrupt disabled 1 = interrupt enabled.	RW modify	0x0000 0000

6.78. NVIC_ISER1

NVIC_ISER1			
Description	Interrupt Set-enable Register 1		
Address Region	cm4	**Type:**	RW
Offset	0x0 E104		
Physical address View0	0xE000 E104		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	SETENA	Interrupt set-enable bits.	RW modify	0x0000 0000

6.79. NVIC_ISER2

NVIC_ISER2			
Description	Interrupt Set-enable Register 2		
Address Region	cm4	**Type:**	RW
Offset	0x0 E108		
Physical address View0	0xE000 E108		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:16	Reserved	-	-	-
15:0	SETENA	Interrupt set-enable bits.	RW modify	0x0000

6.80. NVIC_ICER0

NVIC_ICER0			
Description	Interrupt Clear-enable Register 0		
Address Region	cm4	**Type:**	RW
Offset	0x0 E180		
Physical address View0	0xE000 E180		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	CLRENA	Interrupt clear-enable bits. Write: 0 = no effect 1 = disable interrupt. Read: 0 = interrupt disabled 1 = interrupt enabled.	RW modify	0x0000 0000

6.81. NVIC_ICER1

NVIC_ICER1			
Description	Interrupt Clear-enable Register 1		
Address Region	cm4	**Type:**	RW
Offset	0x0 E184		
Physical address View0	0xE000 E184		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	CLRENA	Interrupt Clear-enable bits.	RW modify	0x0000 0000

6.82. NVIC_ICER2

NVIC_ICER2			
Description	Interrupt Clear-enable Register 2		
Address Region	cm4	**Type:**	RW
Offset	0x0 E188		
Physical address View0	0xE000 E188		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:16	Reserved	-	-	-
15:0	Reserved	-	-	-

6.83. NVIC_ISPR0

NVIC_ISPR0				
Description	Interrupt Set-pending Register 0			
Address Region	cm4	**Type:**	RW	
Offset	0x0 E200			
Physical address View0	0xE000 E200			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	SETPEND	Interrupt set-pending bits. Write: 0 = no effect 1 = changes interrupt state to pending. Read: 0 = interrupt is not pending 1 = interrupt is pending.	RW modify	0x0000 0000

6.84. NVIC_ISPR1

NVIC_ISPR1				
Description	Interrupt Set-pending Register 1			
Address Region	cm4	**Type:**	RW	
Offset	0x0 E204			
Physical address View0	0xE000 E204			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	SETPEND	Interrupt set-pending bits.	RW modify	0x0000 0000

6.85. NVIC_ISPR2

NVIC_ISPR2				
Description	Interrupt Set-pending Register 2			
Address Region	cm4	**Type:**	RW	
Offset	0x0 E208			
Physical address View0	0xE000 E208			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:16	Reserved	-	-	-
15:0	SETPEND	Interrupt set-pending bits.	RW modify	0x0000

6.86. NVIC_ICPR0

NVIC_ICPR0					
Description	Interrupt Clear-pending Register 0				
Address Region	cm4		**Type:**	RW	
Offset	0x0 E280				
Physical address View0	0xE000 E280				
Physical address View1	-				
Bit field Details					
Bits	**Name**	**Description**		**Access**	**Reset**
31:0	CLRPEND	Interrupt clear-pending bits. Write: 0 = no effect 1 = removes pending state an interrupt. Read: 0 = interrupt is not pending 1 = interrupt is pending.		RW modify	0x0000 0000

6.87. NVIC_ICPR1

NVIC_ICPR1					
Description	Interrupt Clear-pending Register 1				
Address Region	cm4		**Type:**	RW	
Offset	0x0 E284				
Physical address View0	0xE000 E284				
Physical address View1	-				
Bit field Details					
Bits	**Name**	**Description**		**Access**	**Reset**
31:0	CLRPEND	Interrupt Clear-pending bits.		RW modify	0x0000 0000

6.88. NVIC_ICPR2

NVIC_ICPR2					
Description	Interrupt Clear-pending Register 2				
Address Region	cm4		**Type:**	RW	
Offset	0x0 E288				
Physical address View0	0xE000 E288				
Physical address View1	-				
Bit field Details					
Bits	**Name**	**Description**		**Access**	**Reset**
31:16	Reserved	-		-	-
15:0	CLRPEND	Interrupt Clear-pending bits.		RW modify	0x0000

6.89. NVIC_IABR0

NVIC_IABR0				
Description	Interrupt Active Bit Register 0			
Address Region	cm4	**Type:**	RO	
Offset	0x0 E300			
Physical address View0	0xE000 E300			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	ACTIVE	Interrupt active flags: 0 = interrupt not active 1 = interrupt active.	RO	0x0000 0000

6.90. NVIC_IABR1

NVIC_IABR1				
Description	Interrupt Active Bit Register 1			
Address Region	cm4	**Type:**	RO	
Offset	0x0 E304			
Physical address View0	0xE000 E304			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	ACTIVE	Interrupt Active Bit bits.	RO	0x0000 0000

6.91. NVIC_IABR2

NVIC_IABR2				
Description	Interrupt Active Bit Register 2			
Address Region	cm4	**Type:**	RO	
Offset	0x0 E308			
Physical address View0	0xE000 E308			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:16	Reserved	-	-	-
15:0	ACTIVE	Interrupt Active Bit bits.	RO	0x0000

6.92. NVIC_IPR0

NVIC_IPR0			
Description	Interrupt Priority Register 0		
Address Region	cm4	**Type:**	RW
Offset	0x0 E400		
Physical address View0	0xE000 E400		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:24	PRI_3	Each priority field holds a priority value, 0-255. The lower the value, the greater the priority of the corresponding interrupt.	RW modify	0x00
23:16	PRI_2	Each priority field holds a priority value, 0-255. The lower the value, the greater the priority of the corresponding interrupt.	RW modify	0x00
15:8	PRI_1	Each priority field holds a priority value, 0-255. The lower the value, the greater the priority of the corresponding interrupt.	RW modify	0x00
7:0	PRI_0	Each priority field holds a priority value, 0-255. The lower the value, the greater the priority of the corresponding interrupt.	RW modify	0x00

6.93. NVIC_IPR1

NVIC_IPR1			
Description	Interrupt Priority Register 1		
Address Region	cm4	**Type:**	RW
Offset	0x0 E404		
Physical address View0	0xE000 E404		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:24	PRI_7	Each priority field holds a priority value	RW modify	0x00
23:16	PRI_6	Each priority field holds a priority value	RW modify	0x00
15:8	PRI_5	Each priority field holds a priority value	RW modify	0x00
7:0	PRI_4	Each priority field holds a priority value	RW modify	0x00

6.94. NVIC_IPR2

NVIC_IPR2			
Description	Interrupt Priority Register 2		
Address Region	cm4	**Type:**	RW
Offset	0x0 E408		
Physical address View0	0xE000 E408		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:24	PRI_11	Each priority field holds a priority value	RW modify	0x00
23:16	PRI_10	Each priority field holds a priority value	RW modify	0x00
15:8	PRI_9	Each priority field holds a priority value	RW modify	0x00
7:0	PRI_8	Each priority field holds a priority value	RW modify	0x00

6.95. NVIC_IPR3

NVIC_IPR3			
Description	Interrupt Priority Register 3		
Address Region	cm4	**Type:**	RW
Offset	0x0 E40C		
Physical address View0	0xE000 E40C		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:24	PRI_15	Each priority field holds a priority value	RW modify	0x00
23:16	PRI_14	Each priority field holds a priority value	RW modify	0x00
15:8	PRI_13	Each priority field holds a priority value	RW modify	0x00
7:0	PRI_12	Each priority field holds a priority value	RW modify	0x00

6.96. NVIC_IPR4

NVIC_IPR4					
Description	Interrupt Priority Register 4				
Address Region	cm4		**Type:**	RW	
Offset	0x0 E410				
Physical address View0	0xE000 E410				
Physical address View1	-				
Bit field Details					
Bits	**Name**	**Description**		**Access**	**Reset**
31:24	PRI_19	Each priority field holds a priority value		RW modify	0x00
23:16	PRI_18	Each priority field holds a priority value		RW modify	0x00
15:8	PRI_17	Each priority field holds a priority value		RW modify	0x00
7:0	PRI_16	Each priority field holds a priority value		RW modify	0x00

6.97. NVIC_IPR5

NVIC_IPR5					
Description	Interrupt Priority Register 5				
Address Region	cm4		**Type:**	RW	
Offset	0x0 E414				
Physical address View0	0xE000 E414				
Physical address View1	-				
Bit field Details					
Bits	**Name**	**Description**		**Access**	**Reset**
31:24	PRI_23	Each priority field holds a priority value		RW modify	0x00
23:16	PRI_22	Each priority field holds a priority value		RW modify	0x00
15:8	PRI_21	Each priority field holds a priority value		RW modify	0x00
7:0	PRI_20	Each priority field holds a priority value		RW modify	0x00

6.98. NVIC_IPR6

NVIC_IPR6			
Description	Interrupt Priority Register 6		
Address Region	cm4	**Type:**	RW
Offset	0x0 E418		
Physical address View0	0xE000 E418		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:24	PRI_27	Each priority field holds a priority value	RW modify	0x00
23:16	PRI_26	Each priority field holds a priority value	RW modify	0x00
15:8	PRI_25	Each priority field holds a priority value	RW modify	0x00
7:0	PRI_24	Each priority field holds a priority value	RW modify	0x00

6.99. NVIC_IPR7

NVIC_IPR7			
Description	Interrupt Priority Register 7		
Address Region	cm4	**Type:**	RW
Offset	0x0 E41C		
Physical address View0	0xE000 E41C		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:24	PRI_31	Each priority field holds a priority value	RW modify	0x00
23:16	PRI_30	Each priority field holds a priority value	RW modify	0x00
15:8	PRI_29	Each priority field holds a priority value	RW modify	0x00
7:0	PRI_28	Each priority field holds a priority value	RW modify	0x00

6.100. NVIC_IPR8

NVIC_IPR8			
Description	Interrupt Priority Register 8		
Address Region	cm4	**Type:**	RW
Offset	0x0 E420		
Physical address View0	0xE000 E420		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:24	PRI_35	Each priority field holds a priority value	RW modify	0x00
23:16	PRI_34	Each priority field holds a priority value	RW modify	0x00
15:8	PRI_33	Each priority field holds a priority value	RW modify	0x00
7:0	PRI_32	Each priority field holds a priority value	RW modify	0x00

6.101. NVIC_IPR9

NVIC_IPR9			
Description	Interrupt Priority Register 9		
Address Region	cm4	**Type:**	RW
Offset	0x0 E424		
Physical address View0	0xE000 E424		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:24	PRI_39	Each priority field holds a priority value	RW modify	0x00
23:16	PRI_38	Each priority field holds a priority value	RW modify	0x00
15:8	PRI_37	Each priority field holds a priority value	RW modify	0x00
7:0	PRI_36	Each priority field holds a priority value	RW modify	0x00

6.102. NVIC_IPR10

NVIC_IPR10			
Description	Interrupt Priority Register 10		
Address Region	cm4	**Type:**	RW
Offset	0x0 E428		
Physical address View0	0xE000 E428		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:24	PRI_43	Each priority field holds a priority value	RW modify	0x00
23:16	PRI_42	Each priority field holds a priority value	RW modify	0x00
15:8	PRI_41	Each priority field holds a priority value	RW modify	0x00
7:0	PRI_40	Each priority field holds a priority value	RW modify	0x00

6.103. NVIC_IPR11

NVIC_IPR11			
Description	Interrupt Priority Register 11		
Address Region	cm4	**Type:**	RW
Offset	0x0 E42C		
Physical address View0	0xE000 E42C		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:24	PRI_47	Each priority field holds a priority value	RW modify	0x00
23:16	PRI_46	Each priority field holds a priority value	RW modify	0x00
15:8	PRI_45	Each priority field holds a priority value	RW modify	0x00
7:0	PRI_44	Each priority field holds a priority value	RW modify	0x00

6.104. NVIC_IPR12

NVIC_IPR12			
Description	Interrupt Priority Register 12		
Address Region	cm4	**Type:**	RW
Offset	0x0 E430		
Physical address View0	0xE000 E430		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:24	PRI_51	Each priority field holds a priority value	RW modify	0x00
23:16	PRI_50	Each priority field holds a priority value	RW modify	0x00
15:8	PRI_49	Each priority field holds a priority value	RW modify	0x00
7:0	PRI_48	Each priority field holds a priority value	RW modify	0x00

6.105. NVIC_IPR13

NVIC_IPR13			
Description	Interrupt Priority Register 13		
Address Region	cm4	**Type:**	RW
Offset	0x0 E434		
Physical address View0	0xE000 E434		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:24	PRI_55	Each priority field holds a priority value	RW modify	0x00
23:16	PRI_54	Each priority field holds a priority value	RW modify	0x00
15:8	PRI_53	Each priority field holds a priority value	RW modify	0x00
7:0	PRI_52	Each priority field holds a priority value	RW modify	0x00

6.106. NVIC_IPR14

NVIC_IPR14				
Description	Interrupt Priority Register 14			
Address Region	cm4	**Type:**	RW	
Offset	0x0 E438			
Physical address View0	0xE000 E438			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:24	PRI_59	Each priority field holds a priority value	RW modify	0x00
23:16	PRI_58	Each priority field holds a priority value	RW modify	0x00
15:8	PRI_57	Each priority field holds a priority value	RW modify	0x00
7:0	PRI_56	Each priority field holds a priority value	RW modify	0x00

6.107. NVIC_IPR15

NVIC_IPR15				
Description	Interrupt Priority Register 15			
Address Region	cm4	**Type:**	RW	
Offset	0x0 E43C			
Physical address View0	0xE000 E43C			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:24	PRI_63	Each priority field holds a priority value	RW modify	0x00
23:16	PRI_62	Each priority field holds a priority value	RW modify	0x00
15:8	PRI_61	Each priority field holds a priority value	RW modify	0x00
7:0	PRI_60	Each priority field holds a priority value	RW modify	0x00

6.108. NVIC_IPR16

NVIC_IPR16			
Description	Interrupt Priority Register 16		
Address Region	cm4	**Type:**	RW
Offset	0x0 E440		
Physical address View0	0xE000 E440		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:24	PRI_67	Each priority field holds a priority value	RW modify	0x00
23:16	PRI_66	Each priority field holds a priority value	RW modify	0x00
15:8	PRI_65	Each priority field holds a priority value	RW modify	0x00
7:0	PRI_64	Each priority field holds a priority value	RW modify	0x00

6.109. NVIC_IPR17

NVIC_IPR17			
Description	Interrupt Priority Register 17		
Address Region	cm4	**Type:**	RW
Offset	0x0 E444		
Physical address View0	0xE000 E444		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:24	PRI_71	Each priority field holds a priority value	RW modify	0x00
23:16	PRI_70	Each priority field holds a priority value	RW modify	0x00
15:8	PRI_69	Each priority field holds a priority value	RW modify	0x00
7:0	PRI_68	Each priority field holds a priority value	RW modify	0x00

6.110. NVIC_IPR18

NVIC_IPR18			
Description	Interrupt Priority Register 18		
Address Region	cm4	**Type:**	RW
Offset	0x0 E448		
Physical address View0	0xE000 E448		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:24	PRI_75	Each priority field holds a priority value	RW modify	0x00
23:16	PRI_74	Each priority field holds a priority value	RW modify	0x00
15:8	PRI_73	Each priority field holds a priority value	RW modify	0x00
7:0	PRI_72	Each priority field holds a priority value	RW modify	0x00

6.111. NVIC_IPR19

NVIC_IPR19			
Description	Interrupt Priority Register 19		
Address Region	cm4	**Type:**	RW
Offset	0x0 E44C		
Physical address View0	0xE000 E44C		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:24	PRI_79	Each priority field holds a priority value	RW modify	0x00
23:16	PRI_78	Each priority field holds a priority value	RW modify	0x00
15:8	PRI_77	Each priority field holds a priority value	RW modify	0x00
7:0	PRI_76	Each priority field holds a priority value	RW modify	0x00

6.112. SCS_CPUID

SCS_CPUID			
Description	CPUID Base Register		
Address Region	cm4	**Type:**	RO
Offset	0x0 ED00		
Physical address View0	0xE000 ED00		
Physical address View1	-		

Bit field Details

Bits	Name	Description	Access	Reset
31:24	Implementer	Implementer code: 0x41 = ARM	RO	0x41
23:20	Variant	Variant number, the r value in the rnpn product revision identifier: 0x0 = Revision 0	RO	0x0
19:16	Constant	Reads as 0xF	RO	0xF
15:4	PartNo	Part number of the processor: 0xC24 = Cortex-M4	RO	0xC24
3:0	Revision	Revision number, the p value in the rnpn product revision identifier: 0x0 = Patch 0	RO	0x1

6.113. SCS_ICSR

SCS_ICSR			
Description	Interrupt Control and State Register		
Address Region	cm4	**Type:**	RW
Offset	0x0 ED04		
Physical address View0	0xE000 ED04		
Physical address View1	-		

Bit field Details

Bits	Name	Description	Access	Reset
31	NMIPENDSET	NMI set-pending bit. Write: 0 = no effect 1 = changes NMI exception state to pending. Read: 0 = NMI exception is not pending 1 = NMI exception is pending. Because NMI is the highest-priority exception, normally the processor enter the NMI exception handler as soon as it registers a write of 1 to this bit, and entering the handler clears this bit to 0. A read of this bit by the NMI exception handler returns 1 only if the NMI signal is reasserted while the processor is executing that handler.	RW modify	0
30:29	Reserved	-	-	-
28	PENDSVSET	PendSV set-pending bit. Write: 0 = no effect 1 = changes PendSV exception state	RW modify	0

		to pending. Read: 0 = PendSV exception is not pending 1 = PendSV exception is pending. Writing 1 to this bit is the only way to set the PendSV exception state to pending.		
27	PENDSVCLR	PendSV clear-pending bit. Write: 0 = no effect 1 = removes the pending state from the PendSV exception.	RW modify	0
26	PENDSTSET	SysTick exception set-pending bit. Write: 0 = no effect 1 = changes SysTick exception state to pending. Read: 0 = SysTick exception is not pending 1 = SysTick exception is pending.	RW modify	0
25	PENDSTCLR	SysTick exception clear-pending bit. Write: 0 = no effect 1 = removes the pending state from the SysTick exception. This bit is WO. On a register read its value is Unknown.	RW modify	0
24	Reserved	-	-	-
23	Reserved_for_Debug_use	This bit is reserved for Debug use and reads-as-zero when the processor is not in Debug.	RO	0
22	ISRPENDING	Interrupt pending flag, excluding NMI and Faults: 0 = interrupt not pending 1 = interrupt pending.	RO	0
21:18	Reserved	-	-	-
17:12	VECTPENDING	Indicates the exception number of the highest priority pending enabled exception: 0 = no pending exceptions Nonzero = the exception number of the highest priority pending enabled exception. The value indicated by this field includes the effect of the BASEPRI and FAULTMASK registers, but not any effect of the PRIMASK register.	RO	0x00
11	RETTOBASE	Indicates whether there are preempted active exceptions: 0 = there are preempted active exceptions to execute 1 = there are no active exceptions, or the currently-executing exception is the only active exception.	RO	0
10:9	Reserved	-	-	-
8:0	VECTACTIVE	Contains the active exception number: 0 = Thread mode Nonzero = The exception number of the currently active exception (Note) Subtract 16 from this value to obtain	RO	0x000

		the CMSIS IRQ number required to index into the Interrupt Clear-Enable, Set-Enable, Clear-Pending, Set-Pending, or Priority Registers. This is the same value as IPSR bits[8:0], see Interrupt Program Status Register		

6.114. SCS_VTOR

SCS_VTOR			
Description	Vector Table Offset Register		
Address Region	cm4	**Type:**	RW
Offset	0x0 ED08		
Physical address View0	0xE000 ED08		
Physical address View1	-		

Bit field Details

Bits	Name	Description	Access	Reset
31:7	TBLOFF	Vector table base offset field. It contains bits[29:7] of the offset of the table base from the bottom of the memory map. (Note) Bit[29] determines whether the vector table is in the code or SRAM memory region: • 0 = code • 1 = SRAM. Bit[29] is sometimes called the TBLBASE bit.	RW modify	0x000 0000
6:0	Reserved	-	-	-

6.115. SCS_AIRCR

SCS_AIRCR			
Description	Application Interrupt and Reset Control Register		
Address Region	cm4	**Type:**	RW
Offset	0x0 ED0C		
Physical address View0	0xE000 ED0C		
Physical address View1	-		

Bit field Details

Bits	Name	Description	Access	Reset
31:16	VECTKEY	Register key: Reads as 0xFA05 On writes, write 0x5FA to VECTKEY, otherwise the write is ignored.	RW modify	0xFA05
15	ENDIANNESS	Data endianness bit: 0 = Little-endian 1 = Big-endian.	RO	0
14:11	Reserved	-	-	-
10:8	PRIGROUP	Interrupt priority grouping field. This field determines the split of group	RW modify	0b000

		priority from sub priority		
7:3	Reserved	-	-	-
2	SYSRESETREQ	System reset request: 0 = no system reset request 1 = asserts a signal to the outer system that requests a reset. This is intended to force a large system reset of all major components except for debug. This bit reads as 0.	RW modify	0
1	VECTCLRACTIVE	Reserved for Debug use. This bit reads as 0. When writing to the register you must write 0 to this bit, otherwise behavior is Unpredictable.	RW modify	0
0	VECTRESET	Reserved for Debug use. This bit reads as 0. When writing to the register you must write 0 to this bit, otherwise behavior is Unpredictable.	RW modify	0

6.116. SCS_SCR

SCS_SCR			
Description	System Control Register		
Address Region	cm4	**Type:**	RW
Offset	0x0 ED10		
Physical address View0	0xE000 ED10		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:5	Reserved	-	-	-
4	SEVONPEND	Send Event on Pending bit: 0 = only enabled interrupts or events can wake up the processor, disabled interrupts are excluded 1 = enabled events and all interrupts, including disabled interrupts, can wake up the processor. When an event or interrupt enters pending state, the event signal wakes up the processor from WFE. If the processor is not waiting for an event, the event is registered and affects the next WFE. The processor also wakes up on execution of an SEV instruction or an external event.	RW modify	0
3	Reserved	-	-	-
2	SLEEPDEEP	Controls whether the processor uses sleep or deep sleep as its low power mode: 0 = sleep 1 = deep sleep.	RW modify	0
1	SLEEPONEXIT	Indicates sleep-on-exit when returning from Handler mode to Thread mode: 0 = do not sleep when returning to Thread mode. 1 = enter sleep, or deep sleep, on return from an ISR. Setting this bit to 1 enables an interrupt driven application to avoid returning to	RW modify	0

		an empty main application.		
0	Reserved	-	-	-

6.117. SCS_CCR

SCS_CCR			
Description	Configuration and Control Register		
Address Region	cm4	**Type:**	RW
Offset	0x0 ED14		
Physical address View0	0xE000 ED14		
Physical address View1	-		

Bit field Details

Bits	Name	Description	Access	Reset
31:10	Reserved	-	-	-
9	STKALIGN	Indicates stack alignment on exception entry: 0 = 4-byte aligned 1 = 8-byte aligned. On exception entry, the processor uses bit[9] of the stacked PSR to indicate the stack alignment. On return from the exception it uses this stacked bit to restore the correct stack alignment.	RW modify	0
8	BFHFNMIGN	Enables handlers with priority -1 or -2 to ignore data Bus Faults caused by load and store instructions. This applies to the hard fault, NMI, and FAULTMASK escalated handlers: 0 = data bus faults caused by load and store instructions cause a lock-up 1 = handlers running at priority -1 and -2 ignore data bus faults caused by load and store instructions. Set this bit to 1 only when the handler and its data are in absolutely safe memory. The normal use of this bit is to probe system devices and bridges to detect control path problems and fix them.	RW modify	0
7:5	Reserved	-	-	-
4	DIV_0_TRP	Enables faulting or halting when the processor executes an SDIV or UDIV instruction with a divisor of 0: 0 = do not trap divide by 0 1 = trap divide by 0. When this bit is set to 0,a divide by zero returns a quotient of 0.	RW modify	0
3	UNALIGN_TRP	Enables unaligned access traps: 0 = do not trap unaligned half word and word accesses 1 = trap unaligned half word and word accesses. If this bit is set to 1, an unaligned access generates a Usage Fault. Unaligned LDM, STM, LDRD, and STRD instructions always fault irrespective of whether UNALIGN_TRP is set to 1.	RW modify	0

2	Reserved	-	-	-
1	USERSETMPEND	Enables unprivileged software access to the STIR: 0 = disable 1 = enable.	RW modify	0
0	NONBASETHRDENA	Indicates how the processor enters Thread mode: 0 = processor can enter Thread mode only when no exception is active. 1 = processor can enter Thread mode from any level under the control of an EXC_RETURN value	RW modify	0

6.118. SCS_SHPR1

SCS_SHPR1			
Description	System Handler Priority Register 1		
Address Region	cm4	**Type:**	RW
Offset	0x0 ED18		
Physical address View0	0xE000 ED18		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:24	Reserved	-	-	-
23:16	PRI_6	Priority of system handler 6, Usage Fault	RW modify	0x00
15:8	PRI_5	Priority of system handler 5, Bus Fault	RW modify	0x00
7:0	PRI_4	Priority of system handler 4, MemManage	RW modify	0x00

6.119. SCS_SHPR2

SCS_SHPR2			
Description	System Handler Priority Register 2		
Address Region	cm4	**Type:**	RW
Offset	0x0 ED1C		
Physical address View0	0xE000 ED1C		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:24	PRI_11	Priority of system handler 11, SVCall	RW modify	0x00
23:0	Reserved	-	-	-

6.120. SCS_SHPR3

SCS_SHPR3			
Description	System Handler Priority Register 3		
Address Region	cm4	**Type:**	RW
Offset	0x0 ED20		
Physical address View0	0xE000 ED20		
Physical address View1	-		

Bit field Details

Bits	Name	Description	Access	Reset
31:24	PRI_15	Priority of system handler 15, SysTick exception	RW modify	0x00
23:16	PRI_14	Priority of system handler 14, PendSV	RW modify	0x00
15:0	Reserved	-	-	-

6.121. SCS_SHCRS

SCS_SHCRS			
Description	System Handler Control and State Register		
Address Region	cm4	**Type:**	RW
Offset	0x0 ED24		
Physical address View0	0xE000 ED24		
Physical address View1	-		

Bit field Details

Bits	Name	Description	Access	Reset
31:19	Reserved	-	-	-
18	USGFAULTENA	Usage Fault enable bit, set to 1 to enable (Note) Enable bits, set to 1 to enable the exception, or set to 0 to disable the exception.	RW modify	0
17	BUSFAULTENA	Bus Fault enable bit, set to 1 to enable	RW modify	0
16	MEMFAULTENA	MemManage enable bit, set to 1 to enable	RW modify	0
15	SVCALLPENDED	SVCall pending bit, reads as 1 if exception is pending (Note) Pending bits, read as 1 if the exception is pending, or as 0 if it is not pending. You can write to these bits to change the pending status of the exceptions.	RW modify	0
14	BUSFAULTPENDED	Bus Fault exception pending bit, reads as 1 if exception is pending	RW modify	0
13	MEMFAULTPENDED	MemManage exception pending bit, reads as 1 if exception is pending	RW modify	0
12	USGFAULTPENDED	Usage Fault exception pending bit, reads as 1 if exception is pending	RW modify	0
11	SYSTICKACT	SysTick exception active bit, reads as 1 if exception is active (Note)	RW modify	0

		Active bits, read as 1 if the exception is active, or as 0 if it is not active. You can write to these bits to change the active status of the exceptions.		
10	PENDSVACT	PendSV exception active bit, reads as 1 if exception is active	RW modify	0
9	Reserved	-	-	-
8	MONITORACT	Debug monitor active bit, reads as 1 if Debug monitor is active	RW modify	0
7	SVCALLACT	SVCall active bit, reads as 1 if SVC call is active	RW modify	0
6:4	Reserved	-	-	-
3	USGFAULTACT	Usage Fault exception active bit, reads as 1 if exception is active	RW modify	0
2	Reserved	-	-	-
1	BUSFAULTACT	Bus Fault exception active bit, reads as 1 if exception is active	RW modify	0
0	MEMFAULTACT	MemManage exception active bit, reads as 1 if exception is active	RW modify	0

6.122. SCS_CFSR

SCS_CFSR			
Description	Configurable Fault Status Register		
Address Region	cm4	**Type:**	RW
Offset	0x0 ED28		
Physical address View0	0xE000 ED28		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:26	Reserved	-	-	-
25	DIVBYZERO	Usage Fault Status Register: Divide by zero Usage Fault: 0 = no divide by zero fault, or divide by zero trapping not enabled 1 = the processor has executed an SDIV or UDIV instruction with a divisor of 0. When the processor sets this bit to 1, the PC value stacked for the exception return points to the instruction that performed the divide by zero. Enable trapping of divide by zero by setting the DIV_0_TRP bit in the CCR to 1.	RW modify	0
24	UNALIGNED	Usage Fault Status Register: Unaligned access Usage Fault: 0 = no unaligned access fault, or unaligned access trapping not enabled 1 = the processor has made an unaligned memory access. Enable trapping of unaligned accesses by setting the UNALIGN_TRP bit in the CCR to 1. Unaligned LDM, STM, LDRD, and STRD instructions always fault irrespective of the setting of UNALIGN_TRP.	RW modify	0

23:20	Reserved	-	-	-
19	NOCP	Usage Fault Status Register: No coprocessor Usage Fault. The processor does not support coprocessor instructions: 0 = no Usage Fault caused by attempting to access a coprocessor 1 = the processor has attempted to access a coprocessor.	RW modify	0
18	INVPC	Usage Fault Status Register: Invalid PC load Usage Fault, caused by an invalid PC load by EXC_RETURN: 0 = no invalid PC load Usage Fault 1 = the processor has attempted an illegal load of EXC_RETURN to the PC, as a result of an invalid context, or an invalid EXC_RETURN value. When this bit is set to 1, the PC value stacked for the exception return points to the instruction that tried to perform the illegal load of the PC.	RW modify	0
17	INVSTATE	Usage Fault Status Register: Invalid state Usage Fault: 0 = no invalid state Usage Fault 1 = the processor has attempted to execute an instruction that makes illegal use of the EPSR. When this bit is set to 1, the PC value stacked for the exception return points to the instruction that attempted the illegal use of the EPSR. This bit is not set to 1 if an undefined instruction uses the EPSR.	RW modify	0
16	UNDEFINSTR	Usage Fault Status Register: Undefined instruction Usage Fault: 0 = no undefined instruction Usage Fault 1 = the processor has attempted to execute an undefined instruction. When this bit is set to 1, the PC value stacked for the exception return points to the undefined instruction. An undefined instruction is an instruction that the processor cannot decode.	RW modify	0
15	BFARVALID	Bus Fault Address Register (BFAR) valid flag: 0 = value in BFAR is not a valid fault address 1 = BFAR holds a valid fault address. The processor sets this bit to 1 after a Bus Fault where the address is known. Other faults can set this bit to 0, such as a MemManage fault occurring later. If a Bus Fault occurs and is escalated to a hard fault because of priority, the hard fault handler must set this bit to 0. This prevents problems if returning to a stacked active Bus Fault handler whose BFAR value has been	RW modify	0

		overwritten.		
14	Reserved	-	-	-
13	LSPERR	Bus Fault Status Register: 0 = No bus fault occurred during floating-point lazy state preservation. 1 = A bus fault occurred during floating-point lazy state preservation	RW modify	0
12	STKERR	Bus Fault Status Register: Bus Fault on stacking for exception entry: 0 = no stacking fault 1 = stacking for an exception entry has caused one or more Bus Faults. When the processor sets this bit to 1, the SP is still adjusted but the values in the context area on the stack might be incorrect. The processor does not write a fault address to the BFAR.	RW modify	0
11	UNSTKERR	Bus Fault Status Register: Bus Fault on unstacking for a return from exception: 0 = no unstacking fault 1 = unstack for an exception return has caused one or more Bus Faults. This fault is chained to the handler. This means that when the processor sets this bit to 1, the original return stack is still present. The processor does not adjust the SP from the failing return, does not performed a new save, and does not write a fault address to the BFAR.	RW modify	0
10	IMPRECISERR	Bus Fault Status Register: Imprecise data bus error: 0 = no imprecise data bus error 1 = a data bus error has occurred, but the return address in the stack frame is not related to the instruction that caused the error. When the processor sets this bit to 1, it does not write a fault address to the BFAR. This is an asynchronous fault. Therefore, if it is detected when the priority of the current process is higher than the Bus Fault priority, the Bus Fault becomes pending and becomes active only when the processor returns from all higher priority processes. If a precise fault occurs before the processor enters the handler for the imprecise Bus Fault, the handler detects both IMPRECISERR set to 1 and one of the precise fault status bits set to 1.	RW modify	0

9	PRECISERR	Bus Fault Status Register: Precise data bus error: 0 = no precise data bus error 1 = a data bus error has occurred, and the PC value stacked for the exception return points to the instruction that caused the fault. When the processor sets this bit is 1, it writes the faulting address to the BFAR.	RW modify	0
8	IBUSERR	Bus Fault Status Register: Instruction bus error: 0 = no instruction bus error 1 = instruction bus error. The processor detects the instruction bus error on prefetching an instruction, but it sets the IBUSERR flag to 1 only if it attempts to issue the faulting instruction. When the processor sets this bit is 1, it does not write a fault address to the BFAR.	RW modify	0
7	MMARVALID	MemManage Fault Status Register: MemManage Fault Address Register (MMFAR) valid flag: 0 = value in MMAR is not a valid fault address 1 = MMAR holds a valid fault address. If a MemManage fault occurs and is escalated to a Hard Fault because of priority, the Hard Fault handler must set this bit to 0. This prevents problems on return to a stacked active MemManage fault handler whose MMAR value has been overwritten.	RW modify	0
6	Reserved	-	-	-
5	MLSPERR	MemManage Fault Status Register: 0 = No MemManage fault occurred during floating-point lazy state preservation 1 = A MemManage fault occurred during floating-point lazy state preservation	RW modify	0
4	MSTKERR	MemManage Fault Status Register: MemManage fault on stacking for exception entry: 0 = no stacking fault 1 = stacking for an exception entry has caused one or more access violations. When this bit is 1, the SP is still adjusted but the values in the context area on the stack might be incorrect. The processor has not written a fault address to the MMAR.	RW modify	0
3	MUNSTKERR	MemManage Fault Status Register: MemManage fault on unstacking for a return from exception: 0 = no unstacking fault 1 = unstack for an exception return has caused one or more access violations. This fault is chained to the handler. This means that when this bit is 1, the original return stack is still present. The	RW modify	0

		processor has not adjusted the SP from the failing return, and has not performed a new save. The processor has not written a fault address to the MMAR.		
2	Reserved	-	-	-
1	DACCVIOL	MemManage Fault Status Register: Data access violation flag: 0 = no data access violation fault 1 = the processor attempted a load or store at a location that does not permit the operation. When this bit is 1, the PC value stacked for the exception return points to the faulting instruction. The processor has loaded the MMAR with the address of the attempted access.	RW modify	0
0	IACCVIOL	MemManage Fault Status Register: Instruction access violation flag: 0 = no instruction access violation fault 1 = the processor attempted an instruction fetch from a location that does not permit execution. This fault occurs on any access to an XN region, even when the MPU is disabled or not present. When this bit is 1, the PC value stacked for the exception return points to the faulting instruction. The processor has not written a fault address to the MMAR.	RW modify	0

6.123. SCS_HFSR

SCS_HFSR			
Description	Hard Fault Status Register		
Address Region	cm4	**Type:**	RW
Offset	0x0 ED2C		
Physical address View0	0xE000 ED2C		
Physical address View1	-		

Bit field Details

Bits	Name	Description	Access	Reset
31	DEBUGEVT	Reserved for Debug use. When writing to the register you must write 0 to this bit, otherwise behavior is Unpredictable.	RW modify	0
30	FORCED	Indicates a forced hard fault, generated by escalation of a fault with configurable priority that cannot be handles, either because of priority or because it is disabled: 0 = no forced Hard Fault 1 = forced Hard Fault. When this bit is set to 1, the Hard Fault handler must read the other fault status registers to find the cause of the fault.	RW modify	0
29:2	Reserved	-	-	-
1	VECTTBL	Indicates a Bus Fault on a vector table read during exception processing: 0 = no Bus Fault on vector table read 1 = Bus Fault on vector table read. This error is always handled by the hard fault handler. When this bit is set to 1, the PC value stacked for the exception return points to the instruction that was preempted by the exception.	RW modify	0
0	Reserved	-	-	-

6.124. DFSR

DFSR			
Description	Debug Fault Status Register		
Address Region	cm4	**Type:**	RW
Offset	0x0 ED30		
Physical address View0	0xE000 ED30		
Physical address View1	-		

Bit field Details

Bits	Name	Description	Access	Reset
31:5	Reserved	-	-	-
4	EXTERNAL	Indicates a debug event generated because of the assertion of EDBGRQ: 0 = No EDBGRQ debug event. 1 = EDBGRQ debug event.	RW oneToClear	0
3	VCATCH	Indicates triggering of a Vector catch: 0 = No Vector catch triggered. 1 = Vector catch triggered. The corresponding FSR shows the primary cause of the exception.	RW oneToClear	0
2	DWTTRAP	Indicates a debug event generated by the DWT: 0 = No current debug events generated by the DWT. 1 = At least one current debug event generated by the DWT.	RW oneToClear	0
1	BKPT	Indicates a debug event generated by BKPT instruction execution or a breakpoint match in FPB: 0 = No current breakpoint debug event. 1 = At least one current breakpoint debug event.	RW oneToClear	0
0	HALTED	Indicates a debug event generated by either: • a C_HALT or C_STEP request, triggered by a write to the DHCSR. • a step request triggered by setting DEMCR.MON_STEP to 1. 0 = No active halt request debug event. 1 = Halt request debug event active.	RW oneToClear	0

6.125. SCS_MMAR

SCS_MMAR			
Description	MemManage Fault Address Register		
Address Region	cm4	**Type:**	RW
Offset	0x0 ED34		
Physical address View0	0xE000 ED34		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	ADDRESS	When the MMARVALID bit of the MMFSR is set to 1, this field holds the address of the location that generated the MemManage fault	RW modify	-

6.126. SCS_BFAR

SCS_BFAR			
Description	Bus Fault Address Register		
Address Region	cm4	**Type:**	RW
Offset	0x0 ED38		
Physical address View0	0xE000 ED38		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	ADDRESS	When the BFARVALID bit of the BFSR is set to 1, this field holds the address of the location that generated the Bus Fault	RW modify	-

6.127. SCS_AFSR

SCS_AFSR			
Description	Auxiliary Fault Status Register		
Address Region	cm4	**Type:**	RW
Offset	0x0 ED3C		
Physical address View0	0xE000 ED3C		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	IMPDEF	Implementation defined. The bits map to the AUXFAULT input signals.	RW modify	0x0000 0000

6.128. SCS_ID_PFR0

SCS_ID_PFR0			
Description	Processor Feature Register 0		
Address Region	cm4	**Type:**	RO
Offset	0x0 ED40		
Physical address View0	0xE000 ED40		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	ID_PFR0	Processor Feature Register 0	RO	0x0000 0030

6.129. SCS_ID_PFR1

SCS_ID_PFR1			
Description	Processor Feature Register 1		
Address Region	cm4	**Type:**	RO
Offset	0x0 ED44		
Physical address View0	0xE000 ED44		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	ID_PFR1	Processor Feature Register 1	RO	0x0000 0200

6.130. SCS_ID_DFR0

SCS_ID_DFR0			
Description	Debug Features Register 0		
Address Region	cm4	**Type:**	RO
Offset	0x0 ED48		
Physical address View0	0xE000 ED48		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	ID_DFR0	Debug Features Register 0	RO	0x0010 0000

6.131. SCS_ID_AFR0

SCS_ID_AFR0			
Description	Auxiliary Features Register 0		
Address Region	cm4	**Type:**	RO
Offset	0x0 ED4C		
Physical address View0	0xE000 ED4C		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	ID_AFR0	Auxiliary Features Register 0	RO	0x0000 0000

6.132. SCS_ID_MMFR0

SCS_ID_MMFR0			
Description	Memory Model Feature Register 0		
Address Region	cm4	**Type:**	RO
Offset	0x0 ED50		
Physical address View0	0xE000 ED50		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	ID_MMFR0	Memory Model Feature Register 0	RO	0x0010 0030

6.133. SCS_ID_MMFR1

SCS_ID_MMFR1			
Description	Memory Model Feature Register 1		
Address Region	cm4	**Type:**	RO
Offset	0x0 ED54		
Physical address View0	0xE000 ED54		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	ID_MMFR1	Memory Model Feature Register 1	RO	0x0000 0000

6.134. SCS_ID_MMFR2

SCS_ID_MMFR2					
Description	Memory Model Feature Register 2				
Address Region	cm4		**Type:**	RO	
Offset	0x0 ED58				
Physical address View0	0xE000 ED58				
Physical address View1	-				
Bit field Details					
Bits	**Name**	**Description**		**Access**	**Reset**
31:0	ID_MMFR2	Memory Model Feature Register 2		RO	0x0100 0000

6.135. SCS_ID_MMFR3

SCS_ID_MMFR3					
Description	Memory Model Feature Register 3				
Address Region	cm4		**Type:**	RO	
Offset	0x0 ED5C				
Physical address View0	0xE000 ED5C				
Physical address View1	-				
Bit field Details					
Bits	**Name**	**Description**		**Access**	**Reset**
31:0	ID_MMFR3	Memory Model Feature Register 3		RO	0x0000 0000

6.136. SCS_ID_ISAR0

SCS_ID_ISAR0					
Description	Instruction Set Attributes Register 0				
Address Region	cm4		**Type:**	RO	
Offset	0x0 ED60				
Physical address View0	0xE000 ED60				
Physical address View1	-				
Bit field Details					
Bits	**Name**	**Description**		**Access**	**Reset**
31:0	ID_ISAR0	Instruction Set Attributes Register 0		RO	0x0114 1110

6.137. SCS_ID_ISAR1

SCS_ID_ISAR1				
Description	Instruction Set Attributes Register 1			
Address Region	cm4	**Type:**	RO	
Offset	0x0 ED64			
Physical address View0	0xE000 ED64			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	ID_ISAR1	Instruction Set Attributes Register 1	RO	0x0211 2000

6.138. SCS_ID_ISAR2

SCS_ID_ISAR2				
Description	Instruction Set Attributes Register 2			
Address Region	cm4	**Type:**	RO	
Offset	0x0 ED68			
Physical address View0	0xE000 ED68			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	ID_ISAR2	Instruction Set Attributes Register 2	RO	0x2123 2231

6.139. SCS_ID_ISAR3

SCS_ID_ISAR3				
Description	Instruction Set Attributes Register 3			
Address Region	cm4	**Type:**	RO	
Offset	0x0 ED6C			
Physical address View0	0xE000 ED6C			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	ID_ISAR3	Instruction Set Attributes Register 3	RO	0x0111 1131

6.140. SCS_ID_ISAR4

SCS_ID_ISAR4			
Description	Instruction Set Attributes Register 4		
Address Region	cm4	**Type:**	RO
Offset	0x0 ED70		
Physical address View0	0xE000 ED70		
Physical address View1	-		

Bit field Details

Bits	Name	Description	Access	Reset
31:0	ID_ISAR4	Instruction Set Attributes Register 4	RO	0x0131 0132

6.141. CPACR

CPACR			
Description	Coprocessor Access Control Register		
Address Region	cm4	**Type:**	RW
Offset	0x0 ED88		
Physical address View0	0xE000 ED88		
Physical address View1	-		

Bit field Details

Bits	Name	Description	Access	Reset
31:24	Reserved	-	-	-
23:22	CP11	Access privileges for coprocessor 1. The possible values of each field are: 0b00 = Access denied. Any attempted access generates a NOCP Usage Fault. 0b01 = Privileged access only. An unprivileged access generates a NOCP fault. 0b10 = Reserved. The result of any access is Unpredictable. 0b11 = Full access.	RW modify	0b00
21:20	CP10	Access privileges for coprocessor 0. The possible values of each field are: 0b00 = Access denied. Any attempted access generates a NOCP Usage Fault. 0b01 = Privileged access only. An unprivileged access generates a NOCP fault. 0b10 = Reserved. The result of any access is Unpredictable. 0b11 = Full access.	RW modify	0b00
19:0	Reserved	-	-	-

6.142. MPU_TYPE

MPU_TYPE			
Description	MPU Type Register		
Address Region	cm4	**Type:**	RO
Offset	0x0 ED90		
Physical address View0	0xE000 ED90		
Physical address View1	-		

Bit field Details

Bits	Name	Description	Access	Reset
31:24	Reserved	-	-	-
23:16	IREGION	Indicates the number of supported MPU instruction regions. Always contains 0x00. The MPU memory map is unified and is described by the DREGION field.	RO	0x00
15:8	DREGION	Indicates the number of supported MPU data regions: 0x08 = Eight MPU regions.	RO	0x08
7:1	Reserved	-	-	-
0	SEPARATE	Indicates support for unified or separate instruction and date memory maps: 0 = unified.	RO	0

6.143. MPU_CTRL

MPU_CTRL			
Description	MPU Control Register		
Address Region	cm4	**Type:**	RW
Offset	0x0 ED94		
Physical address View0	0xE000 ED94		
Physical address View1	-		

Bit field Details

Bits	Name	Description	Access	Reset
31:3	Reserved	-	-	-
2	PRIVDEFENA	Enables privileged software access to the default memory map: 0 = If the MPU is enabled, disables use of the default memory map. Any memory access to a location not covered by any enabled region causes a fault. 1 = If the MPU is enabled, enables use of the default memory map as a background region for privileged software accesses. When enabled, the background region acts as if it is region number -1. Any region that is defined and enabled has priority over this default map. If the MPU is disabled, the processor ignores this bit.	RW modify	0
1	HFNMIENA	Enables the operation of MPU during hard fault, NMI, and FAULTMASK handlers. When the MPU is enabled: 0 = MPU is disabled during hard fault, NMI, and FAULTMASK handlers, regardless of the value of the ENABLE bit 1 = the MPU is enabled during hard fault, NMI, and FAULTMASK handlers. When the MPU is disabled, if this bit is set to 1 the behavior is Unpredictable.	RW modify	0
0	ENABLE	Enables the MPU: 0 = MPU disabled 1 = MPU enabled.	RW modify	0

6.144. MPU_RNR

MPU_RNR			
Description	MPU Region Number Register		
Address Region	cm4	**Type:**	RW
Offset	0x0 ED98		
Physical address View0	0xE000 ED98		
Physical address View1	-		

Bit field Details

Bits	Name	Description	Access	Reset
31:8	Reserved	-	-	-
7:0	REGION	Indicates the MPU region referenced by the MPU_RBAR and MPU_RASR registers. The MPU supports 8 memory regions, so the permitted values of this field are 0-7.	RW modify	0x00

6.145. MPU_RBAR

MPU_RBAR			
Description	MPU Region Base Address Register		
Address Region	cm4	**Type:**	RW
Offset	0x0 ED9C		
Physical address View0	0xE000 ED9C		
Physical address View1	-		

Bit field Details

Bits	Name	Description	Access	Reset
31:5	ADDR	Region base address field. [31:N] : ADDR field [N:5] : reserved. The value of N depends on the region size. The ADDR field is bits[31:N] of the MPU_RBAR. The region size, as specified by the SIZE field in the MPU_RASR, defines the value of N: N = Log2(Region size in bytes),	RW modify	0x000 0000
4	VALID	MPU Region Number valid bit: Write: 0 = MPU_RNR not changed, and the processor: • updates the base address for the region specified in the MPU_RNR • ignores the value of the REGION field 1 = the processor: • updates the value of the MPU_RNR to the value of the REGION field • updates the base address for the region specified in the REGION field. Always reads as zero.	RW modify	0
3:0	REGION	MPU region field: For the behavior on writes, see the	RW modify	0x0

		description of the VALID field. On reads, returns the current region number, as specified by the RNR.		

6.146. MPU_RASR

MPU_RASR			
Description	MPU Region Attribute and Size Register		
Address Region	cm4	**Type:**	RW
Offset	0x0 EDA0		
Physical address View0	0xE000 EDA0		
Physical address View1	-		

Bit field Details

Bits	Name	Description	Access	Reset
31:29	Reserved	-	-	-
28	XN	Instruction access disable bit: 0 = instruction fetches enabled 1 = instruction fetches disabled.	RW modify	0
27	Reserved	-	-	-
26:24	AP	Access permission field	RW modify	0b000
23:22	Reserved	-	-	-
21:19	TEX	Memory access attributes	RW modify	0b000
18	S	Shareable bit	RW modify	0
17	C	Memory access attributes	RW modify	0
16	B	Memory access attributes	RW modify	0
15:8	SRD	Sub region disable bits. For each bit in this field: 0 = corresponding sub-region is enabled 1 = corresponding sub-region is disabled Region sizes of 128 bytes and less do not support subregions. When writing the attributes for such a region, write the SRD field as 0x00.	RW modify	0x00
7:6	Reserved	-	-	-
5:1	SIZE	Specifies the size of the MPU protection region. The minimum permitted value is 3(0b00010)	RW modify	0x00
0	ENABLE	Region enable bit.	RW modify	0

6.147. MPU_RBAR_A1

MPU_RBAR_A1			
Description	Alias of RBAR		
Address Region	cm4	**Type:**	RW
Offset	0x0 EDA4		
Physical address View0	0xE000 EDA4		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:5	ADDR	(see MPU_RBAR)	RW modify	0x000 0000
4	VALID	(see MPU_RBAR)	RW modify	0
3:0	REGION	(see MPU_RBAR)	RW modify	0x0

6.148. MPU_RASR_A1

MPU_RASR_A1			
Description	Alias of RASR		
Address Region	cm4	**Type:**	RW
Offset	0x0 EDA8		
Physical address View0	0xE000 EDA8		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:29	Reserved	-	-	-
28	XN	(see MPU_RASR)	RW modify	0
27	Reserved	-	-	-
26:24	AP	(see MPU_RASR)	RW modify	0b000
23:22	Reserved	-	-	-
21:19	TEX	(see MPU_RASR)	RW modify	0b000
18	S	(see MPU_RASR)	RW modify	0
17	C	(see MPU_RASR)	RW modify	0
16	B	(see MPU_RASR)	RW modify	0
15:8	SRD	(see MPU_RASR)	RW modify	0x00
7:6	Reserved	-	-	-
5:1	SIZE	(see MPU_RASR)	RW modify	0x00
0	ENABLE	(see MPU_RASR)	RW modify	0

6.149. MPU_RBAR_A2

MPU_RBAR_A2			
Description	Alias of RBAR		
Address Region	cm4	**Type:**	RW
Offset	0x0 EDAC		
Physical address View0	0xE000 EDAC		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:5	ADDR	(see MPU_RBAR)	RW modify	0x000 0000
4	VALID	(see MPU_RBAR)	RW modify	0
3:0	REGION	(see MPU_RBAR)	RW modify	0x0

6.150. MPU_RASR_A2

MPU_RASR_A2			
Description	Alias of RASR		
Address Region	cm4	**Type:**	RW
Offset	0x0 EDB0		
Physical address View0	0xE000 EDB0		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:29	Reserved	-	-	-
28	XN	(see MPU_RASR)	RW modify	0
27	Reserved	-	-	-
26:24	AP	(see MPU_RASR)	RW modify	0b000
23:22	Reserved	-	-	-
21:19	TEX	(see MPU_RASR)	RW modify	0b000
18	S	(see MPU_RASR)	RW modify	0
17	C	(see MPU_RASR)	RW modify	0
16	B	(see MPU_RASR)	RW modify	0
15:8	SRD	(see MPU_RASR)	RW modify	0x00
7:6	Reserved	-	-	-
5:1	SIZE	(see MPU_RASR)	RW modify	0x00
0	ENABLE	(see MPU_RASR)	RW modify	0

6.151. MPU_RBAR_A3

MPU_RBAR_A3			
Description	Alias of RBAR		
Address Region	cm4	**Type:**	RW
Offset	0x0 EDB4		
Physical address View0	0xE000 EDB4		
Physical address View1	-		

Bit field Details

Bits	Name	Description	Access	Reset
31:5	ADDR	(see MPU_RBAR)	RW modify	0x000 0000
4	VALID	(see MPU_RBAR)	RW modify	0
3:0	REGION	(see MPU_RBAR)	RW modify	0x0

6.152. MPU_RASR_A3

MPU_RASR_A3			
Description	Alias of RASR		
Address Region	cm4	**Type:**	RW
Offset	0x0 EDB8		
Physical address View0	0xE000 EDB8		
Physical address View1	-		

Bit field Details

Bits	Name	Description	Access	Reset
31:29	Reserved	-	-	-
28	XN	(see MPU_RASR)	RW modify	0
27	Reserved	-	-	-
26:24	AP	(see MPU_RASR)	RW modify	0x0
23:22	Reserved	-	-	-
21:19	TEX	(see MPU_RASR)	RW modify	0x0
18	S	(see MPU_RASR)	RW modify	0
17	C	(see MPU_RASR)	RW modify	0
16	B	(see MPU_RASR)	RW modify	0
15:8	SRD	(see MPU_RASR)	RW modify	0x00
7:6	Reserved	-	-	-
5:1	SIZE	(see MPU_RASR)	RW modify	0x00
0	ENABLE	(see MPU_RASR)	RW modify	0

6.153. DHCSR

DHCSR				
Description	Debug Halting Control and Status Register			
Address Region	cm4	**Type:**	RW	
Offset	0x0 EDF0			
Physical address View0	0xE000 EDF0			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:26	Reserved	-	-	-
25	S_RESET_ST	Indicates whether the processor has been reset since the last read of DHCSR: 0 = No reset since last DHCSR read. 1 = At least one reset since last DHCSR read. This is a sticky bit, that clears to 0 on a read of DHCSR. [31:16] DBGKEY WO Debug key: Software must write 0xA05F to this field to enable write accesses to bits [15:0], otherwise the processor ignores the write access.	RO	0
24	S_RETIRE_ST	Indicates whether the processor has completed the execution of an instruction since the last read of DHCSR: 0 = No instruction retired since last DHCSR read. 1 = At least one instruction retired since last DHCSR read. This is a sticky bit, that clears to 0 on a read of DHCSR. A debugger can check this bit to determine if the processor is stalled on a load, store or fetch access. This bit is UNKNOWN after a Power-on or Local reset, but then is set to 1 as soon as the processor executes and retires an instruction.	RO	0
23:20	Reserved	-	-	-
19	S_LOCKUP	Indicates whether the processor is locked up because of an unrecoverable exception: 0 = Not locked up 1 = Locked up This bit can only be read as 1 by a remote debugger, using the DAP. The value of 1 indicates that the processor is running but locked up. The bit clears to 0 when the processor enters Debug	RO	0

		state.		
18	S_SLEEP	Indicates whether the processor is sleeping: 0 = Not sleeping. 1 = Sleeping. The debugger must set the C_HALT bit to 1 to gain control, or wait for an interrupt or other wake up event to wake up the system.	RO	0
17	S_HALT	Indicates whether the processor is in Debug state: 0 = Not in Debug state. 1 = In Debug state.	RO	0
16	S_REGRDY	A handshake flag for transfers through the DCRDR: • Writing to DCRSR clears the bit to 0. • Completion of the DCRDR transfer then sets the bit to 1. 0 = There has been a write to the DCRDR, but the transfer is not complete 1 = The transfer to or from the DCRDR is complete. This bit is valid only when the processor is in Debug state, otherwise the bit is UNKNOWN.	RO	0
15:6	Reserved	-	-	-
5	C_SNAPSTALL	If the processor is stalled on a load or store operation, a debugger can set this bit to 1 to attempt to break the stall. The effect of this bit is: 0 = No action 1 = Attempt to force any stalled load or store instruction to complete. The effect of setting this bit to 1 is UNPREDICTABLE unless the DHCSR write also sets C_DEBUGEN and C_HALT to 1. This means that if the processor is not already in Debug state it enters Debug state when the stalled instruction completes. Writing 1 to this bit makes the state of the memory system UNPREDICTABLE. Therefore, if a debugger writes 1 to this bit it must reset the processor before leaving Debug state. • A debugger can write to the DHCSR to clear this bit to 0. However, this does not remove the UNPREDICTABLE state of the memory system caused by setting C_SNAPSTALL to 1. • The architecture does not guarantee that setting this bit to 1 will force a stalled load or store operation to complete A Power-on reset sets this bit to 0.	RW modify	0

4	Reserved	-	-	-
3	C_MASKINTS	When debug is enabled, the debugger can write to this bit to mask PendSV, SysTick and external configurable interrupts: 0 = Do not mask. 1 = Mask PendSV, SysTick and external configurable interrupts. The effect of any attempt to change the value of this bit is UNPREDICTABLE unless both: • before the write to DHCSR, the value of the C_HALT bit is 1 • the write to the DHCSR that changes the C_MASKINTS bit also writes 1 to the C_HALT bit. This means that a single write to DHCSR cannot set the C_HALT to 0 and change the value of the C_MASKINTS bit. The bit does not affect NMI. When DHCSR.C_DEBUGEN is set to 0,the value of this bit is UNKNOWN. This bit is UNKNOWN after a Power-on reset.	RW modify	0
2	C_STEP	Processor step bit. The effects of writes to this bit are: 0 = No effect. 1 = Step the processor. This bit is UNKNOWN after a Power-on reset.	RW modify	0
1	C_HALT	Processor halt bit. The effects of writes to this bit are: 0 = No effect. 1 = Halt the processor. This bit is UNKNOWN after a Power-on reset	RW modify	0
0	C_DEBUGEN	Halting debug enable bit: 0 = Disabled. 1 = Enabled. If a debugger writes to DHCSR to change the value of this bit from 0 to 1, it must also write 0 to the C_MASKINTS bit, otherwise behavior is UNPREDICTABLE. This bit can only be set to 1 from the DAP, it cannot be set to 1 under software control. This bit is 0 after a Power-on reset.	RW modify	0

6.154. DCRSR

DCRSR			
Description	Debug Core Register Selector Register		
Address Region	cm4	**Type:**	RW
Offset	0x0 EDF4		
Physical address View0	0xE000 EDF4		
Physical address View1	-		

Bit field Details

Bits	Name	Description	Access	Reset
31:17	Reserved	-	-	-
16	REGWnR	Specifies the access type for the transfer: 0 = Read 1 = Write	RW modify	0
15:7	Reserved	-	-	-
6:0	REGSEL	Specifies the ARM core register, special-purpose register, or Floating-point extension register, to transfer: 0b0000000-0b0001100 ARM core registers R0-R12. For example, 0b0000000 specifies R0, and 0b0000101 specifies R5. 0b0001101 The current SP. See also values 0b0010001 and 0b0010010. 0b0001110 LR. 0b0001111 DebugReturnAddress. 0b0010000 xPSR. 0b0010001 Main stack pointer, MSP. 0b0010010 Process stack pointer, PSP. 0b0010100 Bits [31:24] CONTROL Bits [23:16] FAULTMASK Bits [15:8] BASEPRI Bits [7:0] PRIMASK. In each field, the valid bits are packed with leading zeros. For example, FAULTMASK is always a single bit, DCRDR[16], and DCRDR[23:17] is 0b0000000. 0b0100001 Floating-point Status and Control Register, FPSCR 0b1000000-0b1011111 FP registers S0-S31. For example, 0b1000000 specifies S0, and 0b1000101 specifies S5. All other values are Reserved. If the processor does not implement the FP extension the REGSEL field is bits [4:0], and bits [6:5] are Reserved, SBZ	RW modify	0x00

6.155. DCRDR

DCRDR			
Description	Debug Core Register Data Register		
Address Region	cm4	**Type:**	RW
Offset	0x0 EDF8		
Physical address View0	0xE000 EDF8		
Physical address View1	-		

Bit field Details

Bits	Name	Description	Access	Reset
31:0	DBGTMP	Data temporary cache, for reading and writing the ARM core registers, special-purpose registers, and Floating-point extension registers. The value of this register is UNKNOWN: • on reset • if the processor is in Debug state, the debugger has written to DCRSR since entering Debug state and DHCSR.S_REGRDY is set to 0.	RW modify	0x0000 0000

6.156. DEMCR

DEMCR			
Description	Debug Exception and Monitor Control Register		
Address Region	cm4	**Type:**	RW
Offset	0x0 EDFC		
Physical address View0	0xE000 EDFC		
Physical address View1	-		

Bit field Details

Bits	Name	Description	Access	Reset
31:25	Reserved	-	-	-
24	TRCENA	Global enable for all DWT and ITM features: 0 = DWT and ITM blocks disabled. 1 = DWT and ITM blocks enabled. If the DWT and ITM blocks are not implemented, this bit is UNK/SBZP. When TRCENA is set to 0: • DWT registers return UNKNOWN values on reads. Whether the processor ignores writes to the DWT unit is IMPLEMENTATION DEFINED. • ITM registers return UNKNOWN values on reads. Whether the processor ignores writes to the ITM unit is IMPLEMENTATION DEFINED. Setting this bit to 0 might not stop all events. To ensure all events are stopped, software must set all DWT and ITM feature enable bits to 0, and then set this bit to 0. The effect of this bit on the TPIU, ETM, and other system trace components is IMPLEMENTATION DEFINED.	RW modify	0
23:20	Reserved	-	-	-
19	MON_REQ	Debug Monitor semaphore bit. The processor does not use this bit. The monitor software defines the meaning and use of this bit.	RW modify	0
18	MON_STEP	When MON_EN is set to 0, this feature is disabled and the processor ignores MON_STEP. When MON_EN is set to 1, the meaning of MON_STEP is: 0 = Do not step the processor. 1 = Step the processor. Setting this bit to 1 makes the step request pending. The request becomes active when the processor returns from the Debug Monitor handler to the code being debugged. The effect of setting this bit to 1 is UNPREDICTABLE if the code being debugged is executing at an execution priority that is lower than the priority of the Debug Monitor exception.	RW modify	0
17	MON_PEND	Sets or clears the pending state of the	RW	0

		Debug Monitor exception: 0 = Clear the status of the Debug Monitor exception to not pending. 1 = Set the status of the Debug Monitor exception to pending. When the Debug Monitor exception is pending it becomes active subject to the exception priority rules. A debugger can use this bit to wake up the monitor using the DAP. The effect of setting this bit to 1 is not affected by the value of the MON_EN bit. A debugger can set MON_PEND to 1, and force the processor to take a Debug Monitor exception, even when MON_EN is set to 0.	modify	
16	MON_EN	Enable the Debug Monitor exception: 0 = Debug Monitor exception disabled. 1 = Debug Monitor exception enabled, If DHCSR.C_DEBUGEN is set to 1, the processor ignores the value of this bit.	RW modify	0
15:11	Reserved	-	-	-
10	VC_HARDERR	Enable halting debug trap on a Hard Fault exception. 0 = Halting debug trap disabled. 1 = Halting debug trap enabled. If DHCSR.C_DEBUGEN is set to 0, the processor ignores the value of this bit.	RW modify	0
9	VC_INTERR	Enable halting debug trap on a fault occurring during exception entry or exception return. 0 = Halting debug trap disabled. 1 = Halting debug trap enabled. If DHCSR.C_DEBUGEN is set to 0, the processor ignores the value of this bit.	RW modify	0
8	VC_BUSERR	Enable halting debug trap on a Bus Fault exception. 0 = Halting debug trap disabled. 1 = Halting debug trap enabled. If DHCSR.C_DEBUGEN is set to 0, the processor ignores the value of this bit.	RW modify	0
7	VC_STATERR	Enable halting debug trap on a Usage Fault exception caused by a state information error, for example an Undefined Instruction exception. 0 = Halting debug trap disabled. 1 = Halting debug trap enabled. If DHCSR.C_DEBUGEN is set to 0, the processor ignores the value of this bit.	RW modify	0
6	VC_CHKERR	Enable halting debug trap on a Usage Fault exception caused by a checking error, for example an alignment check error. 0 = Halting debug trap disabled. 1 = Halting debug trap enabled. If DHCSR.C_DEBUGEN is set to 0, the processor ignores the value of this bit.	RW modify	0
5	VC_NOCPERR	Enable halting debug trap on a Usage Fault caused by an access to a Coprocessor.	RW modify	0

		0 = Halting debug trap disabled. 1 = Halting debug trap enabled. If DHCSR.C_DEBUGEN is set to 0, the processor ignores the value of this bit.		
4	VC_MMERR	Enable halting debug trap on a MemManage exception. 0 = Halting debug trap disabled. 1 = Halting debug trap enabled. If DHCSR.C_DEBUGEN is set to 0, the processor ignores the value of this bit.	RW modify	0
3:1	Reserved	-	-	-
0	VC_CORERESET	Enable Reset Vector Catch. This causes a Local reset to halt a running system. 0 = Reset Vector Catch disabled. 1 = Reset Vector Catch enabled. If DHCSR.C_DEBUGEN is set to 0, the processor ignores the value of this bit.	RW modify	0

6.157. STIR

STIR			
Description	Software Trigger Interrupt Register		
Address Region	cm4	**Type:**	RW
Offset	0x0 EF00		
Physical address View0	0xE000 EF00		
Physical address View1	-		

Bit field Details

Bits	Name	Description	Access	Reset
31:9	Reserved	-	-	-
8:0	INTID	Interrupt ID of the interrupt to trigger, in the range 0-239. For example, a value of 0x03 specifies interrupt IRQ3.	RW modify	0x000

6.158. FPCCR

FPCCR			
Description	Floating-point Context Control Register		
Address Region	cm4	**Type:**	RW
Offset	0x0 EF34		
Physical address View0	0xE000 EF34		
Physical address View1	-		

Bit field Details

Bits	Name	Description	Access	Reset
31	ASPEN	Enables CONTROL<2> setting on execution of a floating-point instruction. This results in automatic hardware state preservation and restoration, for floating-point context, on exception entry and exit. 0 = Disable CONTROL<2> setting on execution of a floating-point instruction.	RW modify	1

		1 = Enable CONTROL<2> setting on execution of a floating-point instruction.		
30	LSPEN	0 = Disable automatic lazy state preservation for floating-point context. 1 = Enable automatic lazy state preservation for floating-point context.	RW modify	1
29:9	Reserved	-	-	-
8	MONRDY	0 = Debug Monitor is disabled or priority did not permit setting MON_PEND when the floating-point stack frame was allocated. 1 = Debug Monitor is enabled and priority permits setting MON_PEND when the floating-point stack frame was allocated.	RW modify	0
7	Reserved	-	-	-
6	BFRDY	0 = Bus Fault is disabled or priority did not permit setting the Bus Fault handler to the pending state when the floating-point stack frame was allocated. 1 = Bus Fault is enabled and priority permitted setting the Bus Fault handler to the pending state when the floating-point stack frame was allocated.	RW modify	0
5	MMRDY	0 = MemManage is disabled or priority did not permit setting the MemManage handler to the pending state when the floating-point stack frame was allocated. 1 = MemManage is enabled and priority permitted setting the MemManage handler to the pending state when the floating-point stack frame was allocated.	RW modify	0
4	HFRDY	0 = Priority did not permit setting the Hard Fault handler to the pending state when the floating-point stack frame was allocated. 1 = Priority permitted setting the Hard Fault handler to the pending state when the floating-point stack frame was allocated.	RW modify	0
3	THREAD	0 = Mode was not Thread Mode when the floating-point stack frame was allocated. 1 = Mode was Thread Mode when the floating-point stack frame was allocated.	RW modify	0
2	Reserved	-	-	-
1	USER	0 = Privilege level was not user when the floating-point stack frame was allocated. 1 = Privilege level was user when the	RW modify	0

		floating-point stack frame was allocated.		
0	LSPACT	0 = Lazy state preservation is not active. 1 = Lazy state preservation is active. Floating-point stack frame has been allocated but saving state to it has been deferred.	RW modify	0

6.159. FPCAR

FPCAR			
Description	Floating-point Context Address Register		
Address Region	cm4	**Type:**	RW
Offset	0x0 EF38		
Physical address View0	0xE000 EF38		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:3	ADDRESS	The location of the unpopulated floating-point register space allocated on an exception stack frame.	RW modify	0x0000 0000
2:0	Reserved	-	-	-

6.160. FPDSCR

FPDSCR			
Description	Floating-point Default Status Control Register		
Address Region	cm4	**Type:**	RW
Offset	0x0 EF3C		
Physical address View0	0xE000 EF3C		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:27	Reserved	-	-	-
26	AHP	Default value for FPSCR.AHP	RW modify	0
25	DN	Default value for FPSCR.DN	RW modify	0
24	FZ	Default value for FPSCR.FZ	RW modify	0
23:22	RMode	Default value for FPSCR.RMode	RW modify	0b00
21:0	Reserved	-	-	-

6.161. MVFR0

MVFR0				
Description	Media and VFP Feature Register 0			
Address Region	cm4	**Type:**	RO	
Offset	0x0 EF40			
Physical address View0	0xE000 EF40			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	MVFR0	Media and VFP Feature Register 0	RO	0x1011 0021

6.162. MVFR1

MVFR1				
Description	Media and VFP Feature Register 1			
Address Region	cm4	**Type:**	RO	
Offset	0x0 EF44			
Physical address View0	0xE000 EF44			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	MVFR1	Media and VFP Feature Register 1	RO	0x1100 0011

6.163. SCS_PERIPHERAL_ID4

SCS_PERIPHERAL_ID4				
Description	ROM table components Peripheral ID4			
Address Region	cm4	**Type:**	RO	
Offset	0x0 EFD0			
Physical address View0	0xE000 EFD0			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	SCS_PERIPHERAL_ID4	Peripheral ID4	RO	0x0000 0004

6.164. SCS_PERIPHERAL_ID0

SCS_PERIPHERAL_ID0				
Description	ROM table components Peripheral ID0			
Address Region	cm4	**Type:**	RO	
Offset	0x0 EFE0			
Physical address View0	0xE000 EFE0			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	SCS_PERIPHERAL_ID0	Peripheral ID0	RO	0x0000 000C

6.165. SCS_PERIPHERAL_ID1

SCS_PERIPHERAL_ID1				
Description	ROM table components Peripheral ID1			
Address Region	cm4	**Type:**	RO	
Offset	0x0 EFE4			
Physical address View0	0xE000 EFE4			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	SCS_PERIPHERAL_ID1	Peripheral ID1	RO	0x0000 00B0

6.166. SCS_PERIPHERAL_ID2

SCS_PERIPHERAL_ID2				
Description	ROM table components Peripheral ID2			
Address Region	cm4	**Type:**	RO	
Offset	0x0 EFE8			
Physical address View0	0xE000 EFE8			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	SCS_PERIPHERAL_ID2	Peripheral ID2	RO	0x0000 000B

6.167. SCS_PERIPHERAL_ID3

SCS_PERIPHERAL_ID3			
Description	ROM table components Peripheral ID3		
Address Region	cm4	**Type:**	RO
Offset	0x0 EFEC		
Physical address View0	0xE000 EFEC		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	SCS_PERIPHERAL_ID3	Peripheral ID3	RO	0x0000 0000

6.168. SCS_COMPONENT_ID0

SCS_COMPONENT_ID0			
Description	ROM table components Component ID0		
Address Region	cm4	**Type:**	RO
Offset	0x0 EFF0		
Physical address View0	0xE000 EFF0		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	SCS_COMPONENT_ID0	Component ID0	RO	0x0000 000D

6.169. SCS_COMPONENT_ID1

SCS_COMPONENT_ID1			
Description	ROM table components Component ID1		
Address Region	cm4	**Type:**	RO
Offset	0x0 EFF4		
Physical address View0	0xE000 EFF4		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	SCS_COMPONENT_ID1	Component ID1	RO	0x0000 00E0

6.170. SCS_COMPONENT_ID2

SCS_COMPONENT_ID2					
Description	ROM table components Component ID2				
Address Region	cm4		**Type:**	RO	
Offset	0x0 EFF8				
Physical address View0	0xE000 EFF8				
Physical address View1	-				
Bit field Details					
Bits	**Name**	**Description**		**Access**	**Reset**
31:0	SCS_COMPONENT_ID2	Component ID2		RO	0x0000 0005

6.171. SCS_COMPONENT_ID3

SCS_COMPONENT_ID3					
Description	ROM table components Component ID3				
Address Region	cm4		**Type:**	RO	
Offset	0x0 EFFC				
Physical address View0	0xE000 EFFC				
Physical address View1	-				
Bit field Details					
Bits	**Name**	**Description**		**Access**	**Reset**
31:0	SCS_COMPONENT_ID3	Component ID3		RO	0x0000 00B1

6.172. TPIU_SSPSR

TPIU_SSPSR					
Description	Supported Parallel Port Sizes Register				
Address Region	cm4		**Type:**	RO	
Offset	0x4 0000				
Physical address View0	0xE004 0000				
Physical address View1	-				
Bit field Details					
Bits	**Name**	**Description**		**Access**	**Reset**
31:0	SWIDTH	SWIDTH[N] represents a trace port width of (N+1). The meaning of each bit is: 0 = Width (N+1) not supported. 1 = Width (N+1) supported.		RO	-

6.173. TPIU_CSPSR

TPIU_CSPSR			
Description	Current Parallel Port Size Register		
Address Region	cm4	**Type:**	RW
Offset	0x4 0004		
Physical address View0	0xE004 0004		
Physical address View1	-		

Bit field Details

Bits	Name	Description	Access	Reset
31:0	CWIDTH	CWIDTH[N] represents a trace port width of (N+1). The meaning of each bit is: 0 = Width (N+1) is not the current trace port width. 1 = Width (N+1) is the current trace port width.	RW modify	0x0000 0001

6.174. TPIU_ACPR

TPIU_ACPR			
Description	Asynchronous Clock Prescaler Register		
Address Region	cm4	**Type:**	RW
Offset	0x4 0010		
Physical address View0	0xE004 0010		
Physical address View1	-		

Bit field Details

Bits	Name	Description	Access	Reset
31:13	Reserved	-	-	-
12:0	PRESCALER	Divisor for TRACECLKIN is Prescaler + 1.	RW modify	0x0000

6.175. TPIU_SPPR

TPIU_SPPR			
Description	Selected Pin Protocol Register		
Address Region	cm4	**Type:**	RW
Offset	0x4 00F0		
Physical address View0	0xE004 00F0		
Physical address View1	-		

Bit field Details

Bits	Name	Description	Access	Reset
31:2	Reserved	-	-	-
1:0	TXMODE	Specified the protocol for trace output from the TPIU. Permitted values are: 0b00 = Parallel trace port mode. 0b01 = Asynchronous SWO, using Manchester encoding. 0b10 = Asynchronous SWO, using	RW modify	0b01

		NRZ encoding. The value 0b11 is reserved. The effect of selecting a reserved value, or a mode that the implementation does not support, is UNPREDICTABLE.		

6.176. TPIU_FFSR

TPIU_FFSR			
Description	Formatter and Flush Status Register		
Address Region	cm4	**Type:**	RO
Offset	0x4 0300		
Physical address View0	0xE004 0300		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:4	Reserved	-	-	-
3	FtNonStop	Formatter cannot be stopped	RO	1
2	TCPresent	This bit always reads zero	RO	0
1	FtStopped	This bit always reads zero	RO	0
0	FlInProg	This bit always reads zero	RO	0

6.177. TPIU_FFCR

TPIU_FFCR			
Description	Formatter and Flush Control Register		
Address Region	cm4	**Type:**	RW
Offset	0x4 0304		
Physical address View0	0xE004 0304		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:9	Reserved	-	-	-
8	TrigIn	This bit Reads-As-One (RAO), specifying that triggers are inserted when a trigger pin is asserted.	RW modify	1
7:2	Reserved	-	-	-
1	EnFCont	Enable continuous formatting. Value can be: 0 = Continuous formatting disabled. 1 = Continuous formatting enabled.	RW modify	1
0	Reserved	-	-	-

6.178. TPIU_FSCR

TPIU_FSCR				
Description	Formatter Synchronization Counter Register			
Address Region	cm4	**Type:**	RO	
Offset	0x4 0308			
Physical address View0	0xE004 0308			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	TPIU_FSCR	Formatter Synchronization Counter Register	RO	0x0000 0000

6.179. TPIU_TRIGGER

TPIU_TRIGGER				
Description	TRIGGER			
Address Region	cm4	**Type:**	RO	
Offset	0x4 0EE8			
Physical address View0	0xE004 0EE8			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	TRIGGER_input_value	When read, this bit returns the TRIGGER input.	RO	0

6.180. TPIU_FIFO_DATA0

TPIU_FIFO_DATA0				
Description	Integration ETM Data			
Address Region	cm4	**Type:**	RO	
Offset	0x4 0EEC			
Physical address View0	0xE004 0EEC			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:30	Reserved	-	-	-
29	ITM_ATVALID_input	Returns the value of the ITM ATVALID signal	RO	0
28:27	ITM_byte_count	Number of bytes of ITM trace data since last read of Integration ITM Data Register.	RO	0b00
26	ETM_ATVALID_input	Not used.	RO	0
25:24	ETM_byte_count	Not used.	RO	0b00
23:16	ETM_data_2	Not used.	RO	0x00
15:8	ETM_data_1	Not used.	RO	0x00
7:0	ETM_data_0	Not used.	RO	0x00

6.181. TPIU_ITATBCTR2

TPIU_ITATBCTR2			
Description	ITATBCTR2		
Address Region	cm4	**Type:**	RO
Offset	0x4 0EF0		
Physical address View0	0xE004 0EF0		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	ATREADY1_ATREADY2	This bit sets the value of both the ETM and ITM ATREADY outputs, if the TPIU is in integration test mode.	RO	0

6.182. TPIU_ITATBCTR0

TPIU_ITATBCTR0			
Description	ITATBCTR0		
Address Region	cm4	**Type:**	RO
Offset	0x4 0EF8		
Physical address View0	0xE004 0EF8		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	ATVALID1_ATVALID2	A read of this bit returns the value of ATVALIDS1 OR-ed with ATVALIDS2.	RO	0

6.183. TPIU_FIFO_DATA1

TPIU_FIFO_DATA1			
Description	Integration ITM Data		
Address Region	cm4	**Type:**	RO
Offset	0x4 0EFC		
Physical address View0	0xE004 0EFC		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:30	Reserved	-	-	-
29	ITM_ATVALID_input	Returns the value of the ITM ATVALID signal	RO	0
28:27	ITM_byte_count	Number of bytes of ITM trace data since last read of Integration ITM Data Register.	RO	0b00
26	ETM_ATVALID_input	Not used.	RO	0
25:24	ETM_byte_count	Not used.	RO	0b00
23:16	ITM_data_2	ITM trace data. The TPIU discards this data when the register is read.	RO	0x00

15:8	ITM_data_1	ITM trace data. The TPIU discards this data when the register is read.	RO	0x00
7:0	ITM_data_0	ITM trace data. The TPIU discards this data when the register is read.	RO	0x00

6.184. TPIU_ITCTRL

TPIU_ITCTRL			
Description	Integration Mode Control		
Address Region	cm4	**Type:**	RW
Offset	0x4 0F00		
Physical address View0	0xE004 0F00		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:2	Reserved	-	-	-
1:0	Mode	Specifies the current mode for the TPIU: 0b00 normal mode 0b01 integration test mode 0b10 integration data test mode 0b11 Reserved. In integration data test mode, the trace output is disabled, and data can be read directly from each input port using the integration data registers	RW	0x0

6.185. TPIU_CLAIMSET

TPIU_CLAIMSET			
Description	Claim tag set		
Address Region	cm4	**Type:**	RW
Offset	0x4 0FA0		
Physical address View0	0xE004 0FA0		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	CLAIMSET	Claim tag set	RW modify	0x0000 000F

6.186. TPIU_CLAIMCLR

TPIU_CLAIMCLR			
Description	Claim tag clear		
Address Region	cm4	**Type:**	RW
Offset	0x4 0FA4		
Physical address View0	0xE004 0FA4		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	CLAIMCLR	Claim tag clear	RW modify	0x0000 0000

6.187. TPIU_DEVID

TPIU_DEVID			
Description	TPIU_DEVID		
Address Region	cm4	**Type:**	RO
Offset	0x4 0FC8		
Physical address View0	0xE004 0FC8		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:12	Reserved	-	-	-
11	Asynchronous_Serial_Wire_Output_NRZ	This bit Reads-As-One (RAO), indicating that the output is supported.	RO	1
10	Asynchronous_Serial_Wire_Output_Manchester	This bit Reads-As-One (RAO), indicating that the output is supported.	RO	1
9	Tracedata_and_clock_modes	This bit Reads-As-Zero (RAZ), indicating that trace data and clock modes are supported	RO	0
8:6	Minimum_buffer_size	Specifies the minimum TPIU buffer size: 0b010 = 4 bytes	RO	0b010
5	Asynchronous_TRACECLKIN	Specifies whether TRACECLKIN can be asynchronous to CLK 0 = TRACECLKIN must be synchronous to CLK 1 = TRACECLKIN can be asynchronous to CLK	RO	1
4:0	Number_of_trace_inputs	Specifies the number of trace inputs: 0b000000 = 1 input 0b000001 = 2 inputs If your implementation includes an ETM, the value of this field is 0b000001	RO	0x00

6.188. TPIU_DEVTYPE

TPIU_DEVTYPE			
Description	TPIU_DEVTYPE		
Address Region	cm4	**Type:**	RO
Offset	0x4 0FCC		
Physical address View0	0xE004 0FCC		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:4	Sub_type	Sub type	RO	0x1
3:0	Major_type	Major type	RO	0x1

6.189. TPIU_PID4

TPIU_PID4			
Description	TPIU components Peripheral ID4		
Address Region	cm4	**Type:**	RO
Offset	0x4 0FD0		
Physical address View0	0xE004 0FD0		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	TPIU_PID4	Peripheral ID4	RO	0x0000 0004

6.190. TPIU_PID5

TPIU_PID5			
Description	TPIU components Peripheral ID5		
Address Region	cm4	**Type:**	RO
Offset	0x4 0FD4		
Physical address View0	0xE004 0FD4		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	TPIU_PID5	Peripheral ID5	RO	0x0000 0000

6.191. TPIU_PID6

TPIU_PID6				
Description	TPIU components Peripheral ID6			
Address Region	cm4	**Type:**	RO	
Offset	0x4 0FD8			
Physical address View0	0xE004 0FD8			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	TPIU_PID6	Peripheral ID6	RO	0x0000 0000

6.192. TPIU_PID7

TPIU_PID7				
Description	TPIU components Peripheral ID7			
Address Region	cm4	**Type:**	RO	
Offset	0x4 0FDC			
Physical address View0	0xE004 0FDC			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	TPIU_PID7	Peripheral ID7	RO	0x0000 0000

6.193. TPIU_PID0

TPIU_PID0				
Description	TPIU components Peripheral ID0			
Address Region	cm4	**Type:**	RO	
Offset	0x4 0FE0			
Physical address View0	0xE004 0FE0			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	TPIU_PID0	Peripheral ID0	RO	0x0000 00A1

6.194. TPIU_PID1

TPIU_PID1				
Description	TPIU components Peripheral ID1			
Address Region	cm4	**Type:**	RO	
Offset	0x4 0FE4			
Physical address View0	0xE004 0FE4			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	TPIU_PID1	Peripheral ID1	RO	0x0000 00B9

6.195. TPIU_PID2

TPIU_PID2				
Description	TPIU components Peripheral ID2			
Address Region	cm4	**Type:**	RO	
Offset	0x4 0FE8			
Physical address View0	0xE004 0FE8			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	TPIU_PID2	Peripheral ID2	RO	0x0000 000B

6.196. TPIU_PID3

TPIU_PID3				
Description	TPIU components Peripheral ID3			
Address Region	cm4	**Type:**	RO	
Offset	0x4 0FEC			
Physical address View0	0xE004 0FEC			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	TPIU_PID3	Peripheral ID3	RO	0x0000 0000

6.197. TPIU_CID0

TPIU_CID0				
Description	TPIU components Component ID0			
Address Region	cm4	**Type:**	RO	
Offset	0x4 0FF0			
Physical address View0	0xE004 0FF0			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	TPIU_CID0	Component ID0	RO	0x0000 000D

6.198. TPIU_CID1

TPIU_CID1				
Description	TPIU components Component ID1			
Address Region	cm4	**Type:**	RO	
Offset	0x4 0FF4			
Physical address View0	0xE004 0FF4			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	TPIU_CID1	Component ID1	RO	0x0000 0090

6.199. TPIU_CID2

TPIU_CID2				
Description	TPIU components Component ID2			
Address Region	cm4	**Type:**	RO	
Offset	0x4 0FF8			
Physical address View0	0xE004 0FF8			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	TPIU_CID2	Component ID2	RO	0x0000 0005

6.200. TPIU_CID3

TPIU_CID3				
Description	TPIU components Component ID3			
Address Region	cm4	**Type:**	RO	
Offset	0x4 0FFC			
Physical address View0	0xE004 0FFC			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	TPIU_CID3	Component ID3	RO	0x0000 00B1

6.201. SCS

SCS				
Description	ROM table components SCS			
Address Region	cm4	**Type:**	RO	
Offset	0xF F000			
Physical address View0	0xE00F F000			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	SCS	SCS	RO	0xFFF0 F003

6.202. DWT

DWT				
Description	ROM table components DWT			
Address Region	cm4	**Type:**	RO	
Offset	0xF F004			
Physical address View0	0xE00F F004			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	DWT	DWT	RO	0xFFF0 2003

6.203. FPB

FPB			
Description	ROM table components FPB		
Address Region	cm4	**Type:**	RO
Offset	0xF F008		
Physical address View0	0xE00F F008		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	FPB	FPB	RO	0xFFF0 3003

6.204. ITM

ITM			
Description	ROM table components ITM		
Address Region	cm4	**Type:**	RO
Offset	0xF F00C		
Physical address View0	0xE00F F00C		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	ITM	ITM	RO	0xFFF0 1003

6.205. TPIU

TPIU			
Description	ROM table components TPIU		
Address Region	cm4	**Type:**	RO
Offset	0xF F010		
Physical address View0	0xE00F F010		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	TPIU	TPIU	RO	0xFFF4 1003

6.206. ETM

ETM				
Description	ROM table components ETM			
Address Region	cm4	**Type:**	RO	
Offset	0xF F014			
Physical address View0	0xE00F F014			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	ETM	ETM	RO	0xFFF4 2002

6.207. END_MARKER

END_MARKER				
Description	ROM table components END_MARKER			
Address Region	cm4	**Type:**	RO	
Offset	0xF F018			
Physical address View0	0xE00F F018			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	END_MARKER	END_MARKER	RO	0x0000 0000

6.208. SYSTEM_ACCESS

SYSTEM_ACCESS				
Description	ROM table components SYSTEM_ACCESS			
Address Region	cm4	**Type:**	RO	
Offset	0xF FFCC			
Physical address View0	0xE00F FFCC			
Physical address View1	-			
Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	SYSTEM_ACCESS	SYSTEM_ACCESS	RO	0x0000 0001

6.209. PERIPHERAL_ID4

PERIPHERAL_ID4			
Description	ROM table components Peripheral ID4		
Address Region	cm4	**Type:**	RO
Offset	0xF FFD0		
Physical address View0	0xE00F FFD0		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	PERIPHERAL_ID4	Peripheral ID4	RO	0x0000 0004

6.210. PERIPHERAL_ID5

PERIPHERAL_ID5			
Description	ROM table components Peripheral ID5		
Address Region	cm4	**Type:**	RO
Offset	0xF FFD4		
Physical address View0	0xE00F FFD4		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	PERIPHERAL_ID5	Peripheral ID5	RO	0x0000 0000

6.211. PERIPHERAL_ID6

PERIPHERAL_ID6			
Description	ROM table components Peripheral ID6		
Address Region	cm4	**Type:**	RO
Offset	0xF FFD8		
Physical address View0	0xE00F FFD8		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	PERIPHERAL_ID6	Peripheral ID6	RO	0x0000 0000

6.212. PERIPHERAL_ID7

PERIPHERAL_ID7			
Description	ROM table components Peripheral ID7		
Address Region	cm4	**Type:**	RO
Offset	0xF FFDC		
Physical address View0	0xE00F FFDC		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	PERIPHERAL_ID7	Peripheral ID7	RO	0x0000 0000

6.213. PERIPHERAL_ID0

PERIPHERAL_ID0			
Description	ROM table components Peripheral ID0		
Address Region	cm4	**Type:**	RO
Offset	0xF FFE0		
Physical address View0	0xE00F FFE0		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	PERIPHERAL_ID0	Peripheral ID0	RO	0x0000 00C4

6.214. PERIPHERAL_ID1

PERIPHERAL_ID1			
Description	ROM table components Peripheral ID1		
Address Region	cm4	**Type:**	RO
Offset	0xF FFE4		
Physical address View0	0xE00F FFE4		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	PERIPHERAL_ID1	Peripheral ID1	RO	0x0000 00B4

6.215. PERIPHERAL_ID2

PERIPHERAL_ID2			
Description	ROM table components Peripheral ID2		
Address Region	cm4	**Type:**	RO
Offset	0xF FFE8		
Physical address View0	0xE00F FFE8		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	PERIPHERAL_ID2	Peripheral ID2	RO	0x0000 000B

6.216. PERIPHERAL_ID3

PERIPHERAL_ID3			
Description	ROM table components Peripheral ID3		
Address Region	cm4	**Type:**	RO
Offset	0xF FFEC		
Physical address View0	0xE00F FFEC		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	PERIPHERAL_ID3	Peripheral ID3	RO	0x0000 0000

6.217. COMPONENT_ID0

COMPONENT_ID0			
Description	ROM table components Component ID0		
Address Region	cm4	**Type:**	RO
Offset	0xF FFF0		
Physical address View0	0xE00F FFF0		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	COMPONENT_ID0	Component ID0	RO	0x0000 000D

6.218. COMPONENT_ID1

COMPONENT_ID1			
Description	ROM table components Component ID1		
Address Region	cm4	**Type:**	RO
Offset	0xF FFF4		
Physical address View0	0xE00F FFF4		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	COMPONENT_ID1	Component ID1	RO	0x0000 0010

6.219. COMPONENT_ID2

COMPONENT_ID2			
Description	ROM table components Component ID2		
Address Region	cm4	**Type:**	RO
Offset	0xF FFF8		
Physical address View0	0xE00F FFF8		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	COMPONENT_ID2	Component ID2	RO	0x0000 0005

6.220. COMPONENT_ID3

COMPONENT_ID3			
Description	ROM table components Component ID3		
Address Region	cm4	**Type:**	RO
Offset	0xF FFFC		
Physical address View0	0xE00F FFFC		
Physical address View1	-		

Bit field Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	COMPONENT_ID3	Component ID3	RO	0x0000 00B1

7. Revision History

Table 7.1 Revision History

Revision	Date	Description
0.1	2014-03-11	Newly released
0.2	2014-08-01	Added No.79 fpu exception Interrupt to 3. Cortex®-M4F interrupts map. Added 5.7 Trace clock enable section.
0.3	2014-09-29	Deleted Retention-shutdown from 5.4. Power mode section.
0.4	2014-10-07	Added 3.1 CPU Interrupts section. Rename 5.7 section title to Trace signal output enable.
0.5	2015-01-20	Added Table 3.2 Added 5.8 PMU initialization setting when connecting a debugger
1.0	2015-01-21	Official version.
1.1	2015-04-09	Changed cover.
1.2	2018-02-01	Changed header, footer and the last page. Changed corporate name and descriptions. Modified Arm logo and descriptions. Modified trademark description. Modified Table 3.2. Corrected typos.

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