

MOSFETs Silicon P-Channel MOS

# SSM3J338R

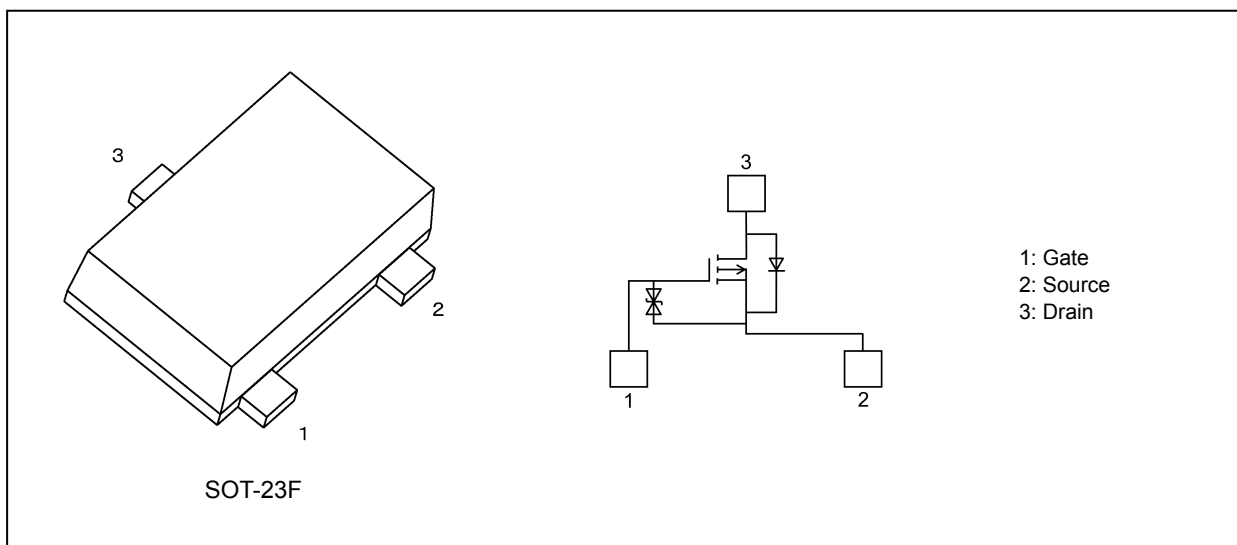
### 1. Applications

- Power Management Switches

### 2. Features

- (1) 1.8 V gate drive voltage.
- (2) Low drain-source on-resistance
  - :  $R_{DS(ON)} = 26.3 \text{ m}\Omega$  (typ.) (@ $V_{GS} = -1.8 \text{ V}$ )
  - $R_{DS(ON)} = 20.1 \text{ m}\Omega$  (typ.) (@ $V_{GS} = -2.5 \text{ V}$ )
  - $R_{DS(ON)} = 15.9 \text{ m}\Omega$  (typ.) (@ $V_{GS} = -4.5 \text{ V}$ )

### 3. Packaging and Pin Assignment



Start of commercial production  
2015-08

### 4. Absolute Maximum Ratings (Note) (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$ )

Characteristics	Symbol	Rating	Unit
Drain-source voltage	$V_{DSS}$	-12	V
Gate-source voltage	$V_{GSS}$	$\pm 10$	
Drain current (DC) (Note 1)	$I_D$	-6	A
Drain current (pulsed) (Note 1), (Note 2)	$I_{DP}$	-14	A
Power dissipation (Note 3)	$P_D$	1	W
Power dissipation $t \leq 10\text{s}$ (Note 3)	$P_D$	2	W
Channel temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage temperature	$T_{stg}$	-55 to 150	$^\circ\text{C}$

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Note 1: Ensure that the channel temperature does not exceed  $150\text{ }^\circ\text{C}$

Note 2: Pulse width (PW)  $\leq 10\text{ ms}$ , duty  $\leq 1\%$

Note 3: Device mounted on a FR4 board.

( $25.4\text{ mm} \times 25.4\text{ mm} \times 1.6\text{ mm}$ , Cu Pad :  $645\text{ mm}^2$ )

Note: The MOSFETs in this device are sensitive to electrostatic discharge. When handling this device, the worktables, operators, soldering irons and other objects should be protected against anti-static discharge.

Note: The channel-to-ambient thermal resistance,  $R_{th(ch-a)}$ , and the drain power dissipation,  $P_D$ , vary according to the board material, board area, board thickness and pad area. When using this device, be sure to take heat dissipation fully into account.

### 5. Thermal Characteristics

Characteristics	Symbol	Max	Unit
Channel-to-ambient thermal resistance (Note 1)	$R_{th(ch-a)}$	125	$^\circ\text{C/W}$

Note 1: Device mounted on an  $25.4\text{ mm} \times 25.4\text{ mm} \times 1.6\text{ mm}$  FR4 glass epoxy board (Cu pad:  $645\text{ mm}^2$ )

### 6. Electrical Characteristics

#### 6.1. Static Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$ )

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	$I_{GSS}$	$V_{GS} = \pm 8\text{ V}, V_{DS} = 0\text{ V}$	—	—	$\pm 1$	$\mu\text{A}$
Drain cut-off current	$I_{DSS}$	$V_{DS} = -12\text{ V}, V_{GS} = 0\text{ V}$	—	—	-1	$\mu\text{A}$
Drain-source breakdown voltage	$V_{(BR)DSS}$	$I_D = -1\text{ mA}, V_{GS} = 0\text{ V}$	-12	—	—	V
Drain-source breakdown voltage (Note 1)	$V_{(BR)DSX}$	$I_D = -1\text{ mA}, V_{GS} = 5\text{ V}$	-7	—	—	
Gate threshold voltage (Note 2)	$V_{th}$	$V_{DS} = -3\text{ V}, I_D = -1\text{ mA}$	-0.3	—	-1.0	
Drain-source on-resistance (Note 3)	$R_{DS(ON)}$	$I_D = -6.0\text{ A}, V_{GS} = -8.0\text{ V}$	—	13.9	17.6	m $\Omega$
		$I_D = -6.0\text{ A}, V_{GS} = -4.5\text{ V}$	—	15.9	20.2	
		$I_D = -6.0\text{ A}, V_{GS} = -3.6\text{ V}$	—	17.0	21.9	
		$I_D = -6.0\text{ A}, V_{GS} = -2.5\text{ V}$	—	20.1	27.9	
		$I_D = -4.5\text{ A}, V_{GS} = -1.8\text{ V}$	—	26.3	45.3	
Forward transfer admittance (Note 3)	$ Y_{fs} $	$V_{DS} = -3\text{ V}, I_D = -2\text{ A}$	—	17	—	S

Note 1: If a reverse bias is applied between gate and source, this device enters  $V_{(BR)DSX}$  mode. Note that the drain-source breakdown voltage is lowered in this mode.

Note 2: Let  $V_{th}$  be the voltage applied between gate and source that causes the drain current ( $I_D$ ) to below (-1 mA for this device). Then, for normal switching operation,  $V_{GS(ON)}$  must be higher than  $V_{th}$ , and  $V_{GS(OFF)}$  must be lower than  $V_{th}$ . This relationship can be expressed as:  $V_{GS(OFF)} < V_{th} < V_{GS(ON)}$ .

Take this into consideration when using the device.

Note 3: Pulse measurement.

#### 6.2. Dynamic Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$ )

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Input capacitance	$C_{iss}$	$V_{DS} = -6\text{ V}, V_{GS} = 0\text{ V},$ $f = 1\text{ MHz}$	—	1400	—	pF
Reverse transfer capacitance	$C_{rss}$		—	225	—	
Output capacitance	$C_{oss}$		—	250	—	
Switching time (turn-on time)	$t_{on}$	$V_{DD} = -6\text{ V}, I_D = -6\text{ A}$ $V_{GS} = 0\text{ to }-4.5\text{ V}, R_{GS} = 10\text{ }\Omega$	—	65	—	ns
Switching time (turn-off time)	$t_{off}$		—	383	—	

#### 6.3. Switching Time Test Circuit

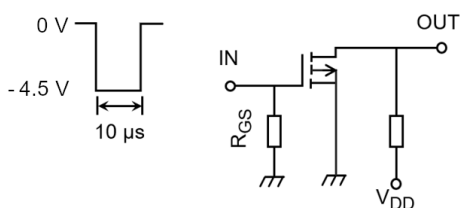


Fig. 6.3.1 Switching Time Test Circuit

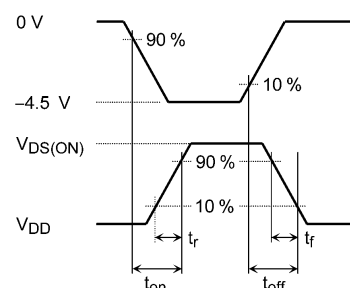


Fig. 6.3.2 Input Waveform/Output Waveform

#### 6.4. Gate Charge Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$ )

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Total gate charge (gate-source plus gate-drain)	$Q_g$	$V_{DD} = -6\text{ V}, V_{GS} = -4.5\text{ V},$ $I_D = -6\text{ A}$	—	19.5	—	nC
Gate-source charge 1	$Q_{gs1}$		—	1.4	—	
Gate-drain charge	$Q_{gd}$		—	9.0	—	

## 6.5. Source-Drain Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$ )

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Diode forward voltage (Note 1)	$V_{DSF}$	$I_{DR} = 6\text{ A}, V_{GS} = 0\text{ V}$	—	0.75	1.1	V

Note 1: Pulse measurement.

## 7. Marking

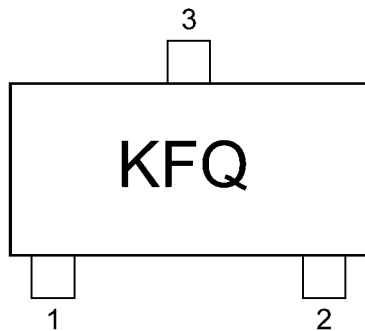
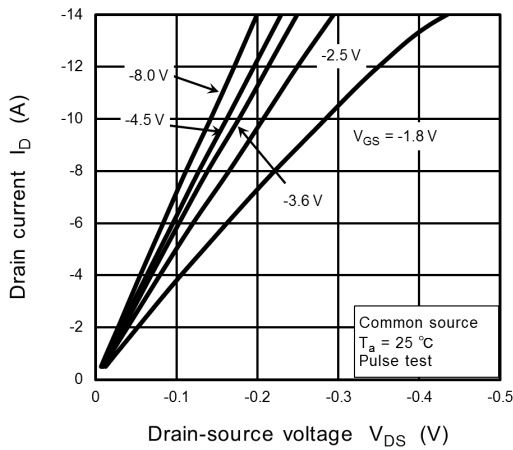
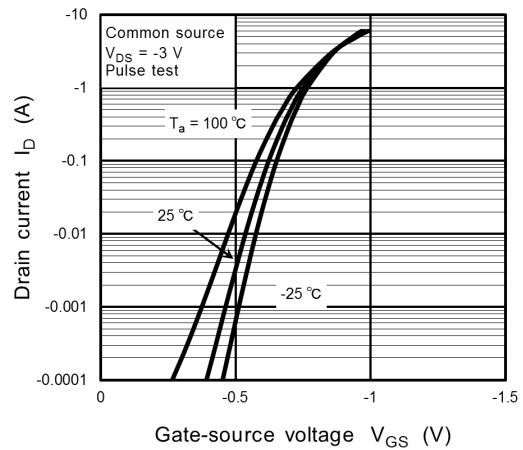


Fig. 7.1 Marking

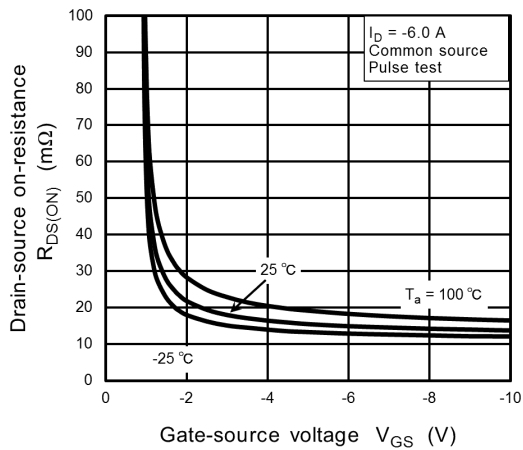
### 8. Characteristics Curves (Note)



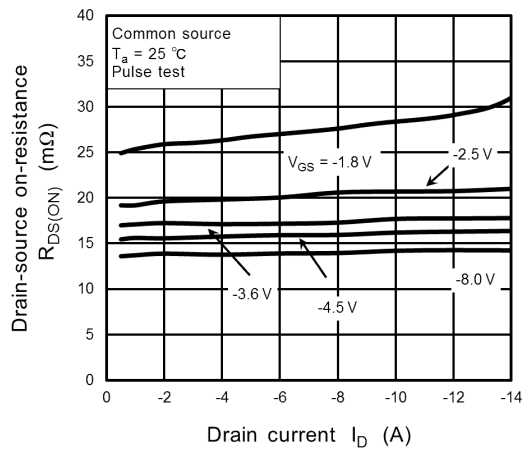
**Fig. 8.1**  $I_D - V_{DS}$



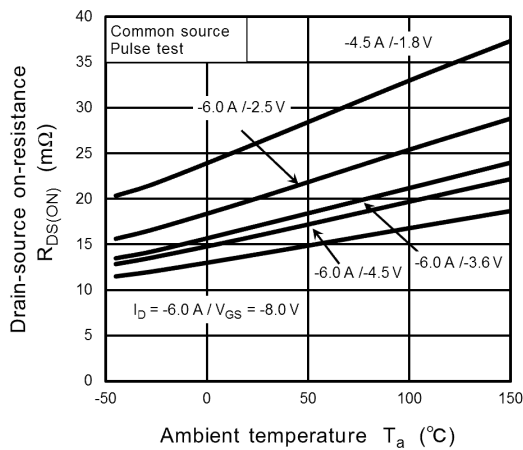
**Fig. 8.2**  $I_D - V_{GS}$



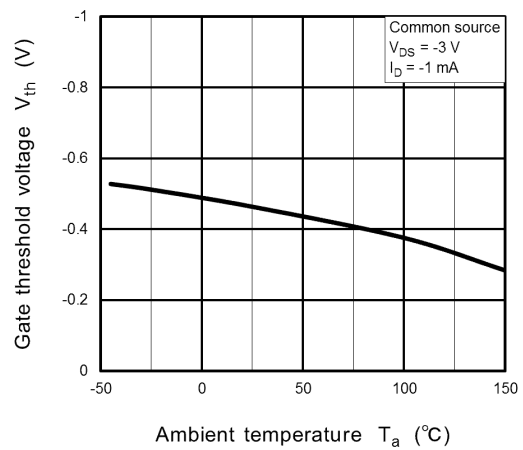
**Fig. 8.3**  $R_{DS(ON)} - V_{GS}$



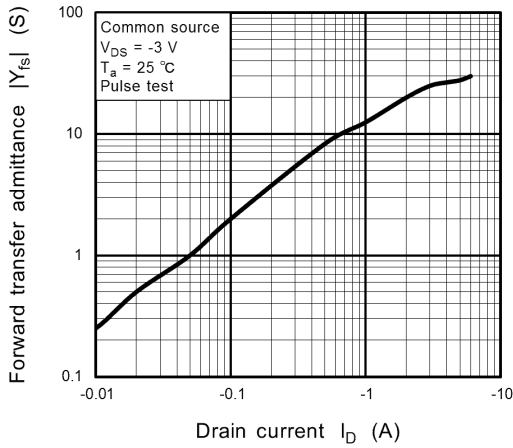
**Fig. 8.4**  $R_{DS(ON)} - I_D$



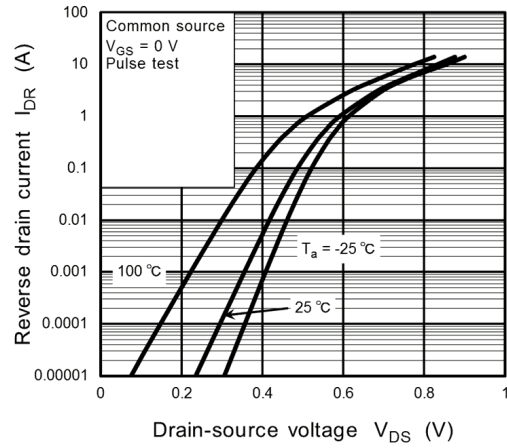
**Fig. 8.5**  $R_{DS(ON)} - T_a$



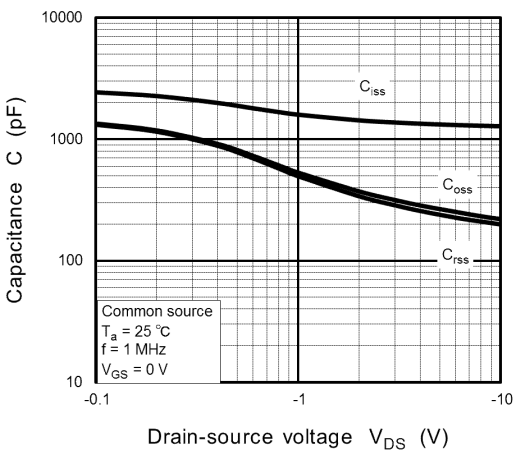
**Fig. 8.6**  $V_{th} - T_a$



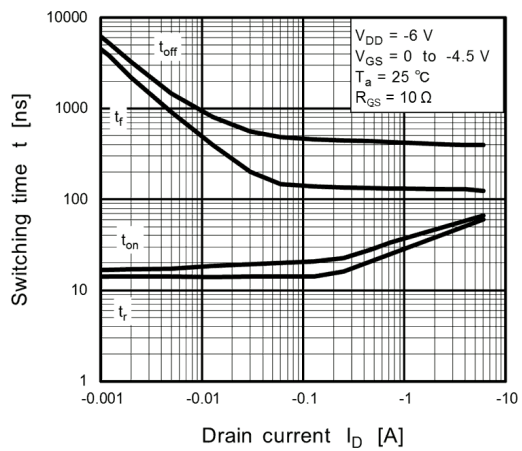
**Fig. 8.7**  $|Y_{fs}| - I_D$



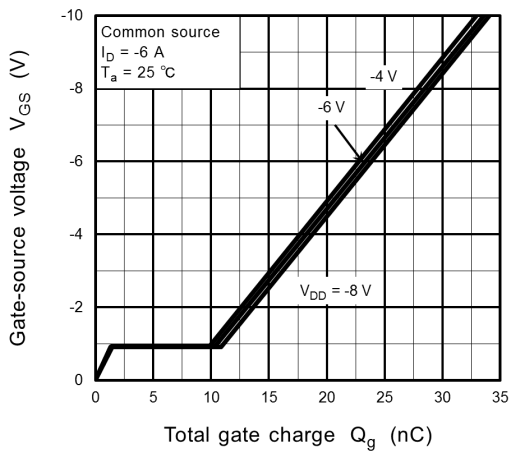
**Fig. 8.8**  $I_{DR} - V_{DS}$



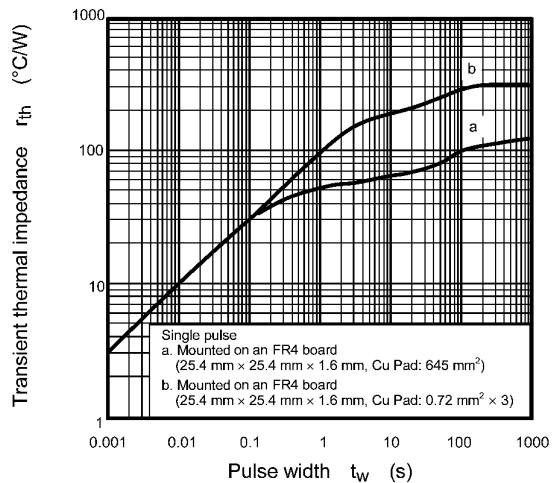
**Fig. 8.9**  $C - V_{DS}$



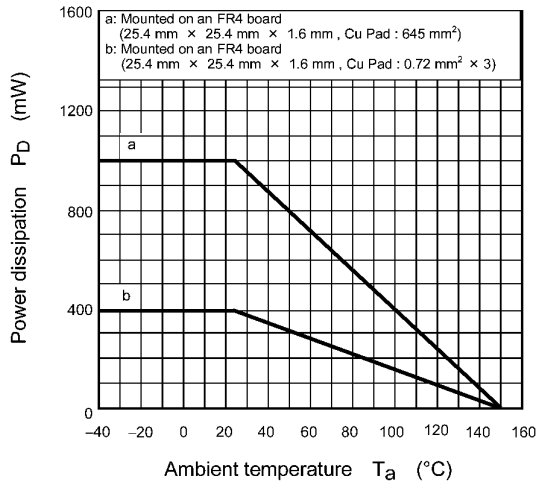
**Fig. 8.10**  $t - I_D$



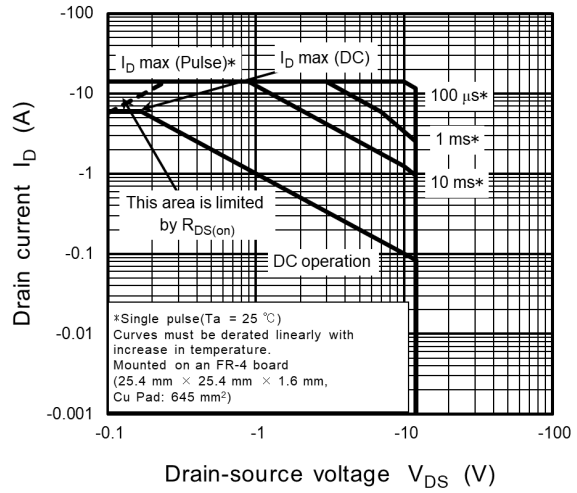
**Fig. 8.11** Dynamic Input Characteristics



**Fig. 8.12**  $r_{th} - t_w$



**Fig. 8.13  $P_D - T_a$**



**Fig. 8.14 Safe Operating Area**

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.



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