

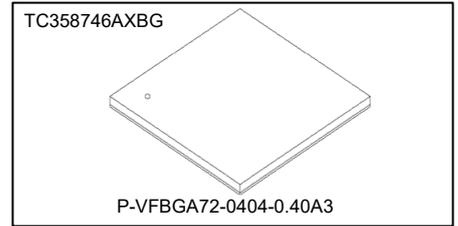
CMOS Digital Integrated Circuit Silicon Monolithic

TC358746AXBG/TC358748XBG

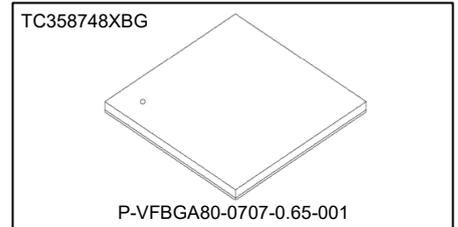
Mobile Peripheral Devices

Overview

The MIPI® CSI-2 to Parallel port and Parallel port to CSI-2 (TC358746AXBG/TC358748XBG) is a bridge device that converts MIPI data transfers from devices such as a camera to an application processor over a Parallel port interface. All internal registers can be access through I²C or SPI (in CSI out case only).



Weight: 32 mg (typ.)



Weight: 68 mg (typ.)

Features

- CSI-2 TX/RX Interface
 - ✧ MIPI CSI-2 compliant
 - ✧ Configurable to CSI-2 TX or CSI-2 RX
 - ✧ Supports up to 1Gbps per data lane
 - ✧ Supports up to 4 data lanes
 - ✧ Supports video data formats
 - RX: RAW8/10/12/14, YUV422 (CCIR/ITU 8/10-bit), RGB888/666/565 and User-Defined 8-bit
 - TX: YUV422 (CCIR/ITU 8/10-bit), YUV444, RGB888/666/565 and RAW8/10/12/14
- Parallel Port Interface
 - ✧ Supports data formats
 - 24-bit bus – un-packed format (Both Input and Output mode)
 - RGB888/666/565, RAW8/10/12/14 and YUV422 8-bit (on 8/16-bit data bus) and 10-bit data formats.
 - YUV444 (Parallel Input mode only)
 - YUV422 8-bit – ITU BT.656 and ITU BT.601 (Parallel input mode only)
 - Up to 100 MHz PCLK frequency for Output mode, and 166 MHz for Input mode.
- I²C Target Interface (CS = L)
 - ✧ Support for normal (100 kHz), fast mode (400 kHz) and special mode (1 MHz)
 - ✧ Configure all TC358746AXBG/TC358748XBG internal registers
- SPI Target Interface (Only applicable in CSIOut configuration, MSEL = H, and CS = H)
 - ✧ SPI interface support for up to 25 MHz operation.
 - ✧ Configure all TC358746AXBG/TC358748XBG internal registers
- GPIO signals
 - ✧ 3 GPIO signals
 - Three GPIO signals can be configured as control signals (MCLK, CXRST, XShutdown) for CSI-2 RX device.
 - Or one GPIO signal can be configured as INT signal for Parallel interface.
- System
 - ✧ Clock and power management support to achieve low power states.
- Power supply inputs
 - ✧ Core and MIPI D-PHY: 1.2 V
 - ✧ I/O: 1.8 V – 3.3 V
- Power Consumption during typical operations
 - ✧ Parallel Input to CSI-2 output, 1080P, 60fps, CSI-2 Clock = 500MHz : 79 mW
 - ✧ CSI-2 Input to Parallel output, PCLK = 100MHz, CSI-2 Clock = 500MHz : 93 mW

Table of content

REFERENCES	5
1. Overview	6
2. Features	8
3. External Pins	9
3.1. TC358746AXBG pinout description	9
3.2. TC358746AXBG BGA72 pin Count Summary	10
3.3. TC358748XBG BGA80 Pin Count Summary	10
3.4. TC358746AXBG Pin Layout.....	11
3.5. TC358748XBG Pin Layout	12
4. Package	13
4.1. TC358746AXBG Package.....	13
4.2. TC358748XBG Package	14
5. Electrical Characteristics.....	15
5.1. Absolute Maximum Ratings.....	15
5.2. Operating Condition.....	15
5.3. DC Electrical Specification	16
6. Revision History	17
RESTRICTIONS ON PRODUCT USE.....	18

Table of Figures

Figure 1.1 System Overview with TC358746AXBG/TC358748XBG in CSI-2 RX to Parallel Port Configuration	6
Figure 1.2 System Overview with TC358746AXBG/TC358748XBG in Parallel Port to CSI-2 TX Configuration	7
Figure 3.1 TC358746AXBG BGA72-Pin Layout (Top View)	11
Figure 3.2 TC358748XBG 80-Pin Layout (Top View).....	12
Figure 4.1 TC358746AXBG P-VFBGA72-0404-0.40A3 package	13
Figure 4.2 TC358748XBG P-VFBGA80-0707-0.65-001 package.....	14

List of Tables

Table 3.1 TC358746AXBG/ TC358748XBG Functional Signal List.....	9
Table 3.2 TC358746AXBG BGA 72Pin Count Summary	10
Table 3.3 TC358748XBG BGA 80 Pin Count Summary	10
Table 4.1 TC358746AXBG P-VFBGA72-0404-0.40A3 Mechanical Dimension.....	13
Table 4.2 TC358748XBG P-VFBGA80-0707-0.65-001 Mechanical Dimension	14
Table 6.1 Revision History	17

- MIPI[®] and CSI-2[®] are registered trademarks of MIPI Alliance, Inc.

1 NOTICE OF DISCLAIMER

2 The material contained herein is not a license, either expressly or impliedly, to any IPR owned or controlled
3 by any of the authors or developers of this material or MIPI. The material contained herein is provided on
4 an "AS IS" basis and to the maximum extent permitted by applicable law, this material is provided AS IS
5 AND WITH ALL FAULTS, and the authors and developers of this material and MIPI hereby disclaim all
6 other warranties and conditions, either express, implied or statutory, including, but not limited to, any (if
7 any) implied warranties, duties or conditions of merchantability, of fitness for a particular purpose, of
8 accuracy or completeness of responses, of results, of workmanlike effort, of lack of viruses, and of lack of
9 negligence.

10 All materials contained herein are protected by copyright laws, and may not be reproduced, republished,
11 distributed, transmitted, displayed, broadcast or otherwise exploited in any manner without the express
12 prior written permission of MIPI Alliance. MIPI, MIPI Alliance and the dotted rainbow arch and all related
13 trademarks, tradenames, and other intellectual property are the exclusive property of MIPI Alliance and
14 cannot be used without its express prior written permission.

15 ALSO, THERE IS NO WARRANTY OF CONDITION OF TITLE, QUIET ENJOYMENT, QUIET
16 POSSESSION, CORRESPONDENCE TO DESCRIPTION OR NON-INFRINGEMENT WITH REGARD
17 TO THIS MATERIAL OR THE CONTENTS OF THIS DOCUMENT. IN NO EVENT WILL ANY
18 AUTHOR OR DEVELOPER OF THIS MATERIAL OR THE CONTENTS OF THIS DOCUMENT OR
19 MIPI BE LIABLE TO ANY OTHER PARTY FOR THE COST OF PROCURING SUBSTITUTE
20 GOODS OR SERVICES, LOST PROFITS, LOSS OF USE, LOSS OF DATA, OR ANY INCIDENTAL,
21 CONSEQUENTIAL, DIRECT, INDIRECT, OR SPECIAL DAMAGES WHETHER UNDER
22 CONTRACT, TORT, WARRANTY, OR OTHERWISE, ARISING IN ANY WAY OUT OF THIS OR
23 ANY OTHER AGREEMENT, SPECIFICATION OR DOCUMENT RELATING TO THIS MATERIAL,
24 WHETHER OR NOT SUCH PARTY HAD ADVANCE NOTICE OF THE POSSIBILITY OF SUCH
25 DAMAGES.

26 Without limiting the generality of this Disclaimer stated above, the user of the contents of this Document is
27 further notified that MIPI: (a) does not evaluate, test or verify the accuracy, soundness or credibility of the
28 contents of this Document; (b) does not monitor or enforce compliance with the contents of this Document;
29 and (c) does not certify, test, or in any manner investigate products or services or any claims of compliance
30 with the contents of this Document. The use or implementation of the contents of this Document may
31 involve or require the use of intellectual property rights ("IPR") including (but not limited to) patents,
32 patent applications, or copyrights owned by one or more parties, whether or not Members of MIPI. MIPI
33 does not make any search or investigation for IPR, nor does MIPI require or request the disclosure of any
34 IPR or claims of IPR as respects the contents of this Document or otherwise.

35 Questions pertaining to this document, or the terms or conditions of its provision, should be addressed to:

36 MIPI Alliance, Inc.
37 c/o IEEE-ISTO
38 445 Hoes Lane
39 Piscataway, NJ 08854
40 Attn: Board Secretary

REFERENCES

1. MIPI D-PHY, “MIPI_D-PHY_specification_v01-00-00, May 14, 2009”
2. MIPI CSI-2, “MIPI Alliance Standard for Camera Serial Interface 2 (CSI-2) Version 1.01 Revision Nov 2010”
3. I²C bus specification, version 2.1, January 2000, Philips Semiconductor

1. Overview

The MIPI CSI-2 to Parallel port and Parallel port to CSI-2 (TC358746AXBG/TC358748XBG) is a bridge device that converts MIPI data transfers from devices such as a camera to an application processor over a Parallel port interface. All internal registers can be access through I²C or SPI (in CSI out case only).

There are several system configurations where TC358746AXBG/TC358748XBG are typically be used.

- CSI-2 TX with Parallel Input mode for Analog TV, Tele-presence Type, and Specialty/Older Cameras application. In this mode, TC358746AXBG/TC358748XBG (Parallel to CSI-2 converter) is a bridge device that converts parallel data transfers to an application over a MIPI CSI-2 interface. Toshiba Bridge Chip provides a low power bridge solution to efficiently translate parallel transfers to serial transfers.
- CSI-2 RX with Parallel output mode for scanner application. In this mode, TC358746AXBG/TC358748XBG (CSI-2 to Parallel converter) is a bridge device that converts serial data transfers from devices such as a camera to an application processor over a parallel interface. Toshiba Bridge Chip provides a low power bridge solution to efficiently translate serial transfers to parallel transfers.

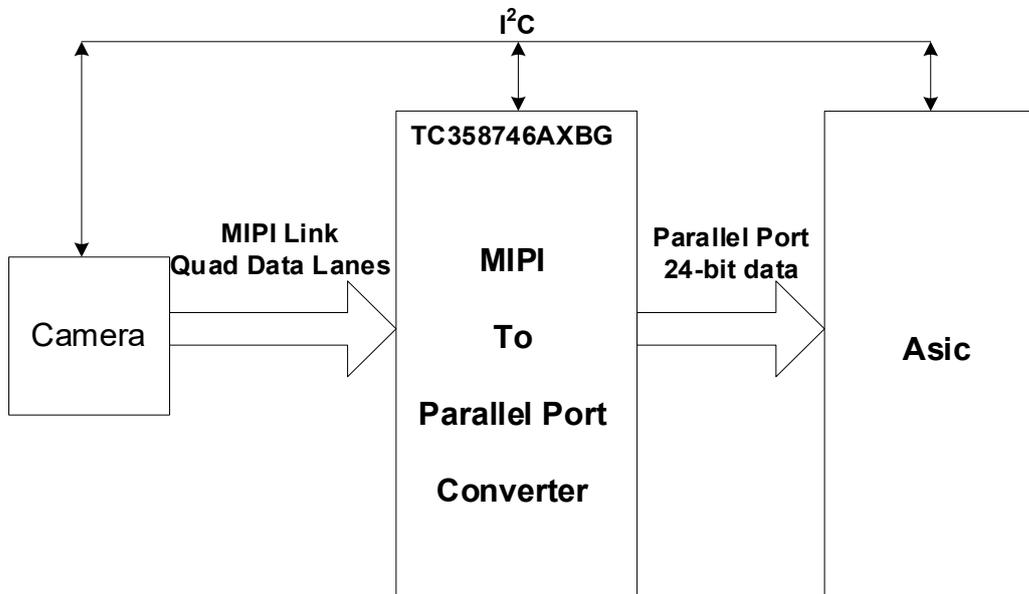


Figure 1.1 System Overview with TC358746AXBG/TC358748XBG in CSI-2 RX to Parallel Port Configuration

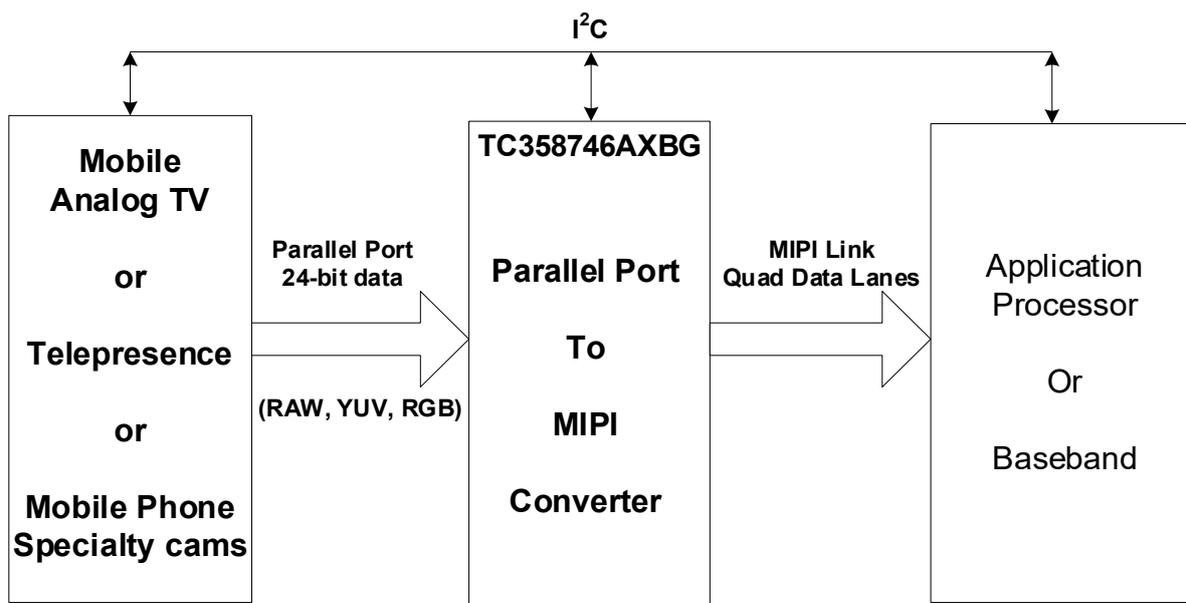


Figure 1.2 System Overview with TC358746AXBG/TC358748XBG in Parallel Port to CSI-2 TX Configuration

2. Features

Below are the main features supported by TC358746AXBG/TC358748XBG.

- CSI-2 TX/RX Interface
 - ✧ MIPI CSI-2 compliant
 - ✧ Configurable to TX or RX controller
 - ✧ Supports up to 1Gbps per data lane
 - ✧ Supports up to 4 data lanes
 - ✧ Supports video data formats
 - RX: RAW8/10/12/14, YUV422 (CCIR/ITU 8/10-bit), RGB888/666/565 and User-Defined 8-bit
 - TX: YUV422 (CCIR/ITU 8/10-bit), YUV444, RGB888/666/565 and RAW8/10/12/14
- Parallel Port Interface
 - ✧ Supports data formats
 - 24-bit bus – un-packed format (Both Input and Output mode)
 - RGB888/666/565, RAW8/10/12/14 and YUV422 8-bit (on 8/16-bit data bus) and 10-bit data formats.
 - YUV444 (Parallel Input mode only)
 - YUV422 8-bit – ITU BT.656 and ITU BT.601 (Parallel input mode only)
 - ✧ Up to 100 MHz PCLK frequency for Output mode, and 166 MHz for Input mode.
- I²C Target Interface (CS = L)
 - ✧ Support for normal (100 kHz), fast mode (400 kHz) and special mode (1 MHz)
 - ✧ Configure all TC358746AXBG/TC358748XBG internal registers
- SPI Target Interface (Only applicable in Sciote configuration, MSEL = H, and CS = H)
 - ✧ SPI interface support for up to 25 MHz operation.
 - ✧ Configure all TC358746AXBG/TC358748XBG internal registers
- GPIO signals
 - ✧ 3 GPIO signals
 - Three GPIO signals can be configured as control signals (MCLK, CXRST, XShutdown) for CSI-2 RX device.
 - Or one GPIO signal can be configured as INT signal for Parallel interface.
- System
 - ✧ Clock and power management support to achieve low power states.
- Power supply inputs
 - ✧ Core and MIPI D-PHY: 1.2 V
 - ✧ I/O: 1.8 V – 3.3 V
- Power Consumption during typical operations
 - ✧ Parallel Input to CSI-2 output, 1080P, 60fps, CSI-2 Clock = 500 MHz : 79 mW
 - ✧ CSI-2 Input to Parallel output, PCLK = 100MHz, CSI-2 Clock = 500 MHz : 93 mW

3. External Pins

3.1. TC358746AXBG pinout description

TC358746AXBG/TC358748XBG resides in BGA pin packages. The following table gives the signals of TC358746AXBG/TC358748XBG and their function.

Table 3.1 TC358746AXBG/ TC358748XBG Functional Signal List

Group	Pin Name	I/O		Type	Initial (O)	Function	Note
		MSEL=0	MSEL=1				
System: Reset & Clock (4)	RESX	I	I	Sch	-	System reset input, active low	-
	REFCLK	I	I	N	-	Reference clock input (6 MHz to 40 MHz)	-
	MSEL	I	I	N	-	Mode Select 1'b0: CSI-2 RX in → Parallel_out 1'b1: Parallel_in → CSI-2 TX	-
	CS	I	I	N	-	Chip Select, active low MSEL= 0 (CSI-2 RX in → Parallel_out) - When CS = 0, chip selected Normal operation - When CS = 1, chip not selected Cannot access to internal registers and optionally Parallel output ports can be tri-state when 0x0004[15] is set MSEL= 1 (Parallel_in → CSI-2 TX) - CS = 0, I ² C I/F is selected - CS = 1, SPI I/F is chosen	-
MIPI-CSI (10)	MIPI_CP	I	O	PHY	LP11	MIPI-CSI clock positive	-
	MIPI_CN	I	O	PHY	LP11	MIPI-CSI clock negative	-
	MIPI_D0P	I	O	PHY	LP11	MIPI-CSI Data 0 positive	-
	MIPI_D0N	I	O	PHY	LP11	MIPI-CSI Data 0 negative	-
	MIPI_D1P	I	O	PHY	LP11	MIPI-CSI Data 1 positive	-
	MIPI_D1N	I	O	PHY	LP11	MIPI-CSI Data 1 negative	-
	MIPI_D2P	I	O	PHY	LP11	MIPI-CSI Data 2 positive	-
	MIPI_D2N	I	O	PHY	LP11	MIPI-CSI Data 2 negative	-
	MIPI_D3P	I	O	PHY	LP11	MIPI-CSI Data 3 positive	-
MIPI_D3N	I	O	PHY	LP11	MIPI-CSI Data 3 negative	-	
I ² C I/F (2)	I2C_SCL	I	I	Sch	-	I ² C serial clock or SPI_SCLK	4 mA
	I2C_SDA	I	I	Sch	-	I ² C serial data or SPI_MOSI	4 mA
Parallel Port I/F (27)	PD[23:0]	O	I	N	L	Parallel Port Data - PD[23:12] can configure to be GPIO[15:4]	4 mA
	VVALID	O	I	N	H	Parallel port VVALID signal	4 mA
	HVALID	O	I	N	L	Parallel port HVALID signal	4 mA
	PCLK	O	I	N	L	Parallel Port Clock signal	4 mA
GPIO (3)	GPIO[2:0]	I	I	N	-	GPIO[2:0] signals CSI-2 RX in → Parallel_out - (GPIO[0] option to become MCLK signal) - (GPIO[1] option to become CXRST or INT) - (GPIO[2] option to become XShutdown) Parallel_in → CSI-2 TX - (GPIO[0] option to become MCLK signal) - (GPIO[1] option to become SPI_SS or INT) - (GPIO[2] option to become SPI_MISO)	4 mA
POWER (9)	VDDC (1.2 V)	NA	-	-	-	VDD for Internal Core (2)	-
	VDDIO (1.8 V – 3.3 V)	NA	-	-	-	VDDIO is for IO power supply (3)	-
	VDD_MIPI (1.2 V)	NA	-	-	-	VDD for the MIPI CSI2 (2)	-
Ground (Note 1)	VSS	NA	-	-	-	Ground	-

Note 1: TC358746AXBG = 17, TC358748XBG = 25

3.2. TC358746AXBG BGA72 pin Count Summary

Table 3.2 TC358746AXBG BGA 72Pin Count Summary

Group Name	Pin Count	Notes
SYSTEM	4	-
MIPI-CSI	10	-
I ² C I/F	2	-
GPIO	3	-
Parallel Port I/F	27	-
POWER	9	IO, MIPI and Core Power
GROUND	17	-
TOTAL	72	-

3.3. TC358748XBG BGA80 Pin Count Summary

Table 3.3 TC358748XBG BGA 80 Pin Count Summary

Group Name	Pin Count	Notes
SYSTEM	4	-
MIPI-CSI	10	-
I ² C I/F	2	-
GPIO	3	-
Parallel Port I/F	27	-
POWER	9	IO, MIPI and Core Power
GROUND	25	-
TOTAL	80	-

3.4. TC358746AXBG Pin Layout

A1	A2	A3	A4	A5	A6	A7	A8	A9
VSS	PD17	PD19	PD21	PD23	GPIO2	I2C_SCL	MSEL	VSS
B1	B2	B3	B4	B5	B6	B7	B8	B9
VDDC	PD16	PD18	PD20	PD22	GPIO1	I2C_SDA	RESX	VDDIO
C1	C2	C3	C4	C5	C6	C7	C8	C9
PD15	PD14	VSS	VSS	VSS	VSS	VDD_MIPI	MIPI_D3P	MIPI_D3N
D1	D2	D3	D4	D5	D6	D7	D8	D9
PD13	PD12	VSS				VSS	MIPI_D2P	MIPI_D2N
E1	E2	E3	E4	E5	E6	E7	E8	E9
VSS	VSS	VDDC				VDD_MIPI	MIPI_CP	MIPI_CN
F1	F2	F3	F4	F5	F6	F7	F8	F9
VSS	VSS	VSS				VSS	MIPI_D1P	MIPI_D1N
G1	G2	G3	G4	G5	G6	G7	G8	G9
PD11	PD10	VDDIO	VSS	VSS	VDDIO	VDDIO	MIPI_D0P	MIPI_D0N
H1	H2	H3	H4	H5	H6	H7	H8	H9
VDDC	PD8	PD6	PD4	PD2	PD0	PCLK	HVALID	CS
J1	J2	J3	J4	J5	J6	J7	J8	J9
VSS	PD9	PD7	PD5	PD3	PD1	REFCLK	WVALID	GPIO0

Figure 3.1 TC358746AXBG BGA72-Pin Layout (Top View)

3.5. TC358748XBG Pin Layout

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10
VSS	PD17	PD19	PD21	PD23	GPIO2	VDDC	I2C_SCL	MSEL	VSS
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10
VDDC	PD16	PD18	PD20	PD22	GPIO1	VSS	I2C_SDA	RESX	VDDIO
C1	C2	C3	C4	C5	C6	C7	C8	C9	C10
PD15	PD14							MIPI_D3P	MIPI_D3N
D1	D2	D3	D4	D5	D6	D7	D8	D9	D10
PD13	PD12		VSS	VSS	VSS	VSS		MIPI_D2P	MIPI_D2N
E1	E2	E3	E4	E5	E6	E7	E8	E9	E10
PD11	PD10		VSS	VSS	VSS	VSS		VSS	VDD_MIPI
F1	F2	F3	F4	F5	F6	F7	F8	F9	F10
PD9	PD8		VSS	VSS	VSS	VSS		MIPI_CP	MIPI_CN
G1	G2	G3	G4	G5	G6	G7	G8	G9	G10
PD7	PD6		VSS	VSS	VSS	VSS		MIPI_D1P	MIPI_D1N
H1	H2	H3	H4	H5	H6	H7	H8	H9	H10
VDDIO	VSS							VSS	VDD_MIPI
J1	J2	J3	J4	J5	J6	J7	J8	J9	J10
PD4	PD2	PD0	VSS	VSS	PCLK	HVALID	CS	MIPI_D0P	MIPI_D0N
K1	K2	K3	K4	K5	K6	K7	K8	K9	K10
PD5	PD3	PD1	VDDC	VDDIO	REFCLK	WVALID	GPIO0	VDDIO	VSS

Figure 3.2 TC358748XBG 80-Pin Layout (Top View)

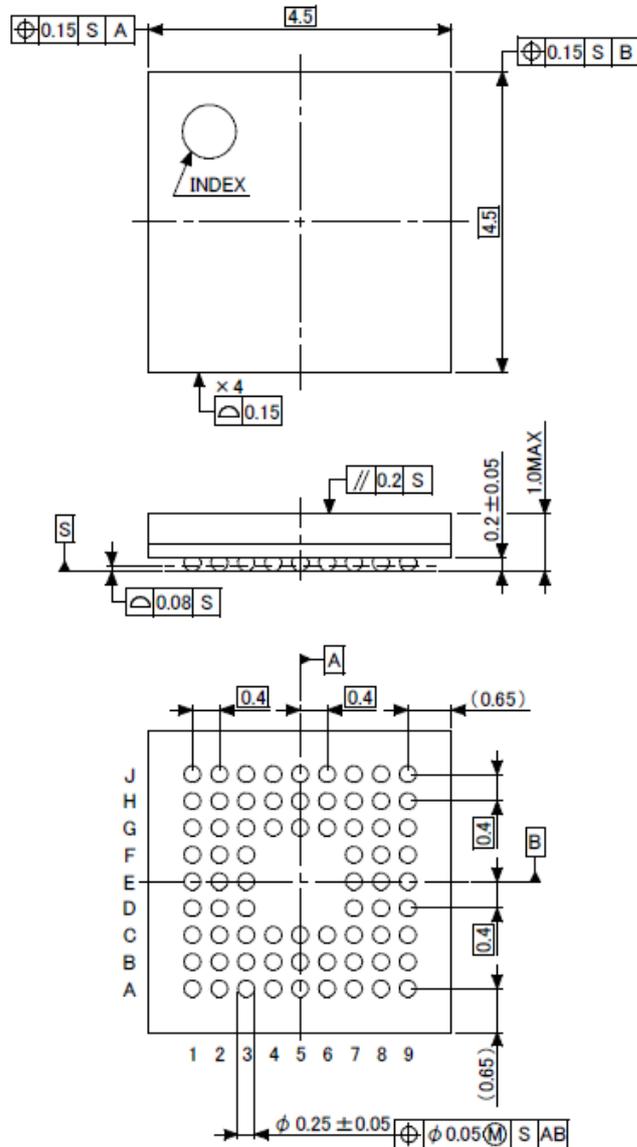
4. Package

4.1. TC358746AXBG Package

The packages for TC358746AXBG are described in the figures below.

P-VFBGA72-0404-0.40A3

(Unit: mm)



Weight: 32 mg (typ.)

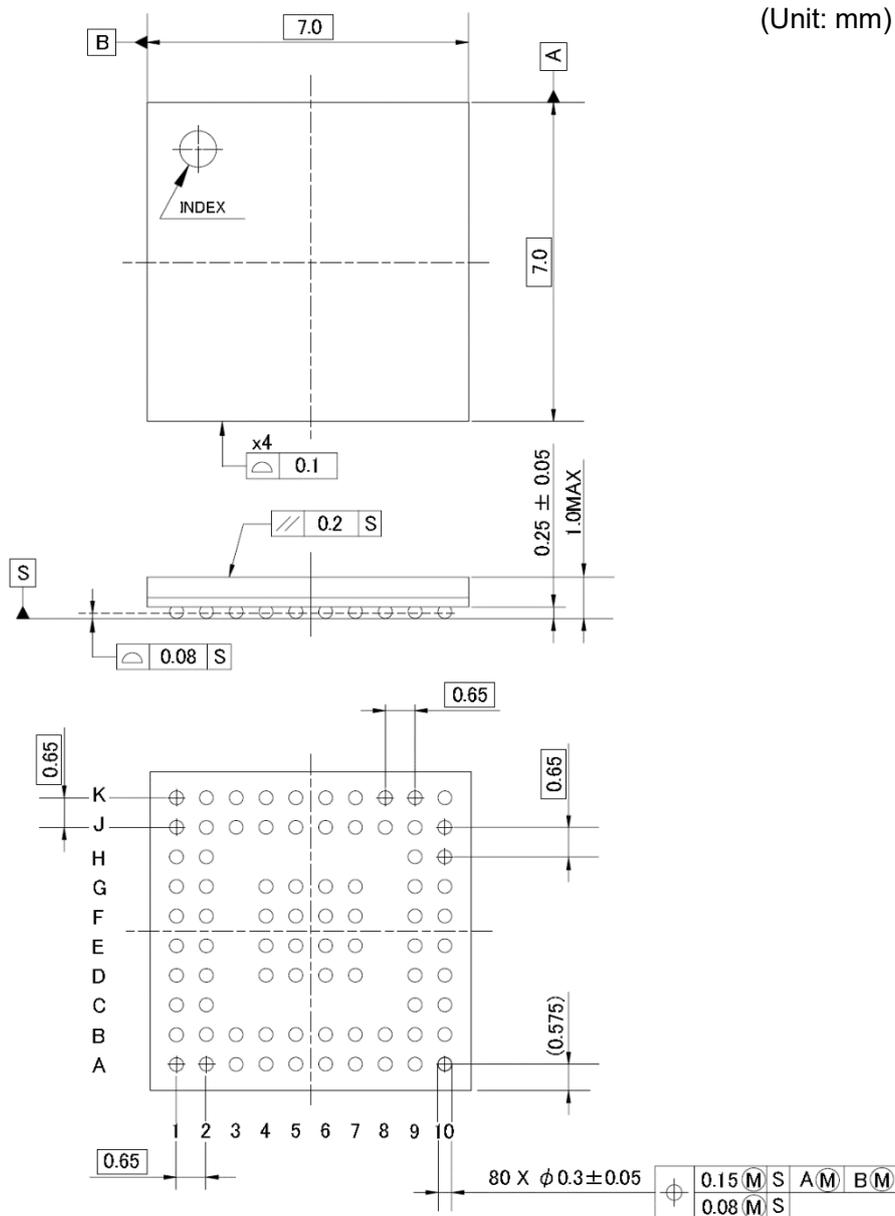
Figure 4.1 TC358746AXBG P-VFBGA72-0404-0.40A3 package

Table 4.1 TC358746AXBG P-VFBGA72-0404-0.40A3 Mechanical Dimension

Dimension	Min	Typ.	Max
Solder ball pitch	-	0.4 mm	-
Solder ball height	0.15 mm	0.2 mm	0.25 mm
Package dimension	-	4.5 x 4.5 mm ²	-
Package height	-	-	1.0 mm

4.2. TC358748XBG Package

The packages for TC358748XBG are described in the figures below.



Weight: 68 mg (typ.)

Figure 4.2 TC358748XBG P-VFBGA80-0707-0.65-001 package

Table 4.2 TC358748XBG P-VFBGA80-0707-0.65-001 Mechanical Dimension

Dimension	Min	Typ.	Max
Solder ball pitch	-	0.65 mm	-
Solder ball height	0.20 mm	0.25 mm	0.30 mm
Package dimension	-	7.0 × 7.0 mm ²	-
Package height	-	-	1.0 mm

5. Electrical Characteristics

5.1. Absolute Maximum Ratings

VSS = 0 V reference

Parameter	Symbol	Rating	Unit
Supply voltage (1.8 V – Digital IO)	VDDIO	-0.3 to +3.9	V
Supply voltage (1.2 V – Digital Core)	VDDC	-0.3 to +1.8	V
Supply voltage (1.2 V – MIPI CSI PHY)	VDD_MIPI	-0.3 to +1.8	V
Input voltage (CSI IO)	V _{IN_CSI}	-0.3 to VDD_MIPI + 0.3	V
Output voltage (CSI IO)	V _{OUT_CSI}	-0.3 to VDD_MIPI + 0.3	V
Input voltage (Digital IO)	V _{IN_IO}	-0.3 to VDDIO + 0.3	V
Output voltage (Digital IO)	V _{OUT_IO}	-0.3 to VDDIO + 0.3	V
Junction temperature	T _j	125	°C
Storage temperature	T _{stg}	-40 to + 125	°C

5.2. Operating Condition

VSS = 0 V reference

Parameter	Symbol	Min	Typ.	Max	Unit
Supply voltage (1.8 V – Digital IO)	VDDIO	1.65	1.8	1.95	V
Supply voltage (3.3 V – Digital IO)	VDDIO	3.0	3.3	3.6	V
Supply voltage (1.2 V – Digital Core)	VDDC	1.1	1.2	1.3	V
Supply voltage (1.2 V – MIPI CSI PHY)	VDD_MIPI	1.1	1.2	1.3	V
Operating temperature (ambient temperature with voltage applied)	T _a	-30	+25	+85	°C
Supply Noise Voltage	V _{SN}	-	-	100	mV

5.3. DC Electrical Specification

Parameter	Symbol	Min	Typ.	Max	Unit
Input voltage, High level input (Note 1)	V_{IH}	0.7 VDDIO	-	VDDIO	V
Input voltage, Low level input (Note 1)	V_{IL}	0	-	0.3 VDDIO	V
Input voltage High level CMOS Schmitt Trigger (Note 1), (Note 2)	V_{IHS}	0.7 VDDIO	-	VDDIO	V
Input voltage Low level CMOS Schmitt Trigger (Note 1), (Note 2)	V_{ILS}	0	-	0.3 VDDIO	V
Output voltage High level (Note 1), (Note 2) (Condition: $I_{OH} = -0.4$ mA)	V_{OH}	0.8 VDDIO	-	VDDIO	V
Output voltage Low level (Note 1), (Note 2) (Condition: $I_{OL} = 2$ mA)	V_{OL}	0	-	0.2 VDDIO	V
Input leak current, High level (Normal IO or Pull-up IO) (Condition: $V_{IN} = +VDDIO$, VDDIO = 3.6 V)	I_{ILH1} (Note 3)	-10	-	10	μ A
Input leak current, High level (Pull-down IO) (Condition: $V_{IN} = +VDDIO$, VDDIO = 3.6 V)	I_{ILH2} (Note 3)	-	-	100	μ A
Input leak current, Low level (Normal IO or Pull-down IO) (Condition: $V_{IN} = 0$ V, VDDIO = 3.6 V)	I_{ILL1} (Note 4)	-10	-	10	μ A
Input leak current, Low level (Pull-up IO) (Condition: $V_{IN} = 0$ V, VDDIO = 3.6 V)	I_{ILL2} (Note 4)	-	-	200	μ A

Note 1: Each power source is operating within recommended operation condition.

Note 2: Current output value is specified to each IO buffer individually. Output voltage changes with output current value.

Note 3: Normal pin or Pull-up IO pin applied VDDIO supply voltage to V_{IN} (input voltage)

Note 4: Normal pin or Pull-down IO pin applied VSSIO (0 V) to V_{IN} (input voltage)

6. Revision History

Table 6.1 Revision History

Revision	Date	Description
0.91	2014-05-29	Newly released
1.11	2015-10-07	1. Remove Fail safe I ² C pad operation 2. Change HSync/VSync to HVALID/VVALID 3. Update table 3-1 for I/O init direction and its output value
1.12	2016-04-01	1. Packages' weight is cut off after the decimal point. 2. TC358746A's package code: P-VFBGA72-0505-0.40-001 → P-VFBGA72-0404-0.40A3 3. Replaced TC358746A's package drawing
1.4	2017-02-07	Corrected condition in 2.1. Typical Power Consumption.
1.5	2017-02-23	Corrected Typo in Table 4.1.
1.6a	2017-10-11	Changed header, footer and the last page. Changed corporate name.
1.85	2020-12-14	Modified Table 3.1 VVALID initial value
1.88	2025-03-14	Updated the terms "Master/Slave" to "Controller/Target" in Features
1.90	2026-03-24	Moved 2.1. Typical Power Consumption to 2. Features Corrected typos

RESTRICTIONS ON PRODUCT USE

Toshiba Corporation and its subsidiaries and affiliates are collectively referred to as "TOSHIBA". Hardware, software and systems described in this document are collectively referred to as "Product".

- TOSHIBA reserves the right to make changes to the information in this document and related Product without notice.
- This document and any information herein may not be reproduced without prior written permission from TOSHIBA. Even with TOSHIBA's written permission, reproduction is permissible only if reproduction is without alteration/omission.
- Though TOSHIBA works continually to improve Product's quality and reliability, Product can malfunction or fail. Customers are responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of Product could cause loss of human life, bodily injury or damage to property, including data loss or corruption. Before customers use the Product, create designs including the Product, or incorporate the Product into their own applications, customers must also refer to and comply with (a) the latest versions of all relevant TOSHIBA information, including without limitation, this document, the specifications, the data sheets and application notes for Product and the precautions and conditions set forth in the "TOSHIBA Semiconductor Reliability Handbook" and (b) the instructions for the application with which the Product will be used with or for. Customers are solely responsible for all aspects of their own product design or applications, including but not limited to (a) determining the appropriateness of the use of this Product in such design or applications; (b) evaluating and determining the applicability of any information contained in this document, or in charts, diagrams, programs, algorithms, sample application circuits, or any other referenced documents; and (c) validating all operating parameters for such designs and applications. **TOSHIBA ASSUMES NO LIABILITY FOR CUSTOMERS' PRODUCT DESIGN OR APPLICATIONS.**
- **PRODUCT IS NEITHER INTENDED NOR WARRANTED FOR USE IN EQUIPMENTS OR SYSTEMS THAT REQUIRE EXTRAORDINARILY HIGH LEVELS OF QUALITY AND/OR RELIABILITY, AND/OR A MALFUNCTION OR FAILURE OF WHICH MAY CAUSE LOSS OF HUMAN LIFE, BODILY INJURY, SERIOUS PROPERTY DAMAGE AND/OR SERIOUS PUBLIC IMPACT ("UNINTENDED USE").** Except for specific applications as expressly stated in this document, Unintended Use includes, without limitation, equipment used in nuclear facilities, equipment used in the aerospace industry, Class 3 medical devices, equipment used for automobiles, and military vehicles and munitions. **IF YOU USE PRODUCT FOR UNINTENDED USE, TOSHIBA ASSUMES NO LIABILITY FOR PRODUCT.** For details, please contact your TOSHIBA sales representative or contact us via our website.
- Do not disassemble, analyze, reverse-engineer, alter, modify, translate or copy Product, whether in whole or in part.
- Product shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable laws or regulations.
- The information contained herein is presented only as guidance for Product use. No responsibility is assumed by TOSHIBA for any infringement of patents or any other intellectual property rights of third parties that may result from the use of Product. No license to any intellectual property right is granted by this document, whether express or implied, by estoppel or otherwise.
- **ABSENT A WRITTEN SIGNED AGREEMENT, EXCEPT AS PROVIDED IN THE RELEVANT TERMS AND CONDITIONS OF SALE FOR PRODUCT, AND TO THE MAXIMUM EXTENT ALLOWABLE BY LAW, TOSHIBA (1) ASSUMES NO LIABILITY WHATSOEVER, INCLUDING WITHOUT LIMITATION, INDIRECT, CONSEQUENTIAL, SPECIAL, OR INCIDENTAL DAMAGES OR LOSS, INCLUDING WITHOUT LIMITATION, LOSS OF PROFITS, LOSS OF OPPORTUNITIES, BUSINESS INTERRUPTION AND LOSS OF DATA, AND (2) DISCLAIMS ANY AND ALL EXPRESS OR IMPLIED WARRANTIES AND CONDITIONS RELATED TO SALE, USE OF PRODUCT, OR INFORMATION, INCLUDING WARRANTIES OR CONDITIONS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ACCURACY OF INFORMATION, OR NONINFRINGEMENT.**
- Do not use or otherwise make available Product or related software or technology for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). Product and related software and technology may be controlled under the applicable export laws and regulations including, without limitation, the Japanese Foreign Exchange and Foreign Trade Law and the U.S. Export Administration Regulations. Export and re-export of Product or related software or technology are strictly prohibited except in compliance with all applicable export laws and regulations.
- Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product. Please use Product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. **TOSHIBA ASSUMES NO LIABILITY FOR DAMAGES OR LOSSES OCCURRING AS A RESULT OF NONCOMPLIANCE WITH APPLICABLE LAWS AND REGULATIONS.**