

CMOS Digital Integrated Circuit Silicon Monolithic

# TC358746AXBG/TC358748XBG/TC9591XBG

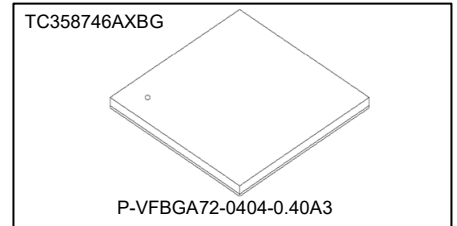
Mobile Peripheral Devices

## Overview

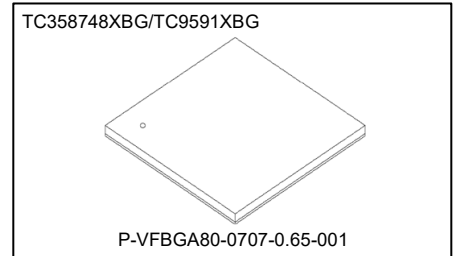
TC358746AXBG/TC358748XBG/TC9591XBG are bridge devices that convert video data from MIPI<sup>®</sup> CSI-2<sup>®</sup> interface to parallel interface, or from parallel interface to MIPI CSI-2 interface. All internal registers can be access through I<sup>2</sup>C or SPI (in CSI out case only).

## Features

- CSI-2 TX/RX Interface
  - + MIPI CSI-2 compliant
  - + Configurable to CSI-2 TX or CSI-2 RX
  - + Supports up to 1Gbps per data lane
  - + Supports up to 4 data lanes
  - + Supports video data formats
    - RX: RAW8/10/12/14, YUV422 (CCIR/ITU 8/10-bit), RGB888/666/565 and User-Defined 8-bit
    - TX: YUV422 (CCIR/ITU 8/10-bit), YUV444, RGB888/666/565 and RAW8/10/12/14
- Parallel Port Interface
  - + Supports data formats
    - 24-bit bus – un-packed format (Both Input and Output mode)
      - RGB888/666/565, RAW8/10/12/14 and YUV422 8-bit (on 8/16-bit data bus) and 10-bit data formats.
      - YUV444 (Parallel Input mode only)
    - YUV422 8-bit – ITU BT.656 and ITU BT.601 (Parallel input mode only)
      - Up to 100 MHz PCLK frequency for Output mode, and 166 MHz for Input mode.
- I<sup>2</sup>C Target Interface (CS = L)
  - + Support for normal (100 kHz), fast mode (400 kHz) and special mode (1 MHz)
  - + Configure all TC358746AXBG/TC358748XBG/TC9591XBG internal registers
- SPI Target Interface (Only applicable in CSIOut configuration, MSEL = H, and CS = H)
  - + SPI interface support for up to 25 MHz operation.
  - + Configure all TC358746AXBG/TC358748XBG/TC9591XBG internal registers
- GPIO signals
  - + 3 GPIO signals
    - Three GPIO signals can be configured as control signals (MCLK, CXRST, XShutdown) for CSI-2 RX device.
    - Or one GPIO signal can be configured as INT signal for Parallel interface.
- System
  - + Clock and power management support to achieve low power states.
- Power supply inputs
  - + Core and MIPI D-PHY<sup>SM</sup>: 1.2 V
  - + I/O: 1.8 V or 3.3 V
- Power Consumption during typical operations
  - + Parallel Input to CSI-2 output, 1080P, 60fps, CSI-2 Clock = 500MHz : 79 mW
  - + CSI-2 Input to Parallel output, PCLK = 100MHz, CSI-2 Clock = 500MHz : 93 mW



Weight: 32 mg (typ.)



Weight: 68 mg (typ.)

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## REFERENCES

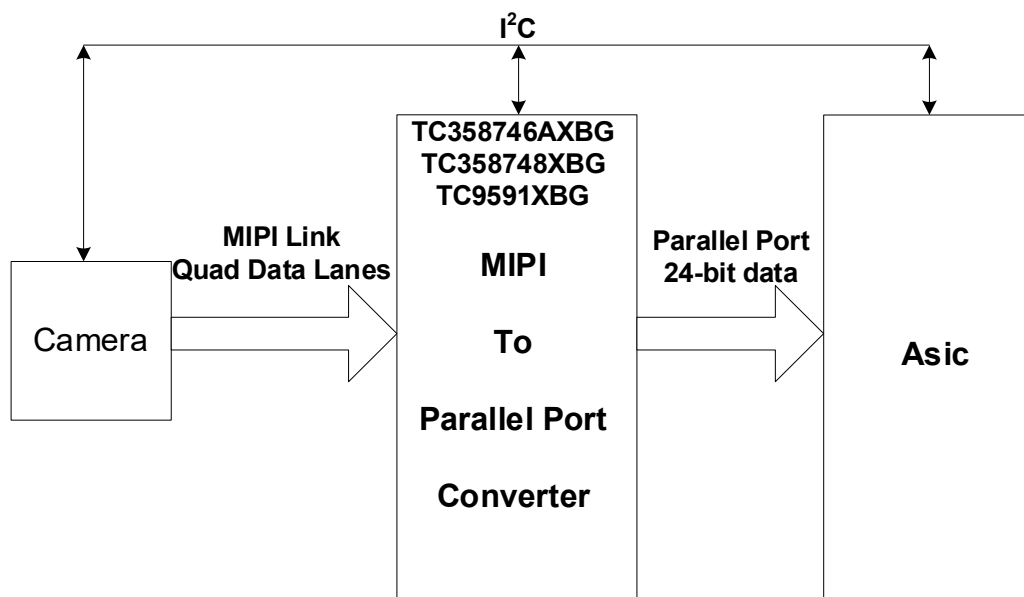
1. MIPI D-PHY, “MIPI\_D-PHY\_specification\_v01-00-00, May 14, 2009”
2. MIPI CSI-2, “MIPI Alliance Standard for Camera Serial Interface 2 (CSI-2) Version 1.01 Revision Nov 2010”
3. I<sup>2</sup>C bus specification, version 2.1, January 2000, Philips Semiconductor

### 1. Overview

TC358746AXBG/TC358748XBG/TC9591XBG are bridge devices that convert video data from MIPI CSI-2 interface to parallel interface, or from parallel interface to MIPI CSI-2 interface. All internal registers can be access through I<sup>2</sup>C or SPI (in CSI out case only).

There are several system configurations where TC358746AXBG/TC358748XBG/TC9591XBG are typically be used.

- CSI-2 TX with Parallel Input mode for Analog TV, Tele-presence Type, and Specialty/Older Cameras application. In this mode, TC358746AXBG/TC358748XBG/TC9591XBG (Parallel to CSI-2 converter) is a bridge device that converts parallel data transfers to an application processor over a MIPI CSI-2 interface. Toshiba Bridge Chip provides a low power bridge solution to efficiently translate parallel transfers to serial transfers.
- CSI-2 RX with Parallel output mode for scanner application. In this mode, TC358746AXBG/TC358748XBG/TC9591XBG (CSI-2 to Parallel converter) is a bridge device that converts serial data transfers from devices such as a camera to an application processor over a parallel interface. Toshiba Bridge Chip provides a low power bridge solution to efficiently translate serial transfers to parallel transfers.



**Figure 1.1 System Overview with TC358746AXBG/TC358748XBG/TC9591XBG in CSI-2 RX to Parallel Port Configuration**

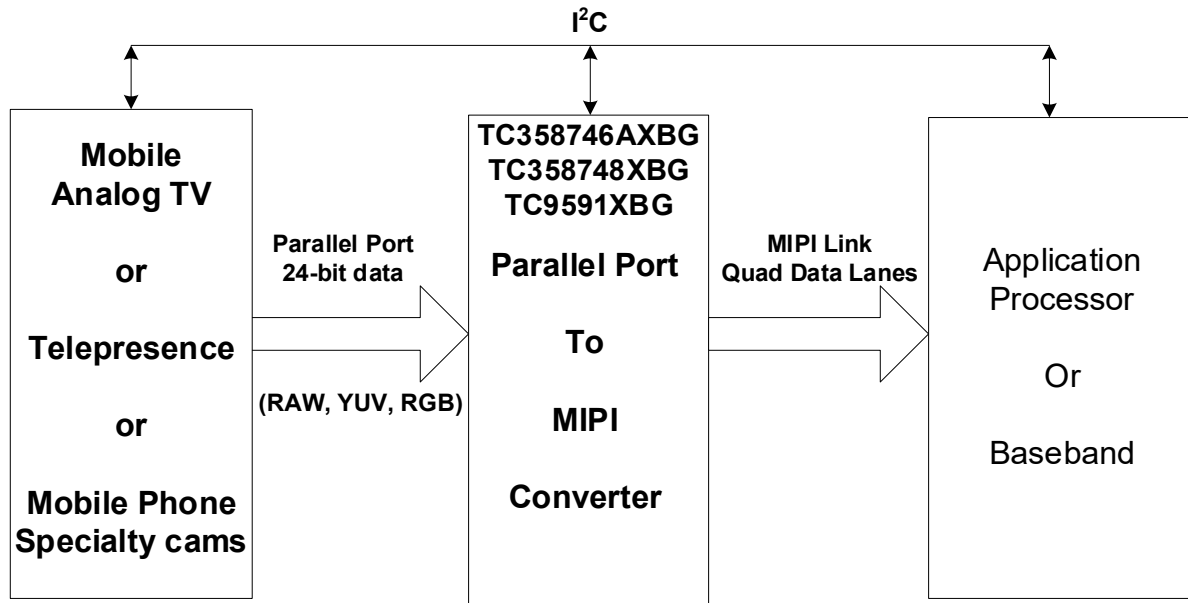


Figure 1.2 System Overview with TC358746AXBG/TC358748XBG/TC9591XBG in Parallel Port to CSI-2 TX Configuration

## 2. Features

Below are the main features supported by TC358746AXBG/TC358748XBG/TC9591XBG.

- CSI-2 TX/RX Interface
  - + MIPI CSI-2 compliant
  - + Configurable to TX or RX controller
  - + Supports up to 1Gbps per data lane
  - + Supports up to 4 data lanes
  - + Supports video data formats
    - RX: RAW8/10/12/14, YUV422 (CCIR/ITU 8/10-bit), RGB888/666/565 and User-Defined 8-bit
    - TX: YUV422 (CCIR/ITU 8/10-bit), YUV444, RGB888/666/565 and RAW8/10/12/14
- Parallel Port Interface
  - + Supports data formats
    - 24-bit bus – un-packed format (Both Input and Output mode)  
RGB888/666/565, RAW8/10/12/14 and YUV422 8-bit (on 8/16-bit data bus) and 10-bit data formats.  
YUV444 (Parallel Input mode only)
    - YUV422 8-bit – ITU BT.656 and ITU BT.601 (Parallel input mode only)
  - + Up to 100 MHz PCLK frequency for Output mode, and 166 MHz for Input mode.
- I<sup>2</sup>C Target Interface (CS = L)
  - + Support for normal (100 kHz), fast mode (400 kHz) and special mode (1 MHz)
  - + Configure all TC358746AXBG/TC358748XBG/TC9591XBG internal registers
- SPI Target Interface (Only applicable in CSI-2 out configuration, MSEL = H, and CS = H)
  - + SPI interface support for up to 25 MHz operation.
  - + Configure all TC358746AXBG/TC358748XBG/TC9591XBG internal registers
- GPIO signals
  - + 3 GPIO signals
    - Three GPIO signals can be configured as control signals (MCLK, CXRST, XShutdown) for CSI-2 TX device.
    - Or one GPIO signal can be configured as INT signal for Parallel interface.
- System
  - + Clock and power management support to achieve low power states.
- Power supply inputs
  - + Core and MIPI D-PHY: 1.2 V
  - + I/O: 1.8 V or 3.3 V
- Power Consumption during typical operations
  - + Parallel Input to CSI-2 output, 1080P, 60fps, CSI-2 Clock = 500 MHz : 79 mW
  - + CSI-2 Input to Parallel output, PCLK = 100MHz, CSI-2 Clock = 500 MHz : 93 mW

### 3. External Pins

#### 3.1. TC358746AXBG/TC358748XBG/TC9591XBG pinout description

TC358746AXBG/TC358748XBG/TC9591XBG resides in BGA pin packages.

The following table gives the signals of TC358746AXBG/TC358748XBG/TC9591XBG and their function.

**Table 3.1 TC358746AXBG/ TC358748XBG/TC9591XBG Functional Signal List**

Group	Pin Name	I/O		Type	Initial (O)	Function	Note
		MSEL=0	MSEL=1				
System: Reset & Clock (4)	RESX	I	I	Sch	-	System reset input, active low	-
	REFCLK	I	I	N	-	Reference clock input (6 MHz to 40 MHz)	-
	MSEL	I	I	N	-	Mode Select 1'b0: CSI-2 RX in → Parallel_out 1'b1: Parallel_in → CSI-2 TX	-
	CS	I	I	N	-	Chip Select, active low MSEL= 0 (CSI-2 RX in → Parallel_out) - When CS = 0, chip selected Normal operation - When CS = 1, chip not selected Cannot access to internal registers and optionally Parallel output ports can be tri-state when 0x0004[15] is set MSEL= 1 (Parallel_in → CSI-2 TX) - CS = 0, I <sup>2</sup> C I/F is selected - CS = 1, SPI I/F is chosen	-
MIPI-CSI (10)	MIPI_CP	I	O	PHY	LP11	MIPI-CSI clock positive	-
	MIPI_CN	I	O	PHY	LP11	MIPI-CSI clock negative	-
	MIPI_D0P	I	O	PHY	LP11	MIPI-CSI Data 0 positive	-
	MIPI_D0N	I	O	PHY	LP11	MIPI-CSI Data 0 negative	-
	MIPI_D1P	I	O	PHY	LP11	MIPI-CSI Data 1 positive	-
	MIPI_D1N	I	O	PHY	LP11	MIPI-CSI Data 1 negative	-
	MIPI_D2P	I	O	PHY	LP11	MIPI-CSI Data 2 positive	-
	MIPI_D2N	I	O	PHY	LP11	MIPI-CSI Data 2 negative	-
	MIPI_D3P	I	O	PHY	LP11	MIPI-CSI Data 3 positive	-
	MIPI_D3N	I	O	PHY	LP11	MIPI-CSI Data 3 negative	-
I <sup>2</sup> C I/F (2)	I2C_SCL	I	I	Sch	-	I <sup>2</sup> C serial clock or SPI_SCLK	4 mA
	I2C_SDA	I	I	Sch	-	I <sup>2</sup> C serial data or SPI_MOSI	4 mA
Parallel Port I/F (27)	PD[23:0]	O	I	N	L	Parallel Port Data - PD[23:12] can configure to be GPIO[15:4]	4 mA
	VVALID	O	I	N	H	Parallel port VVALID signal	4 mA
	HVALID	O	I	N	L	Parallel port HVALID signal	4 mA
	PCLK	O	I	N	L	Parallel Port Clock signal	4 mA
GPIO (3)	GPIO[2:0]	I	I	N	-	GPIO[2:0] signals CSI-2 RX in → Parallel_out - (GPIO[0] option to become MCLK signal) - (GPIO[1] option to become CXRST or INT) - (GPIO[2] option to become XShutdown) Parallel_in → CSI-2 TX - (GPIO[0] option to become MCLK signal) - (GPIO[1] option to become SPI_SS or INT) - (GPIO[2] option to become SPI_MISO)	4 mA
POWER (9)	VDDC (1.2 V)	NA	-	-	-	VDD for Internal Core (2)	-
	VDDIO (1.8 V or 3.3 V)	NA	-	-	-	VDDIO is for IO power supply (3)	-
	VDD_MIPI (1.2 V)	NA	-	-	-	VDD for the MIPI CSI2 (2)	-
Ground (Note 1)	VSS	NA	-	-	-	Ground	-

Note 1: TC358746AXBG = 17 pins, TC358748XBG = 25 pins, TC9591XBG = 25 pins.

## 3.2. TC358746AXBG BGA72 pin Count Summary

**Table 3.2 TC358746AXBG BGA 72Pin Count Summary**

Group Name	Pin Count	Notes
SYSTEM	4	-
MIPI-CSI	10	-
I <sup>2</sup> C I/F	2	-
GPIO	3	-
Parallel Port I/F	27	-
POWER	9	IO, MIPI and Core Power
GROUND	17	-
TOTAL	72	-

## 3.3. TC358748XBG/TC9591XBG BGA80 Pin Count Summary

**Table 3.3 TC358748XBG/TC9591XBG BGA 80 Pin Count Summary**

Group Name	Pin Count	Notes
SYSTEM	4	-
MIPI-CSI	10	-
I <sup>2</sup> C I/F	2	-
GPIO	3	-
Parallel Port I/F	27	-
POWER	9	IO, MIPI and Core Power
GROUND	25	-
TOTAL	80	-

## 3.4. TC358746AXBG Pin Layout

<b>A1</b> VSS	<b>A2</b> PD17	<b>A3</b> PD19	<b>A4</b> PD21	<b>A5</b> PD23	<b>A6</b> GPIO2	<b>A7</b> I2C_SCL	<b>A8</b> MSEL	<b>A9</b> VSS
<b>B1</b> VDDC	<b>B2</b> PD16	<b>B3</b> PD18	<b>B4</b> PD20	<b>B5</b> PD22	<b>B6</b> GPIO1	<b>B7</b> I2C_SDA	<b>B8</b> RESX	<b>B9</b> VDDIO
<b>C1</b> PD15	<b>C2</b> PD14	<b>C3</b> VSS	<b>C4</b> VSS	<b>C5</b> VSS	<b>C6</b> VSS	<b>C7</b> VDD_MIPI	<b>C8</b> MIPI_D3P	<b>C9</b> MIPI_D3N
<b>D1</b> PD13	<b>D2</b> PD12	<b>D3</b> VSS	<b>D4</b>	<b>D5</b>	<b>D6</b>	<b>D7</b> VSS	<b>D8</b> MIPI_D2P	<b>D9</b> MIPI_D2N
<b>E1</b> VSS	<b>E2</b> VSS	<b>E3</b> VDDC	<b>E4</b>	<b>E5</b>	<b>E6</b>	<b>E7</b> VDD_MIPI	<b>E8</b> MIPI_CP	<b>E9</b> MIPI_CN
<b>F1</b> VSS	<b>F2</b> VSS	<b>F3</b> VSS	<b>F4</b>	<b>F5</b>	<b>F6</b>	<b>F7</b> VSS	<b>F8</b> MIPI_D1P	<b>F9</b> MIPI_D1N
<b>G1</b> PD11	<b>G2</b> PD10	<b>G3</b> VDDIO	<b>G4</b> VSS	<b>G5</b> VSS	<b>G6</b> VDDIO	<b>G7</b> VDDIO	<b>G8</b> MIPI_D0P	<b>G9</b> MIPI_D0N
<b>H1</b> VDDC	<b>H2</b> PD8	<b>H3</b> PD6	<b>H4</b> PD4	<b>H5</b> PD2	<b>H6</b> PD0	<b>H7</b> PCLK	<b>H8</b> HVALID	<b>H9</b> CS
<b>J1</b> VSS	<b>J2</b> PD9	<b>J3</b> PD7	<b>J4</b> PD5	<b>J5</b> PD3	<b>J6</b> PD1	<b>J7</b> REFCLK	<b>J8</b> WVALID	<b>J9</b> GPIO0

Figure 3.1 TC358746AXBG BGA72-Pin Layout (Top View)

## 3.5. TC358748XBG/TC9591XBG Pin Layout

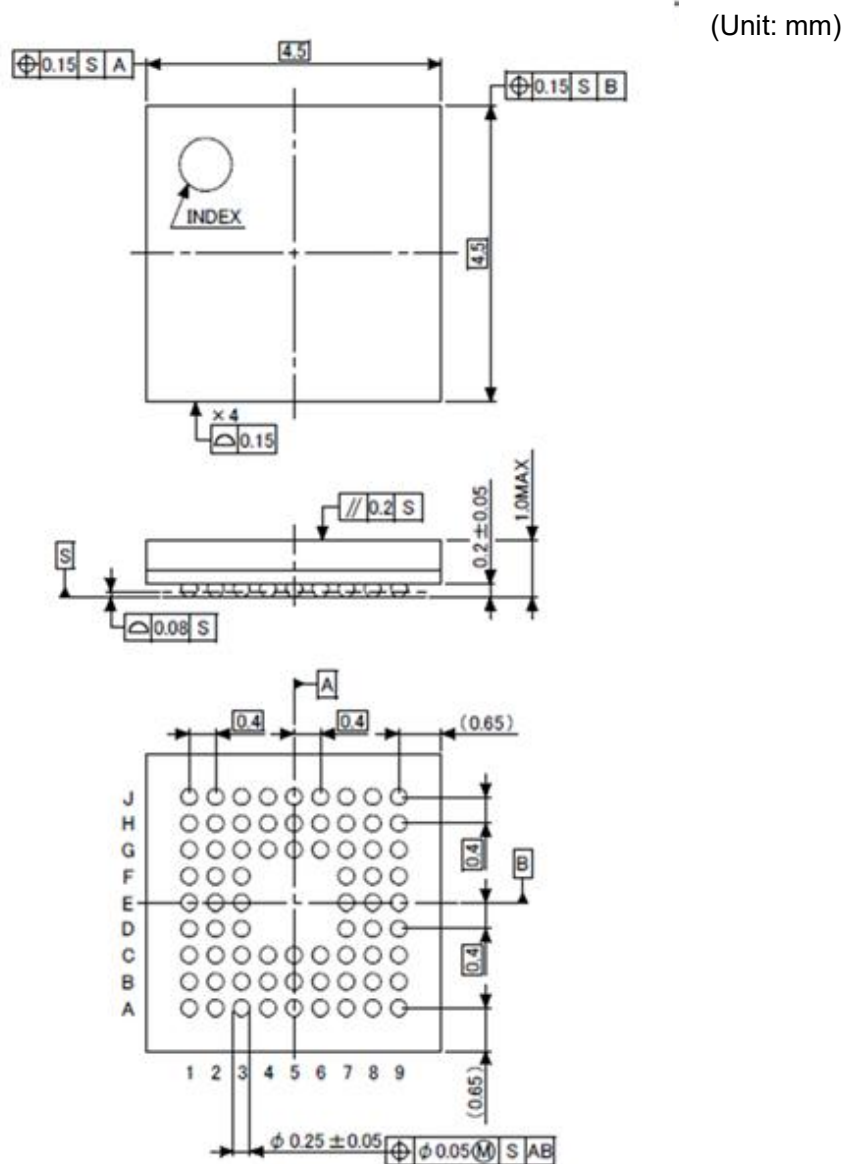
<b>A1</b>	<b>A2</b>	<b>A3</b>	<b>A4</b>	<b>A5</b>	<b>A6</b>	<b>A7</b>	<b>A8</b>	<b>A9</b>	<b>A10</b>
VSS	PD17	PD19	PD21	PD23	GPIO2	VDDC	I2C_SCL	MSEL	VSS
<b>B1</b>	<b>B2</b>	<b>B3</b>	<b>B4</b>	<b>B5</b>	<b>B6</b>	<b>B7</b>	<b>B8</b>	<b>B9</b>	<b>B10</b>
VDDC	PD16	PD18	PD20	PD22	GPIO1	VSS	I2C_SDA	RESX	VDDIO
<b>C1</b>	<b>C2</b>	<b>C3</b>	<b>C4</b>	<b>C5</b>	<b>C6</b>	<b>C7</b>	<b>C8</b>	<b>C9</b>	<b>C10</b>
PD15	PD14							MIPI_D3P	MIPI_D3N
<b>D1</b>	<b>D2</b>	<b>D3</b>	<b>D4</b>	<b>D5</b>	<b>D6</b>	<b>D7</b>	<b>D8</b>	<b>D9</b>	<b>D10</b>
PD13	PD12		VSS	VSS	VSS	VSS		MIPI_D2P	MIPI_D2N
<b>E1</b>	<b>E2</b>	<b>E3</b>	<b>E4</b>	<b>E5</b>	<b>E6</b>	<b>E7</b>	<b>E8</b>	<b>E9</b>	<b>E10</b>
PD11	PD10		VSS	VSS	VSS	VSS		VSS	VDD_MIPI
<b>F1</b>	<b>F2</b>	<b>F3</b>	<b>F4</b>	<b>F5</b>	<b>F6</b>	<b>F7</b>	<b>F8</b>	<b>F9</b>	<b>F10</b>
PD9	PD8		VSS	VSS	VSS	VSS		MIPI_CP	MIPI_CN
<b>G1</b>	<b>G2</b>	<b>G3</b>	<b>G4</b>	<b>G5</b>	<b>G6</b>	<b>G7</b>	<b>G8</b>	<b>G9</b>	<b>G10</b>
PD7	PD6		VSS	VSS	VSS	VSS		MIPI_D1P	MIPI_D1N
<b>H1</b>	<b>H2</b>	<b>H3</b>	<b>H4</b>	<b>H5</b>	<b>H6</b>	<b>H7</b>	<b>H8</b>	<b>H9</b>	<b>H10</b>
VDDIO	VSS							VSS	VDD_MIPI
<b>J1</b>	<b>J2</b>	<b>J3</b>	<b>J4</b>	<b>J5</b>	<b>J6</b>	<b>J7</b>	<b>J8</b>	<b>J9</b>	<b>J10</b>
PD4	PD2	PD0	VSS	VSS	PCLK	HVALID	CS	MIPI_D0P	MIPI_D0N
<b>K1</b>	<b>K2</b>	<b>K3</b>	<b>K4</b>	<b>K5</b>	<b>K6</b>	<b>K7</b>	<b>K8</b>	<b>K9</b>	<b>K10</b>
PD5	PD3	PD1	VDDC	VDDIO	REFCLK	VVALID	GPIO0	VDDIO	VSS

Figure 3.2 TC358748XBG/TC9591XBG 80-Pin Layout (Top View)

### 4. Package

#### 4.1. TC358746AXBG Package

The packages for TC358746AXBG are described in the figures below.



Weight: 32 mg (typ.)

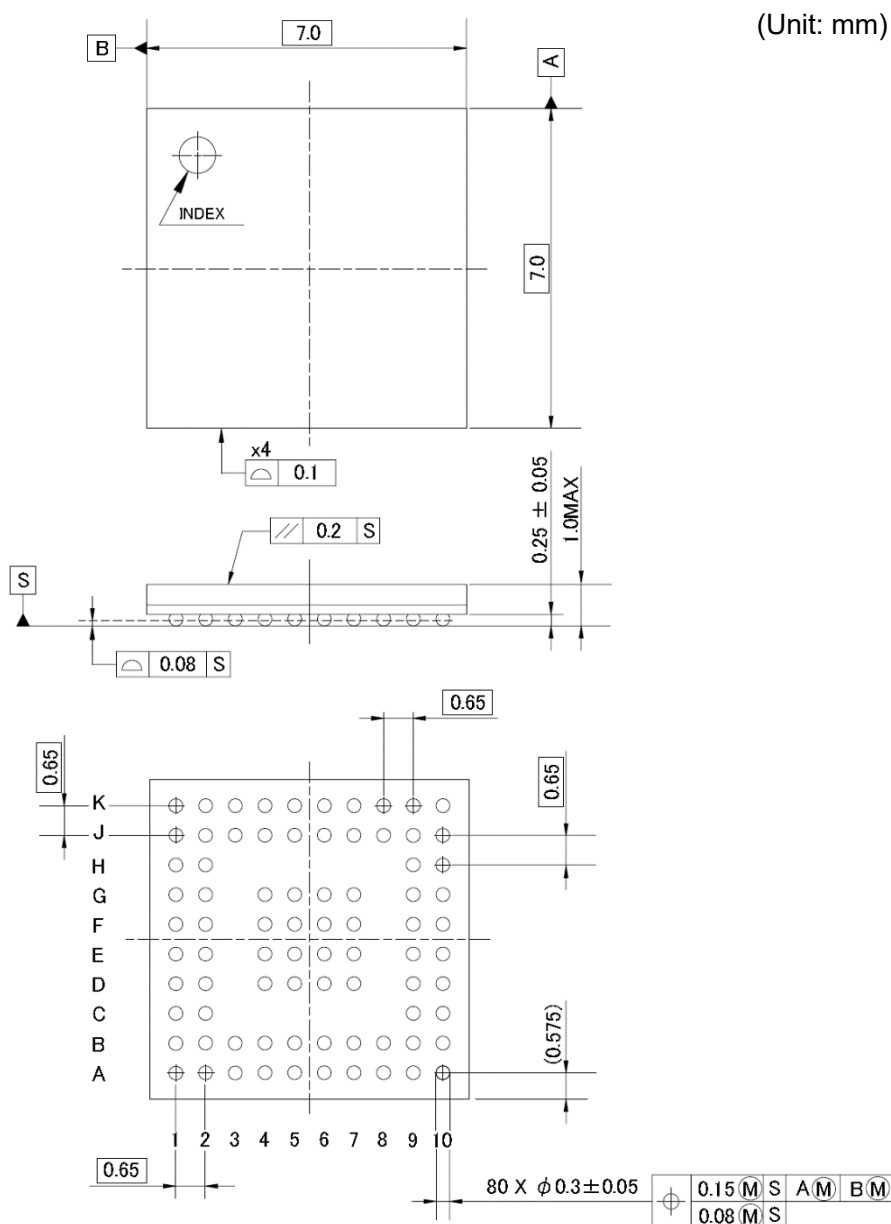
Figure 4.1 TC358746AXBG ( P-VFBGA72-0404-0.40A3 ) package

Table 4.1 TC358746AXBG ( P-VFBGA72-0404-0.40A3 ) Mechanical Dimension

Dimension	Min	Typ.	Max
Solder ball pitch	-	0.4 mm	-
Solder ball height	0.15 mm	0.2 mm	0.25 mm
Package dimension	-	4.5 x 4.5 mm <sup>2</sup>	-
Package height	-	-	1.0 mm

### 4.2. TC358748XBG/TC9591XBG Package

The packages for TC358748XBG/TC9591XBG are described in the figures below.



Weight: 68 mg (typ.)

**Figure 4.2 TC358748XBG/TC9591XBG ( P-VFBGA80-0707-0.65-001 ) package**

**Table 4.2 TC358748XBG/TC9591XBG ( P-VFBGA80-0707-0.65-001 ) Mechanical Dimension**

Dimension	Min	Typ.	Max
Solder ball pitch	-	0.65 mm	-
Solder ball height	0.20 mm	0.25 mm	0.30 mm
Package dimension	-	7.0 × 7.0 mm <sup>2</sup>	-
Package height	-	-	1.0 mm

## 5. Electrical Characteristics

### 5.1. Absolute Maximum Ratings

VSS = 0 V reference

Parameter	Symbol	Rating	Unit
Supply voltage (Digital IO)	VDDIO	-0.3 to +3.9	V
Supply voltage (1.2 V – Digital Core)	VDDC	-0.3 to +1.8	V
Supply voltage (1.2 V – MIPI CSI PHY)	VDD_MIPI	-0.3 to +1.8	V
Input voltage (CSI IO)	V <sub>IN_CSI</sub>	-0.3 to VDD_MIPI + 0.3	V
Output voltage (CSI IO)	V <sub>OUT_CSI</sub>	-0.3 to VDD_MIPI + 0.3	V
Input voltage (Digital IO)	V <sub>IN_IO</sub>	-0.3 to VDDIO + 0.3	V
Output voltage (Digital IO)	V <sub>OUT_IO</sub>	-0.3 to VDDIO + 0.3	V
Storage temperature	T <sub>stg</sub>	-40 to + 125	°C

### 5.2. Operating Condition

VSS = 0 V reference

Parameter	Symbol	Min	Typ.	Max	Unit
Supply voltage (1.8 V – Digital IO)	VDDIO	1.65	1.8	1.95	V
Supply voltage (3.3 V – Digital IO)	VDDIO	3.0	3.3	3.6	V
Supply voltage (1.2 V – Digital Core)	VDDC	1.1	1.2	1.3	V
Supply voltage (1.2 V – MIPI CSI PHY)	VDD_MIPI	1.1	1.2	1.3	V
Operating temperature (ambient temperature with voltage applied) for TC358746AXBG and TC358748AXBG	T <sub>a</sub>	-30	+25	+85	°C
Operating temperature (ambient temperature with voltage applied) for TC9591XBG	T <sub>a</sub>	-40	+25	+105	°C
Supply Noise Voltage (Peak to Peak)	V <sub>SN</sub>	-	-	100	mV

## 5.3. DC Electrical Specification

Parameter	Symbol	Min	Typ.	Max	Unit
Input voltage, High level input (Note 1)	$V_{IH}$	0.7 VDDIO	-	VDDIO	V
Input voltage, Low level input (Note 1)	$V_{IL}$	0	-	0.3 VDDIO	V
Input voltage High level CMOS Schmitt Trigger (Note 1), (Note 2)	$V_{IHS}$	0.7 VDDIO	-	VDDIO	V
Input voltage Low level CMOS Schmitt Trigger (Note 1), (Note 2)	$V_{ILS}$	0	-	0.3 VDDIO	V
Output voltage High level (Note 1), (Note 2) (Condition: $I_{OH} = -0.4$ mA)	$V_{OH}$	0.8 VDDIO	-	VDDIO	V
Output voltage Low level (Note 1), (Note 2) (Condition: $I_{OL} = 2$ mA)	$V_{OL}$	0	-	0.2 VDDIO	V
Input leak current, High level (Normal IO or Pull-up IO) (Condition: $V_{IN} = +VDDIO$ , $VDDIO = 3.6$ V)	$I_{ILH1}$ (Note 3)	-10	-	10	$\mu$ A
Input leak current, High level (Pull-down IO) (Condition: $V_{IN} = +VDDIO$ , $VDDIO = 3.6$ V)	$I_{ILH2}$ (Note 3)	-	-	100	$\mu$ A
Input leak current, Low level (Normal IO or Pull-down IO) (Condition: $V_{IN} = 0$ V, $VDDIO = 3.6$ V)	$I_{ILL1}$ (Note 4)	-10	-	10	$\mu$ A
Input leak current, Low level (Pull-up IO) (Condition: $V_{IN} = 0$ V, $VDDIO = 3.6$ V)	$I_{ILL2}$ (Note 4)	-	-	200	$\mu$ A

Note 1: Each power source is operating within recommended operation condition.

Note 2: Current output value is specified to each IO buffer individually. Output voltage changes with output current value.

Note 3: Normal pin or Pull-up IO pin applied VDDIO supply voltage to  $V_{IN}$  (input voltage)

Note 4: Normal pin or Pull-down IO pin applied VSSIO (0 V) to  $V_{IN}$  (input voltage)

## 6. Revision History

**Table 6.1 Revision History**

Revision	Date	Description
0.91	2014-05-29	Newly released
1.11	2015-10-07	1. Remove Fail safe I <sup>2</sup> C pad operation 2. Change HSync/VSync to HVALID/VVALID 3. Update table 3-1 for I/O init direction and its output value
1.12	2016-04-01	1. Packages' weight is cut off after the decimal point. 2. TC358746A's package code: P-VFBGA72-0505-0.40-001 → P-VFBGA72-0404-0.40A3 3. Replaced TC358746A's package drawing
1.4	2017-02-07	Corrected condition in 2.1. Typical Power Consumption.
1.5	2017-02-23	Corrected Typo in Table 4.1.
1.6a	2017-10-11	Changed header, footer and the last page. Changed corporate name.
1.85	2020-12-14	Modified Table 3.1 VVALID initial value
1.88	2025-03-14	Updated the terms "Master/Slave" to "Controller/Target" in Features
1.90	2026-03-24	Moved 2.1. Typical Power Consumption to 2. Features Corrected typos
2.00	2026-05-11	Marged with TC9591XBG Corrected typos Revised the last page "RESTRICTIONS ON PRODUCT USE".
2.10	2026-05-12	Corrected types.

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