Overview

This document provides design information for Smart Gate Driver Coupler operation.

This document is for reference only and should not be used as the basis for final device design.
# Contents

Overview ....................................................................................................................... 1  
Contents ........................................................................................................................ 2  
1. Introduction ............................................................................................................... 5  
2. SGD coupler products comparison ................................................................................. 6  
3. Protection features ...................................................................................................... 7  
4. Application design ..................................................................................................... 10  
  4.1. Parameters ......................................................................................................... 10  
  4.2. Blanking time settings and adjustment method ....................................................... 11  
    4.2.1. Blanking time ....................................................................................................... 11  
    4.2.2. Calculating the blanking time ................................................................................. 12  
  4.3. Blanking time vs. switching time ........................................................................... 14  
  4.4. Setting the time using an external blanking circuit (R_B) ............................................ 16  
    4.4.1. Impact of R_B on V_{OUT} waveform ........................................................................ 17  
    4.4.2. Varying C_{BLANK} while keeping R_B constant ......................................................... 18  
    4.4.3. Varying R_B while keeping C_{BLANK} constant ............................................................ 19  
  4.5. Modifying the IGBT short detection threshold voltage ............................................. 20  
  4.6. Gate capacitance, gate resistance and propagation delay ......................................... 21  
  4.7. Gate capacitance, output power voltage and soft turn-off time ............................ 22  
  4.8. Bypass condenser and spare terminals ................................................................... 23  
  4.9. Protecting the DESAT terminal from voltage spikes during IGBT switching ............ 24  
  4.10. Buffer transistor ................................................................................................ 25  
  4.11. LED signal waveform shaping .............................................................................. 26  
  4.12. Pull-up resistance R_F for primary side fault signal .............................................. 27  
  4.13. During a protection operation .............................................................................. 28  
  4.14. Miller capacitance error and response ................................................................. 29  
5. Key design considerations ......................................................................................... 30  
RESTRICTIONS ON PRODUCT USE .................................................................................. 32
List of Figures

Figure 3-1 Overcurrent protection sequence ................................................................. 8
Figure 4-1 Diagram during $C_{\text{BLANK}}$ charging ........................................................... 11
Figure 4-2 Timing chart for LED off $\rightarrow$ on sequence .................................................... 11
Figure 4-3 $t_{\text{BLANK}}$ vs. time .......................................................................................... 12
Figure 4-4 Blanking capacitance vs. blanking time ......................................................... 12
Figure 4-5 Voltage waveforms observed at DESAT terminal ($C_{\text{BLANK}} = 0$, $C_{\text{BLANK}} = 100$ pF) .... 13
Figure 4-6 Switching time .............................................................................................. 14
Figure 4-7 $V_{CE} - Q_g$ curve for power device ............................................................... 14
Figure 4-8 Timing chart for normal operation and fault event (reference) ......................... 15
Figure 4-9 IGBT turn-off waveform ............................................................................... 15
Figure 4-10 IGBT saturation voltage vs. collector current ................................................. 15
Figure 4-11 Suggested external blanking ...................................................................... 16
Figure 4-12 $V_{\text{OUT}}$ waveform with no $R_B$ (top) and $R_B = 30k\Omega$ (bottom) ................. 17
Figure 4-13 Test circuit with $R_B$ .................................................................................. 17
Figure 4-14 Impact of $C_{\text{BLANK}}$ on waveform ($R_B$ constant) ................................ 18
Figure 4-15 Test circuit with $R_B$ constant and $C_{\text{BLANK}}$ varying ................................ 18
Figure 4-16 $t_{\text{BLANK}}$ estimates vs. observed values ....................................................... 18
Figure 4-17 Impact of $R_B$ on waveform ($C_{\text{BLANK}}$ constant) .................................. 19
Figure 4-18 Test circuit with $C_{\text{BLANK}}$ constant and $R_B$ varying ................................. 19
Figure 4-19 $t_{\text{BLANK}}$ estimates vs. observed values ($C_{\text{BLANK}}$ fixed) ......................... 19
Figure 4-20 Modifying the short detection threshold voltage ......................................... 20
Figure 4-21 Typical diode configuration ................................................................. 20
Figure 4-22 $C_g$ and $R_g$ vs. propagation delay for TLP5214A ......................................... 21
Figure 4-23 Definition of $t_{\text{PLH}}/t_{\text{PHL}}$ ..................................................................... 21
Figure 4-24 $t_{\text{PLH}}/t_{\text{PHL}}$ measuring circuit ................................................................. 21
Figure 4-25 $C_g$ and $R_g$ vs. soft turn-off time for TLP5214A .......................................... 22
Figure 4-26 Soft turn-off time (observed) ......................................................................... 22
Figure 4-27 Sample configuration for bypass condensers and unused terminals ............... 23
Figure 4-28 Preventing DESAT false detection .............................................................. 24
Figure 4-29 Sample buffer transistor configuration ......................................................... 25
Figure 4-30 Sample input signal waveform shaping configuration ........................................... 26
Figure 4-31 Circuit diagram for pull-up resistor \( R_F \) in primary side fault ........................................ 27
Figure 4-32 Internal circuit diagram showing fault path ................................................................. 28
Figure 4-33 Miller capacitance malfunction .................................................................................. 29
Figure 4-34 Negative power ........................................................................................................... 29
Figure 4-35 Gate resistance ........................................................................................................... 29
Figure 4-36 Miller clamp circuit .................................................................................................... 29

List of Tables

Table 1-1 General-purpose / SGD coupler comparison ................................................................. 5
Table 2-1 Products comparison ..................................................................................................... 6
Table 3-1 Protection and Fault signal reset procedure timing chart ............................................... 8
Table 4-1 Transistor range ............................................................................................................ 25
Table 4-2 Recommended CMOS logic buffers ............................................................................. 26
Table 4-3 TLP5214A thermal resistance ....................................................................................... 28
1. Introduction

TLP5214A/TLP5214/TLP5212/TLP5222 are smart gate driver (hereinafter SGD) couplers with a VCE(sat) detecting function, miller clamping function, FAULT outputting function in addition to a general-purpose gate driver coupler to protect IGBT from overcurrent generated in the inverter applications, etc.

To accommodate multi-functionality, 16-pin SO16L package is used for these products.

In this document, the functional outline of TLP5214A/TLP5214/TLP5212/TLP5222 will be explained.

<table>
<thead>
<tr>
<th>Table 1-1 General-purpose / SGD coupler comparison</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Model</strong></td>
</tr>
<tr>
<td>TLP5702, TLP5754, etc.</td>
</tr>
<tr>
<td>Package/Internal circuit diagram</td>
</tr>
<tr>
<td>Pin count</td>
</tr>
<tr>
<td>Direct driving of the IGBT gate</td>
</tr>
<tr>
<td>UVLO function</td>
</tr>
<tr>
<td>VCE(sat) detecting function</td>
</tr>
<tr>
<td>Active miller clamp</td>
</tr>
<tr>
<td>FAULT outputting function</td>
</tr>
</tbody>
</table>

TLP5214A/TLP5214/TLP5212/TLP5222 is designed for a wide range of applications, from inverter circuits used in industrial equipment (such as general-purpose inverters and power conditioners in solar power systems) to UPS and residential equipment such as home battery storage systems.
2. SGD coupler products comparison

Table 2-1 illustrates some of the key differences among Toshiba SGD couplers.

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>TLPS214A</th>
<th>TLPS214</th>
<th>TLPS212</th>
<th>TLPS222</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating temperature range</td>
<td>T_{opr}</td>
<td>-40 to 110</td>
<td>-40 to 110</td>
<td>-40 to 110</td>
<td>-40 to 110</td>
<td>℃</td>
</tr>
<tr>
<td>Peak output current (max)</td>
<td>I_{OPH} / I_{OPL}</td>
<td>±4.0</td>
<td>±4.0</td>
<td>±2.5</td>
<td>±2.5</td>
<td>A</td>
</tr>
<tr>
<td>Supply current (max)</td>
<td>I_{CC2}</td>
<td>3.8</td>
<td>3.5</td>
<td>5</td>
<td>5</td>
<td>mA</td>
</tr>
<tr>
<td>Supply voltage</td>
<td>V_{CC2} - V_{EE}</td>
<td>15 to 30</td>
<td>15 to 30</td>
<td>15 to 30</td>
<td>15 to 30</td>
<td>V</td>
</tr>
<tr>
<td>Threshold input current (max)</td>
<td>I_{FLH}</td>
<td>6</td>
<td>6</td>
<td>6</td>
<td>6</td>
<td>mA</td>
</tr>
<tr>
<td>DESAT threshold (typ.)</td>
<td>V_{DESAT}</td>
<td>6.5</td>
<td>6.5</td>
<td>6.6</td>
<td>6.6</td>
<td>V</td>
</tr>
<tr>
<td>Blanking capacitor charging current (typ.)</td>
<td>I_{CHG}</td>
<td>-0.24</td>
<td>-0.24</td>
<td>-0.26</td>
<td>-0.26</td>
<td>mA</td>
</tr>
<tr>
<td>Clamp pin threshold voltage (typ.)</td>
<td>V_{Clamp}</td>
<td>2.5</td>
<td>3.0</td>
<td>2.3</td>
<td>2.3</td>
<td>V</td>
</tr>
<tr>
<td>Propagation delay (max) [Note 1]</td>
<td>t_{PLH} / t_{PHL}</td>
<td>150</td>
<td>150</td>
<td>250</td>
<td>250</td>
<td>ns</td>
</tr>
<tr>
<td>Propagation delay skew [Note 1]</td>
<td>t_{plsk}</td>
<td>±80</td>
<td>±80</td>
<td>±150</td>
<td>±150</td>
<td>ns</td>
</tr>
<tr>
<td>DESAT sense to 90% delay (max) [Note 1]</td>
<td>t_{DESAT(90%)}</td>
<td>500</td>
<td>500</td>
<td>500</td>
<td>500</td>
<td>ns</td>
</tr>
<tr>
<td>DESAT sense to 10% delay (max) [Note 1]</td>
<td>t_{DESAT(10%)}</td>
<td>8.5</td>
<td>5</td>
<td>3</td>
<td>3</td>
<td>μs</td>
</tr>
<tr>
<td>DESAT leading edge blanking time (typ.) [Note 1]</td>
<td>t_{DESAT(LEB)}</td>
<td>1.1</td>
<td>-</td>
<td>1.27</td>
<td>1.4</td>
<td>μs</td>
</tr>
<tr>
<td>DESAT sense to low level fault signal delay (max) [Note 1]</td>
<td>t_{DESAT(FAULT)}</td>
<td>C_g=50F</td>
<td>550</td>
<td>500</td>
<td>500</td>
<td>ns</td>
</tr>
<tr>
<td>DESAT trailing edge time (typ.) [Note 1]</td>
<td>t_{DESAT(LOW)}</td>
<td>200</td>
<td>200</td>
<td>172</td>
<td>167</td>
<td>ns</td>
</tr>
<tr>
<td>DESAT input mute (min to max) [Note 1,2]</td>
<td>t_{DESAT(MUTE)}</td>
<td>7 to -</td>
<td>7 to -</td>
<td>5 to -</td>
<td>15 to 40</td>
<td>μs</td>
</tr>
<tr>
<td>Reset to high level fault signal delay [Note 1]</td>
<td>t_{RESET(FAULT)}</td>
<td>0.2 to 2</td>
<td>0.2 to 2</td>
<td>0.1 to 2.5</td>
<td>-</td>
<td>μs</td>
</tr>
<tr>
<td>Protection features</td>
<td>-</td>
<td>UVLO, V_{CE(sat)} detection, Active miller clamp, Fault output</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Fault status reset [Note 3]</td>
<td>-</td>
<td>LED trigger</td>
<td>Automatic</td>
<td>Automatic</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

Refer to the data sheet of each product for details of each characteristic.

[Note 1] Measurement conditions are as follows.
TLP5214A/TLP5214: C_g=25nF, R_g=10Ω
TLP5212/TLP5222: C_g=10nF, R_g=10Ω

[Note 2] The t_{DESAT(MUTE)} has different definition in TLP5214A/TLP5214/TLP5212 and TLP5222. See Table 3-1 in Chapter 3.

[Note 3] See Chapter 3 for more details.

In addition to the given parameters, the shutdown time for the TLP5214A/TLP5212/TLP5222 is slightly longer due to the DESAT leading edge blanking time, to prevent false detection during power device startup.

The TLP5214 has no DESAT leading edge blanking time. It is designed for rapid switching MOSFET and other devices with instantaneous protection functionality.
3. Protection features

- **UVLO function**
  UVLO (under voltage lock-out) function prevents gate driver couplers' accidental output while the power supply for them (VCC2) shows under the threshold voltage. Gate driver couplers keep their output low-level during the period while the VCC2 have not yet attained the UVLO threshold voltage, which is mainly for when turning on the power supply. Similarly, gate driver couplers' output shuts down to prevent accidental output in the event that the VCC2 drops below the UVLO detection voltage. UVLO resets when the VCC2 rises back up above the UVLO threshold voltage.

- **V_{CE(sat)} detection**
  The \( V_{CE(sat)} \) detection feature monitors the saturation level of the collector – emitter voltage \( V_{CE} \) of the driver element (such as IGBT) from the DESAT terminal, and shuts down operation when overcurrent is detected. Normally, \( V_{CE} \) is below the saturation voltage \( V_{CE(sat)} \) (2 V approx.) when the IGBT is on. In the event of overcurrent causing non-saturation, if \( V_{CE(sat)} \) increases beyond the set threshold a fault is declared and \( V_{OUT} \) gradually shuts down.

- **Active miller clamp**
  The active miller clamp feature acts to minimize the increase in electrical potential associated with miller capacitance between the gate and collector of the IGBT or other component by bypassing gate resistance (or equivalent) and allowing direct connection to \( V_{EE} \).

- **Fault output system**
  This feature is to output a fault signal to notify the primary side (the controller side) of a fault detected by the \( V_{CE(sat)} \) detection feature. Normally, when IGBT is ON, \( V_{CE(sat)} \) is about 2V. In the event of overcurrent, \( V_{CE(sat)} \) increasing causes the DESAT – VE pin-to-pin voltage \( (V_{DESAT}) \) exceeds the threshold of 6.5 V (Typ.), and the following two-stage overcurrent protection sequence, as depicted in Figure 3.1, will be carried out by the SGD couplers.
  ① Soft shutdown of \( V_{OUT} \) (gradual transition to OFF status) to prevent IGBT breakdown due to the overcurrent;
  ② Fault signal transfer to controller.
  While most driver couplers take several microseconds to generate the fault signal to the controller and shut down LED signal/coupler output, the TLP5214A/TLP5214/TLP5212/TLP5222 are able to initiate the \( V_{OUT} \) shutdown in less than 500 ns, and are therefore suitable for rapid-acting safety circuits.
**Fault status reset**

Once the protection operation is triggered, the LED signal is not received by SGD couplers for a preset period. This period is denoted $t_{\text{DESAT(MUTE)}}$. There are two types of resetting methods for Fault signal during protection operation.

1. **LED trigger**: The New LED signal, arising after $t_{\text{DESAT(MUTE)}}$, initiates reset procedure. TLP5214A/TLP5214/TLP5212 are applicable.
2. **Automatic**: Automatically initiates reset procedure after $t_{\text{DESAT(MUTE)}}$. TLP5222 is applicable.

The timing chart of Protection and fault signal reset are shown in Table 3-1

**Table 3-1 Protection and Fault signal reset procedure timing chart**
For the LED trigger reset type, resetting Fault signal is linked with LED signal. Therefore, a command from the controller is required. On the other hand, for the automatic reset type, Fault signal is automatically reset over time, which simplifies the sequencing setting in the controller.
4. Application design

4.1. Parameters

Parameters for SGD coupler applications are given below.

1. Gate resistance
   From the gate drivers point of view, gate resistance should not cause the $I_{OP}$ value of the gate drivers greater than the maximum rating. On the other hand, from the power device (IGBT or MOSFET) point of view, gate resistance should also be taken into consideration since this has a bearing on turn-on and turn-off times.

2. Blanking time
   The product switches on in the presence of power and an input signal, and gate drive current is output from $V_{OUT}$. The DESAT function also operates at this time. For power devices with a longer turn-on time, the DESAT function might detect the collector-emitter voltage level $V_{CE}$ and switch to shutdown mode before $V_{CE}$ finishes to become the saturation voltage $V_{CE(sat)}$. The timing of the voltage detection sequence can be adjusted using a blanking capacitor or peripheral circuit.

3. Short-circuit monitoring
   The DESAT terminal is monitored constantly to detect power device faults such as short circuits. If the voltage exceeds the standard threshold value of 6.5 V, the product is switched to shutdown mode. The DESAT diode can be augmented with a Zener diode or SBD to further reduce the short-circuit threshold voltage for the power device.

4. Primary fault signal pull-up resistance
   The open collector feedback circuit output is connected to a pull-up resistor. Recovery time after a fault is governed by the resistance value of the pull-up resistor, and should be tailored to the system requirements and input power.

5. Preventing malfunction
   After all settings have been entered, it may be necessary to insert additional components to prevent malfunction.
4.2. Blanking time settings and adjustment method

4.2.1. Blanking time

Figure 4-1 shows a typical applied circuit with IGBT drive, while Figure 4-2 shows the timing chart for the switching sequence. When the LED input current $I_F$ switches from off to on, the increase in voltage at the output terminal $V_{OUT}$ causes the external IGBT to turn on. At the same time, the blanking capacitance charging current $I_{CHG}$ is output from the DESAT terminal for the purpose of monitoring the collector-emitter voltage $V_{CE}$ for the external IGBT, and the voltage at the DESAT terminal begins rising. TLP5214A/TLP5212/TLP5222 have a $t_{DESAT(LEB)}$ time designed to prevent malfunction associated with DESAT terminal rise.

When the IGBT switches on normally, the DESAT protection circuit needs to be disabled until $V_{CE}$ reaches $V_{th(IGBT)}$, the short-circuit threshold voltage for the IGBT; otherwise a malfunction will occur. Figure 4-2 illustrates the time from the $I_F$ rise until the DESAT voltage reaches the standard threshold of 6.5 V, known as the blanking time ($t_{BLANK}$). The blanking time depends on the value of the capacitor ($C_{BLANK}$) between the DESAT and $V_E$ terminals.

Normally, $t_{BLANK}$ should be longer than the time $t_{th}$ required for $V_{CE}$ to reach $V_{th(IGBT)}$ but shorter than the IGBT short-circuit tolerance interval $t_{SC}$.

![Figure 4-1 Diagram during $C_{BLANK}$ charging](image1)

![Figure 4-2 Timing chart for LED off → on sequence](image2)
4.2.2. Calculating the blanking time

t_{BLANK} is expressed in terms of \(C_{BLANK}, V_{DESAT}, I_{CHG}\) and \(t_{DESAT(LEB)}\) as follows:

\[
t_{BLANK} = C_{BLANK} \times \frac{V_{DESAT}}{I_{CHG}} + t_{DESAT(LEB)}
\]

for example, set \(V_{DESAT}, I_{CHG}, t_{DESAT(LEB)}\) as standard value for TLP5214A

\[
V_{DESAT} = 6.5 \, V \\
I_{CHG} = 240 \, \mu A \\
t_{DESAT(LEB)} = 1.1 \, \mu s
\]

When \(C_{BLANK}\) is 200 pF, \(t_{BLANK}\) is expressed as follows:

\[
t_{BLANK} = 200 \times 10^{-12} \, F \times 6.5 \, V / (240 \times 10^{-6}) \, A + 1.1 \, \mu s = 6.5 \, \mu s
\]

Figure 4-3 shows the relationship between \(C_{BLANK}\) and \(t_{BLANK}\). As Figure 4-4 shows, a higher \(C_{BLANK}\) value lengthens the delay time until overcurrent protection is enabled by altering the gradient of the voltage rise of the DESAT terminal. Note that in real-world applications, \(t_{BLANK}\) is also influenced by other factors such as the parasitic capacitance of connected diode(s).

The \(C_{BLANK}\) value can be used to adjust the \(t_{BLANK}\) period to prevent malfunction associated with overcurrent. Note that this period is shorter than the power device short circuit tolerance interval.
Reference: Impact of CBLANK on representative waveform

Figure 4-5 shows actual waveform observations at DESAT and VOUT terminals when the TLP5214A LED is on.

It can be seen that the CBLANK value has a direct impact on tBLANK. In real-world situations, we also have to consider the capacitance of connected diodes on the DESAT line as well as stray capacitance in the circuit, so these are incorporated into the design estimates. The example above assumes substrate capacitance of approximately 25 pF. (The capacitance of the probe used for waveform observation is also included.)
4.3. Blanking time vs. switching time

The switching time is the period from when the SGD coupler LED comes on to when the IGBT is turned on (see Figure 4-6). It should be no greater than $t_{\text{BLANK}}$, thus (using TLP5214A as an example):

$$t_{\text{PLH}} \text{ for TLP5214A + IGBT } t_{\text{ON}*} = \text{switching time} < t_{\text{BLANK}}$$

* assuming $t_{\text{TH}} \approx t_{\text{ON}}$

where

$t_{\text{PLH}} = 150 \text{ ns (max)}$ (from TLP5214A data sheet)

$t_{\text{ON}}$ is calculated as follows:

$$t_{\text{ON}} = \frac{Q_g \text{ (for IGBT)}}{I_O \text{ (TLP5214A output current)}}$$

For the purpose of this example we assume $V_{\text{GE}} = 15 \text{ V}$ and $I_O = 1.5 \text{ A}$ for IGBT GT30J341 switching. Based on the $V_{\text{CE}}$ and $V_{\text{GE}} - Q_s$ characteristics on the data sheet we have $Q_g = 130 \text{ nC}$ (see Figure 4-7). Thus:

$$t_{\text{ON}} = \frac{130 \text{ nC}}{1.5 \text{ A}} \approx 87 \text{ ns}$$

So the switching time is given by:

$$t_{\text{ON}} = 150 \text{ ns} + 87 \text{ ns}$$

$$= 237 \text{ ns} < 6.5 \mu\text{s (see page 12)}$$

which can be confirmed that it is under $t_{\text{BLANK}}$.

![Figure 4-6 Switching time](image)

![Figure 4-7 $V_{\text{CE}} - Q_g$ curve for power device](image)
Reference: Timing sheet for fault event ON

Figure 4-8 shows waveforms at each terminal (IF, VO, IO, VCE and DESAT) during normal operation and during a fault event.

After input IF to the SGD couplers, VO output drives the IGBT gate. If the IGBT switches normally, the VCE voltage drops to the IGBT saturation voltage. The DESAT terminal voltage monitoring the VCE terminal likewise drops down to the sum total of the saturation voltage and the DESAT diode VF.

When an alarm short (or equivalent fault) occurs, depending on the nature of the fault, the current IC (denoted by blue line) increases, leading to overcurrent. The increase in IGBT current forces up the IGBT VCE(sat) as shown in Figure 4-10. The DESAT terminal voltage also rises simultaneously. When the DESAT terminal voltage exceeds the threshold value (6.5 V standard), the SGD coupler is deemed to have shorted and protection mode engages. The SGD coupler shuts down VO and IO and also initiates a gradual shutdown to prevent any noise associated with the abrupt change to off status. The SGD coupler responsible for detecting the fault notifies the input side by switching on an internal LED and forwarding the fault status.
4.4. Setting the time using an external blanking circuit (R_B)

If we increase the C_BLANK value to boost noise tolerance during switching, this lengthens the charging time, raising the possibility that the protection feature may not engage during the t_{SC} period. Instead, we can use an external resistor as shown in Figure 4-11 to boost the C_BLANK charging current and ensure that protection remains enabled. The external resistor R_B between the DESAT terminals draws external current I_B from the output V_OUT which supplements I_CHG.

R_B allows greater control over the C_BLANK charging current and therefore greater design flexibility in regards to the blanking time.

![SGD coupler](image)

**Figure 4-11 Suggested external blanking**

The voltage applied to the blanking condenser is expressed as follows:

\[
V_I = V_{OUT} - V_E
\]

\[
= R_B \times i(t) + \int (I_{CHG} + i(t)) dt / C_{BLANK}
\]

\[
i(t) = (V_I/R_B + I_{CHG}) \exp(-t/(C_{BLANK} \times R_B)) - I_{CHG}
\]

\[
V_{DESAT}(t) = V_I - R_B \times i(t)
\]

\[
= V_I - (V_I + R_B \times I_{CHG} )\exp(- t / (C_{BLANK} \times R_B)) + R_B \times I_{CHG}
\]

Thus blanking time is given by:

\[
t_{BLANK} = -C_{BLANK} \times R_B \times \log(1 - V_{DESAT} / (V_I + R_B \times I_{CHG}))
\]

For the TLP5214A/TLP5212/TLP5222, blanking time at DESAT rise is included so we add t_{DESAT(LEB)} to the above.

Given that C_{BLANK} = 300 pF, R_B = 30 kΩ, V_{OUT} = 17 V, V_{EE} = -10 V and V_E ≈ 0 V, and from the TLP5214A data sheet we know that V_{DESAT} = 6.5 V, I_{CHG} = 0.24 mA and t_{DESAT(LEB)} = 1.1 μs, we have:

\[
t = -300 \times 10^{-12} \times 30 \times 10^3 \times \log(1 - 6.5 / (17 + 30 \times 10^3 \times 240 \times 10^{-6})) + 1.1 \times 10^{-6}
\]

\[
= -9000 \times 10^{-9} \times \log (1 - 6.5 / (17 + 7.2)) + 1.1 \times 10^{-6}
\]

\[
= -9 \times 10^{-6} \times \log (0.7314) + 1.1 \times 10^{-6}
\]

\[
= 2.815 \times 10^{-6} + 1.1 \times 10^{-6}
\]

which gives us t_{BLANK} = 3.9 μs.
### 4.4.1. Impact of R_B on V_OUT waveform

Figure 4-12 shows waveform observations for the circuit shown in Figure 4-13, with and without a 30 kΩ R_B resistor, where C_BLANK = 125 pF (external 100 pF + test substrate capacitance of 25 pF), V_CC2 = 17 V and V_EE = -10 V.

![Figure 4-12 V_OUT waveform with no R_B (top) and R_B = 30kΩ (bottom)](image)

`t_BLANK` is 4.5 μs without R_B and 2.2 μs with R_B. Blanking time is shorter due to the current I_B flowing through R_B.

Thus even using a C_blank with high value, we can set up `t_BLANK` within short-circuit tolerance interval `t_SC` by adjusting R_B.

Figure 4-13 Test circuit with R_B

Note: Test substrate capacitance = 25 pF approx. (including SBD and Zener diode)
4.4.2. Varying $C_{BLANK}$ while keeping $R_B$ constant

Figure 4-14 shows the impact of $C_{BLANK}$ when $R_B$ is constant, using three values for $C_{BLANK}$: 100 pF, 330 pF and 680 pF.

Figure 4-14 Impact of $C_{BLANK}$ on waveform ($R_B$ constant)

Figure 4-15 shows the test circuit. Waveforms were observed with $R_B = 30$ kΩ (constant), $V_{CC2} = 17$ V and $V_{EE} = -10$ V, and $C_{BLANK}$ varying in the range 100 – 3,000 pF (substrate capacitance = 25 pF).

Figure 4-15 Test circuit with $R_B$ constant and $C_{BLANK}$ varying

$t_{BLANK}$ is given by the following expression:

$$t_{BLANK} = -C_{BLANK} \times R_B \times \log(1 - V_{DESAT}/(V_I + R_B \times I_{CHG}))$$  (see page 16)

Figure 4-16 plots the calculated $t_{BLANK}$ values against the observed values.

For $C_{BLANK}$ values up to approximately 2,000 pF, the calculated values are consistent with the observations. Note that larger capacitors can be limited by the IGBT short-circuit tolerance interval, so it is important to consider the appropriate capacity for the capacitor.
4.4.3. Varying $R_B$ while keeping $C_{BLANK}$ constant

Figure 4-17 shows the impact of $R_B$ when $C_{BLANK}$ is constant.

![Figure 4-17 Impact of $R_B$ on waveform ($C_{BLANK}$ constant)](image)

Figure 4-17 Impact of $R_B$ on waveform ($C_{BLANK}$ constant)

Figure 4-18 shows the test circuit. Waveforms were observed with external $C_{BLANK} = 330$ pF (excluding substrate capacitance), $V_{CC2} = 17$ V and $V_{EE} = -10$ V, and $R_B$ varying in the range 330 $\Omega$ to 30 k$\Omega$.

![Figure 4-18 Test circuit with $C_{BLANK}$ constant and $R_B$ varying](image)

Note: Test substrate capacitance = 25 pF approx. (including SBD and Zener diode)

Figure 4-18 Test circuit with $C_{BLANK}$ constant and $R_B$ varying

Figure 4-19 plots the observed $t_{BLANK}$ values against the estimates calculated using the expression on page 16.

While a lower resistance value can be used to keep $t_{BLANK}$ short, during $V_{OUT}$ output the higher current flowing to $R_B$ boosts current consumption.

![Figure 4-19 $t_{BLANK}$ estimates vs. observed values ($C_{BLANK}$ fixed)](image)
4.5. Modifying the IGBT short detection threshold voltage

The DESAT terminal monitors the voltage during \( I_F \) input. If the terminal voltage \( V_{\text{DESAT}} \) exceeds the standard threshold of 6.5 V, the DESAT circuit engages and the product goes into protection mode. Note that the real power device \( V_{\text{CE}} \) value monitored through the diode or resistor may differ from the observed IGBT \( V_{\text{CE}} \) value. Figure 4-20 shows how to regulate variation in the short detection threshold voltage when a diode or equivalent is present.

Figure 4-21 shows how we can add multiple DESAT diodes in order to either engage protection at a lower voltage or reduce the short detection threshold voltage \( V_{\text{th(IGBT)}} \) in line with the safe operating range of the IGBT are used. By reducing the voltage through \( V_F \) for multiple devices, we can bring down \( V_{\text{th(IGBT)}} \) and set it as a new \( V_{\text{th(IGBT)}} \) value. This is method ①. The other method ②, using Zener diodes, offers a small degree of the adjustment.

Method ①: New \( V_{\text{th(IGBT)}} = V_{\text{DESAT}} - (n \times V_F + R_{\text{DESAT}} \times I_{\text{CHG}}) \) where \( n \) is the number of diodes

Method ②: New \( V_{\text{th(IGBT)}} = V_{\text{DESAT}} - (V_F + V_Z + R_{\text{DESAT}} \times I_{\text{CHG}}) \) where \( V_Z \) is the Zener voltage

For example, with Method ①, if we use three diodes with \( V_F = 0.4 \text{ V} \) at 240 \( \mu \text{A} \) and \( R_{\text{DESAT}} = 100 \text{ Ω} \), we get: New \( V_{\text{th(IGBT)}} = 6.5 - (3 \times 0.4 \text{ V} + 100 \text{ Ω} \times 240 \text{ μA}) \approx 5.3 \text{ V} \)

In normal operation, forward current flowing to the DESAT diode is used to monitor the IGBT \( V_{\text{CE}} \) voltage. In high-power applications, elements such as reverse recovery current may be generated during switching and these can lead to false detection of DESAT voltage. An FRD with low parasitic capacitance can be used to keep reverse recovery current to a minimum.
4.6. Gate capacitance, gate resistance and propagation delay

Using TLP5214A as an example, figure 4-22 illustrates the relationships between propagation delay $t_{PLH} / t_{PHL}$ and $C_g$ and between $t_{PLH} / t_{PHL}$ and $R_g$. The measuring circuit is shown in Figure 4-23 and the waveform observation point in Figure 4-24. It can be seen that $C_g$ and $R_g$ have negligible impact on the propagation delay.

Figure 4-22 $C_g$ and $R_g$ vs. propagation delay for TLP5214A

Figure 4-24 $t_{PLH} / t_{PHL}$ measuring circuit

Figure 4-23 Definition of $t_{PLH} / t_{PHL}$
4.7. Gate capacitance, output power voltage and soft turn-off time

The soft turn-off time of the protection circuit ($t_{\text{DESAT}(10\%)}$) is governed by gate capacitance $C_g$ and output power voltage $V_{CC2}$. Using TLP5214A as an example, figure 4-25 illustrates how $C_g$ and gate resistance $R_g$ affect soft turn-off time. Unlike normal switching operation, there is a soft shutdown followed by a gradual decline in electric potential, as shown in Figure 4-26. Clearly the soft turn-off time is impacted by both the power supply voltage and the gate capacitance.

![Figure 4-25](image1)

**Figure 4-25** $C_g$ and $R_g$ vs. soft turn-off time for TLP5214A

![Figure 4-26](image2)

**Figure 4-26** Soft turn-off time (observed)
4.8. Bypass capacitor and spare terminals

The SGD coupler is a high-performance IC coupler. This means that malfunctions may occur if power supply noise and spare terminals are not dealt with correctly. Figure 4-27 shows how to employ bypass capacitor and what to do with terminals that are not in use.

① Install 1 µF bypass capacitors between $V_E$ and $V_{CC2}$, and between $V_{CC2}$ and $V_{EE}$, as close as possible to the terminals. If the circuit uses a negative supply, another bypass capacitor is needed between the $V_E$ and $V_{EE}$ terminals.
② Install a 0.1 µF bypass capacitor between the $V_{CC1}$ and $V_S$ terminals, as close as possible to the terminals.
③ The LED terminal (pin 15) is a test pin and should not be connected to anything.
④ If the $V_{CLAMP}$ terminal is unused (i.e. when there is no need for an active miller clamp), short it to the $V_{EE}$ terminal.
⑤ If the DESAT terminal is unused, short it to the $V_E$ terminal and isolate from protection.

![Figure 4-27 Sample configuration for bypass capacitors and unused terminals](image)
4.9. Protecting the DESAT terminal from voltage spikes during IGBT switching

A reverse recovery spike from an external IGBT freewheeling diode can cause the DESAT terminal to fall below the electrical potential of ground, generating forward current and damaging the DESAT terminal. It is important to protect the DESAT terminal by adding a Zener diode or Schottky diode (SBD) between the DESAT and $V_E$ terminals as shown in Figure 4-28. Ensure that the diode has the correct rated value.

The Zener diode ($V_Z = 7$ to $8$ V) protects the DESAT terminal from positive overvoltage while the Schottky diode prevents forward bypass by the parasitic diode at the DESAT terminal. Since adding diodes to prevent false detection will increase the capacitance between the DESAT and $V_E$ terminals, it may be necessary to modify the $C_{BLANK}$ setting.

![Figure 4-28 Preventing DESAT false detection](image-url)
4.10. Buffer transistor

Maximum output current of the TLP5214A/TLP5214 and TLP5212/TLP5222 are 4 A and 2.5 A. In the event of insufficient IGBT gate drive current, a buffer transistor can be added. A capacitor should also be installed between the buffer input terminal and $V_{EE}$ to allow IGBT soft turn-off when protection engages. The capacitance will depend on the type of circuit and the soft turn-off time. For a $t_{\text{DESAT}(10\%)}$ value of 7 $\mu$s, a 25 nF capacitor is recommended. A resistor $R_g$ is also required between the SGD coupler output and NPN/PNP base; the size of the resistor will depend on the maximum rated value of the product. Where the $V_{\text{CLAMP}}$ terminal is not used (typically due to negative supply), connect to the $V_{EE}$ terminal instead.

If the IGBT requires gate drive current greater than the maximum of SGD coupler, consider using a transistor such as TTC3710B or TTA1452B as shown in Table 4-1. If using a DESAT diode, we recommend an FRD with voltage resistance equivalent to the IGBT.

<table>
<thead>
<tr>
<th>Product code</th>
<th>Absolute maximum rating</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>NPN</td>
<td>PNP</td>
<td>$</td>
</tr>
<tr>
<td>TTC3710B</td>
<td>TTA1452B</td>
<td>80 V</td>
</tr>
<tr>
<td>TPCP8902</td>
<td>30 V</td>
<td>2 A</td>
</tr>
</tbody>
</table>

The IGBT gate current and transistor collector current are limited by the gate resistance, as per the expression below. Circuit design should take into consideration the maximum rating for the $V_{OUT}$ terminal and the rated values for the IGBT and the transistor.

$$ \text{gate current} = \frac{(V_{OH} - V_{OL})}{(R_g + rg)} $$

where $rg$ is IGBT internal gate resistance.
4.11. LED signal waveform shaping

Where the control substrate and motor controller substrate are separate and there is considerable distance between the SGD coupler and the CPU, inductance effects from the wiring can affect input signal inclination.

Figure 4-30 shows how a hysteresis buffer inserted before the SGD coupler’s input terminal can be used to shape the waveform of the input signal. Table 4-2 lists recommended CMOS logic buffer products.

![Figure 4-30 Sample input signal waveform shaping configuration](image)

| Product code | Function            | V_{CC(opr)} | |I_{OH}| / |I_{OL}| | tpd      | Package     |
|--------------|---------------------|------------|---------|---------|---------|--------|
| 74VHCV244FT  | Octal Schmitt Bus Buffer | 1.8 to 5.5V | 16 mA   | 3.9 ns (typ.) | TSSOP20B |
4.12. Pull-up resistance $R_F$ for primary side fault signal

The product output is in open collector configuration, and requires pull-up resistance $R_F$ as shown in Figure 4-31 to be used as voltage signal.

- The secondary side LED for the fault signal flows less than 10 mA. In the event of a fault, the sink current at the fault signal output terminal is no less than 5 mA (reference value). Assuming $V_{CC1} = 5$ V, and allowing a 50% margin for aging variation and temperature fluctuation, we get
  
  $$R_F = \frac{5 \text{ V}}{2.5 \text{ mA}} = 2 \text{ k}\Omega$$

  Thus, pull-up resistance should be no less than 2 kΩ.

  Around 10 kΩ is recommended in order to reduce current consumption. Note that FAULT terminal recovery times become longer for a higher $R_F$ value, so this should be taken into consideration.

- During normal operation, the open collector $T_r$ is off so the fault terminal has high impedance. At $V_{CC1} = 5$ V, $R_F$ should not be less than 2 kΩ, even for a long fault signal cable subject to external noise interference. Where terminals for multiple devices are connected together, leading to the possibility of simultaneous fault signals, the supply current should also be taken into consideration.

  Buffers may be used to reduce noise and/or supplement the supply current.

![Figure 4-31 Circuit diagram for pull-up resistor $R_F$ in primary side fault signal](SGD coupler)

**How to calculate**

At $V_{CC1} = 3.3$ V, sink current $I_{OF}$ is independent of $V_{CC1}$

Thus:

$$R_F = \frac{3.3 \text{ V}}{2.5 \text{ mA} \text{ (includes 50% margin)}} = 1.3 \text{ k}\Omega$$

So the minimum pull-up resistance $R_F$ is 1.3 kΩ.
4.13. During a protection operation

When the SGD coupler enters protection mode, the feedback LED (i.e., the fault output LED) lights and the fault outputs to report an IGBT fault. If fault mode persists, the secondary side fault output LED lights and a current of approximately 10 mA flows between the V_{CC2} and V_E terminals, leading to increased power loss on the secondary side. Also, bootstrap circuits with IC power are liable to sudden discharge from the capacitors, so the possibility of voltage drop must be taken into consideration.

As shown in P.8, for LED trigger type (TLP5214A/TLP5214/TLP5212), the LED signal must be switched from OFF to ON to cancel the protection operation. For Automatic reset type (TLP5222), after t_{DESAT(MUTE)}, protection operation will be canceled automatically. If the protection function engages, the system should be stopped and restarted as soon as possible. Figure 4-32 shows the internal block diagram for SGD coupler.

![Internal circuit diagram showing fault path](image)

When V_{CC2} = 30 V and fault mode is engaged with LED current of 10 mA, IC consumption is approximately 28 V (V_{drop}). The loss at IC is given by:

\[ P = V_{\text{drop}} \times I_{\text{LED}} = 28 \text{ V} \times 10 \text{ mA} = 280 \text{ mW} \]

Given the thermal resistance of the product R_{th(j-a)} = 70°C/W (from Table 4-3) we can calculate the temperature as follows:

\[ \Delta T_{j} = 70 \times 0.28 = 19.6°C \]

So using at high temperatures should be avoided.

<table>
<thead>
<tr>
<th>Reference value</th>
<th>TLP5214A</th>
</tr>
</thead>
<tbody>
<tr>
<td>R_{th(j-a)}</td>
<td>70°C/W</td>
</tr>
</tbody>
</table>
4.14. Miller capacitance error and response

Malfunctions associated with miller capacitance $C_{CG}$ between the IGBT collector and gate are typical of the problems that can be caused by inverter switching noise. Figure 4-33 illustrates a miller capacitance malfunction in a typical coupler configuration on the lower arm of the inverter circuit.

When the IGBT for the upper arm of the inverter circuit is on, the electrical potential at the mid-point abruptly increases, while the displacement current $I_S (= C_{CG} \times (dV_{CG} / dt))$ flows via the lower arm IGBT $C_{CG}$ in the photocoupler output direction. As it passes through the circuit gate resister $R_g$ the voltage drops and the gate voltage rises, potentially causing a false ON at the IGBT and shorting out the upper and lower arms.

Three strategies can be employed to prevent a miller capacitance malfunction.

① Use negative power
A negative power supply puts the gate at negative potential with the IGBT is off, preventing malfunction (see Figure 4-34).

② Change the gate resistance
Lower gate resistance combined with diodes in parallel suppresses the gate’s contribution to the voltage increase (see Figure 4-35).

③ Add a miller clamp circuit
The SGD coupler includes an active miller clamp circuit that creates a short-circuit between the IGBT gate and emitter. When photocoupler output switches from high to low and the gate voltage falls below 3 V (approximately), the MOSFET between $V_{CLAMP}$ and $V_{EE}$ switches on and the gate is clamped on the emitter $V_{EE}$, as shown in Figure 4-36.
5. Key design considerations

The SGD coupler is a high-performance IC coupler with a number of built-in features. It should be noted that peripheral components can sometimes cause the SGD coupler to malfunction. The following considerations should also be taken into account at the design stage.

1. Gate resistance $R_g$
   A larger $R_g$ will help to reduce the surge voltage at switching as well as the likelihood of $dv/dt$ striking error, but the higher resistance may also exacerbate losses due to longer switching times for power devices. The gate resistance value should take into account peripheral circuits and power devices.

2. Separation between driver circuit and power device
   Excessive separation between the driver circuit (coupler) and the power device can add noise to and cause oscillation of the gate signal. The potential for a malfunction can be minimized by designing the driver circuit and power device as close together as possible; connecting them with the thickest possible wiring; and using a higher gate resistance value.
   Since the wiring for the DESAT terminal that monitors the power device saturation voltage can affect the blanking time, it should be kept as far as possible from $V_E$ so that it does not create capacitance.

3. Bootstrap circuit diode
   Given that the GND potential of the high side IGBT/MOSFET can vary anywhere between zero and 600 V or higher, depending on the application, power for the driver coupler has to come from a floating power supply or bootstrap circuit. If the bootstrap option is used, a high-speed diode is recommended, one that is designed for the same withstand voltages as the power device (at least 600 V).

4. Gate-emitter resistance $R_{GE}$
   The IGBT can fail if voltage is applied to the collector-emitter when gate-emitter is open. This can be prevented by either adding in up to 10 kΩ of resistance or changing the power supply input order so that the gate is served first.

5. Power device in parallel
   Power devices for high-capacitance inverters are often wired in parallel. In this case it is important that the circuit is designed to provide all devices with the same level of current. This will prevent oscillation, which can occur if current is unbalanced and becomes concentrated in a single device.
## Revision History

<table>
<thead>
<tr>
<th>Revision</th>
<th>Date</th>
<th>Page</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rev. 1.0</td>
<td>2018-3-30</td>
<td>-</td>
<td>1st edition</td>
</tr>
<tr>
<td>Rev. 2.0</td>
<td>2022-4-21</td>
<td>All pages</td>
<td>Postscript for TLP5212/TLP5222 and protection operation reset type</td>
</tr>
</tbody>
</table>
RESTRICTIONS ON PRODUCT USE

Toshiba Corporation and its subsidiaries and affiliates are collectively referred to as “TOSHIBA”. Hardware, software and systems described in this document are collectively referred to as “Product”.

- TOSHIBA reserves the right to make changes to the information in this document and related Product without notice.
- This document and any information herein may not be reproduced without prior written permission from TOSHIBA. Even with TOSHIBA’s written permission, reproduction is permissible only if reproduction is without alteration/omission.
- Though TOSHIBA works continually to improve Product’s quality and reliability, Product can malfunction or fail. Customers are responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of Product could cause loss of human life, bodily injury or damage to property, including data loss or corruption. Before customers use the Product, create designs including the Product, or incorporate the Product into their own applications, customers must also refer to and comply with (a) the latest versions of all relevant TOSHIBA information, including without limitation, this document, the specifications, the data sheets and application notes for Product and the precautions and conditions set forth in the "TOSHIBA Semiconductor Reliability Handbook" and (b) the instructions for the application with which the Product will be used with or for. Customers are solely responsible for all aspects of their own product design or applications, including but not limited to (a) determining the appropriateness of the use of this Product in such design or applications; (b) evaluating and determining the applicability of any information contained in this document, or in charts, diagrams, programs, algorithms, sample application circuits, or any other referenced documents; and (c) validating all operating parameters for such designs and applications. TOSHIBA ASSUMES NO LIABILITY FOR CUSTOMERS’ PRODUCT DESIGN OR APPLICATIONS.

- PRODUCT IS NEITHER INTENDED NOR WARRANTED FOR USE IN EQUIPMENTS OR SYSTEMS THAT REQUIRE EXTRAORDINARILY HIGH LEVELS OF QUALITY AND/OR RELIABILITY, AND/OR A MALFUNCTION OR FAILURE OF WHICH MAY CAUSED LOSS OF HUMAN LIFE, BODILY INJURY, SERIOUS PROPERTY DAMAGE AND/OR SERIOUS PUBLIC IMPACT (“UNINTENDED USE”). Except for specific applications as expressly stated in this document, Unintended Use includes, without limitation, equipment used in nuclear facilities, equipment used in the aerospace industry, lifesaving and/or life supporting medical equipment, equipment used for automobiles, trains, ships and other transportation, traffic signaling equipment, equipment used to control combustions or explosions, safety devices, elevators and escalators, and devices related to power plant. IF YOU USE PRODUCT FOR UNINTENDED USE, TOSHIBA ASSUMES NO LIABILITY FOR PRODUCT. For details, please contact your TOSHIBA sales representative or contact us via our website.

- Do not disassemble, analyze, reverse-engineer, alter, modify, translate or copy Product, whether in whole or in part.
- Product shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable laws or regulations.
- The information contained herein is presented only as guidance for Product use. No responsibility is assumed by TOSHIBA for any infringement of patents or any other intellectual property rights of third parties that may result from the use of Product. No license to any intellectual property right is granted by this document, whether express or implied, by estoppel or otherwise.

- ABSENT A WRITTEN SIGNED AGREEMENT, EXCEPT AS PROVIDED IN THE RELEVANT TERMS AND CONDITIONS OF SALE FOR PRODUCT, AND TO THE MAXIMUM EXTENT ALLOWABLE BY LAW, TOSHIBA (1) ASSUMES NO LIABILITY WHATSOEVER, INCLUDING WITHOUT LIMITATION, INDIRECT, CONSEQUENTIAL, SPECIAL, OR INCIDENTAL DAMAGES OR LOSS, INCLUDING WITHOUT LIMITATION, LOSS OF PROFITS, LOSS OF OPPORTUNITIES, BUSINESS INTERRUPTION AND LOSS OF DATA, AND (2) DISCLAIMS ANY AND ALL EXPRESS OR IMPLIED WARRANTIES AND CONDITIONS RELATED TO SALE, USE OF PRODUCT, OR INFORMATION, INCLUDING WARRANTIES OR CONDITIONS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ACCURACY OF INFORMATION, OR NONINFRINGEMENT.

- Do not use or otherwise make available Product or related software or technology for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). Product and related software and technology may be controlled under the applicable export laws and regulations including, without limitation, the Japanese Foreign Exchange and Foreign Trade Law and the U.S. Export Administration Regulations. Export and re-export of Product or related software or technology are strictly prohibited except in compliance with all applicable export laws and regulations.

- Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product. Please use Product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. TOSHIBA ASSUMES NO LIABILITY FOR DAMAGES OR LOSSES OCCURRING AS A RESULT OF NONCOMPLIANCE WITH APPLICABLE LAWS AND REGULATIONS.