TB67S103A

Usage considerations

Summary

The TB67S103A is a two-phase bipolar stepping motor driver using a PWM chopper. The device is controlled by Serial interface (data bank register type). Fabricated with the BiCD process, rating is 50 V/4.0 A.

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1. Power supply voltage

1.1. Power supply voltage and usage range

In using the TB67S103A, the voltage should be applied to the terminals of VM, VREFA, and VREFB. The maximum rating of VM supply voltage is 50 V. Usage range of the power supply voltage is 10 to 47 V.

The maximum rating of VREF voltage is 5 V. Usage range of the voltage is 0 to 3.6 V.

As for the voltage of VREF, the voltage of the internal regulator of the IC (VCC) can be also used. (However, if the current is pulled up exceeding the capability of the internal regulator, the regulation of VCC may not be kept. When the voltage of VREF is applied by dividing the voltage of VCC, the total of the voltage-dividing resistance should not be less than 10 kΩ.

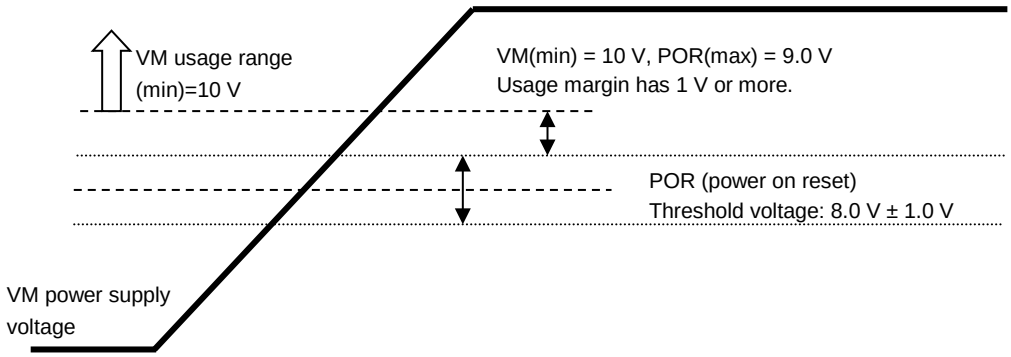


Figure 1.1 Power supply voltage and usage range

1.2. Power supply sequence

There are no special procedures of inputting a power supply and shutdown because the TB67S103A incorporates the power on reset (POR). However, under the unstable state of inputting the power supply (VM) and shutdown, it is recommended to turn off the motor operation. Please operate the motor by switching the input signal after the power supply becomes in the stable state.

2. Output current

Motor usage current should be 3A or less. The maximum current of the actual usage is limited depending on the usage conditions (the ambient temperature, the wiring pattern of the board, the radiation path, and the exciting design). Configure the most appropriate current value after calculating the heat and evaluating the board under the operating environment.

3. Control input

When the logic input signal is inputted under the condition that the voltage of VM is not supplied, the electromotive force by inputting signal is not generated. However, configure the input signal low level before the power supply is applied by referring to the description of the “1.2. Power supply sequence”.

4. PWM control

The TB67S103A can adjust the internal oscillation frequency (fOSCM) and the chopping frequency (fchop) with the constant number of the external parts connecting to OSCM terminal.

- The relation equations of the OSCM oscillation frequency (fOSCM) and the chopping frequency (fchop) are as follows;

  $fOSCM = 1 / [0.56 \times \{C \times (R1 + 500)\}]$

  $fchop = fOSCM / 16$

※ C, R1: external constant number for OSCM (fOSCM is about 1.12 MHz (typ.) at C = 270 pF and R1 = 5.1 kΩ. fchop becomes considerable at about 70 kHz (typ.).)

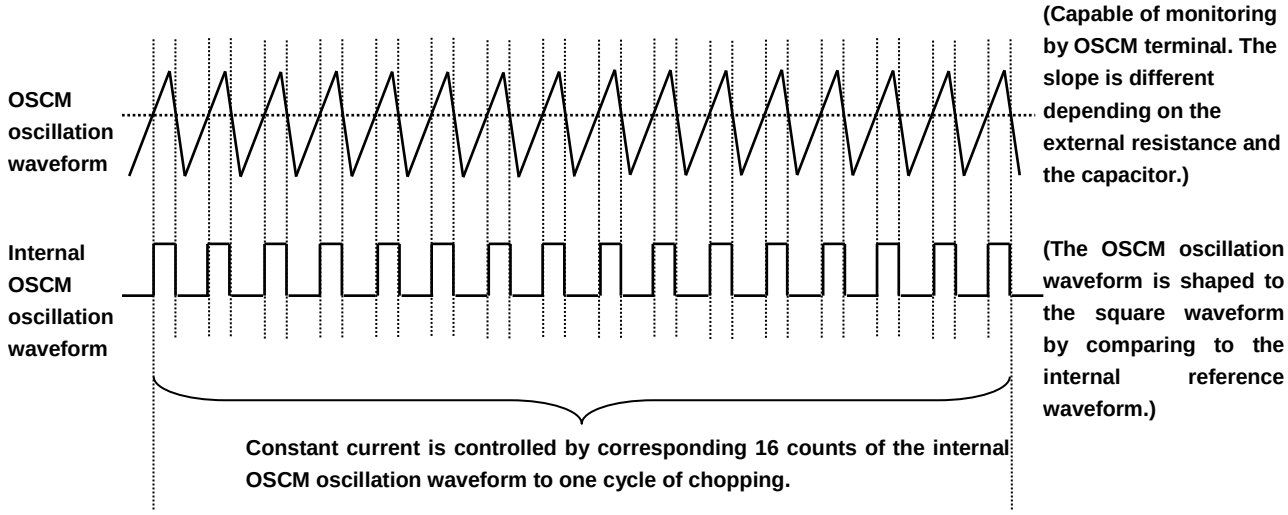


Figure 4.1 OSCM oscillation frequency

When the chopping frequency is increased, the motor can rotate faster because the following capability of the current steps increases. However, switching loss and heat increase may occur because the number of switching of output MOSFET is larger than the case of low frequency of the chopping.

(Example 1) Chopping frequency (fchop) = 100 kHz

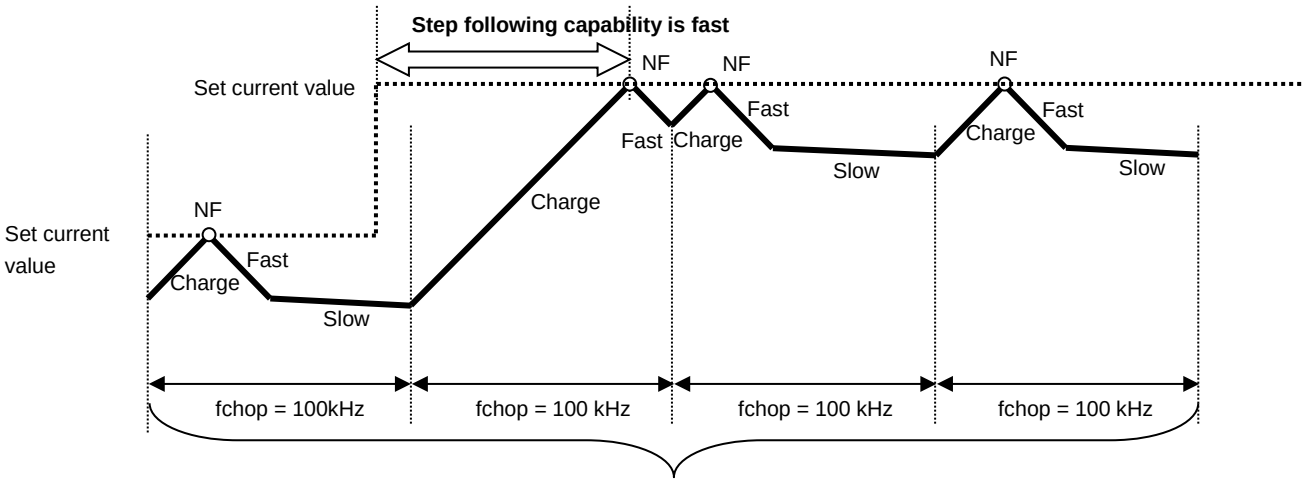


Figure 4.2 Chopping frequency (100 kHz)

(Example 2) Chopping frequency (fchop) = 50 kHz

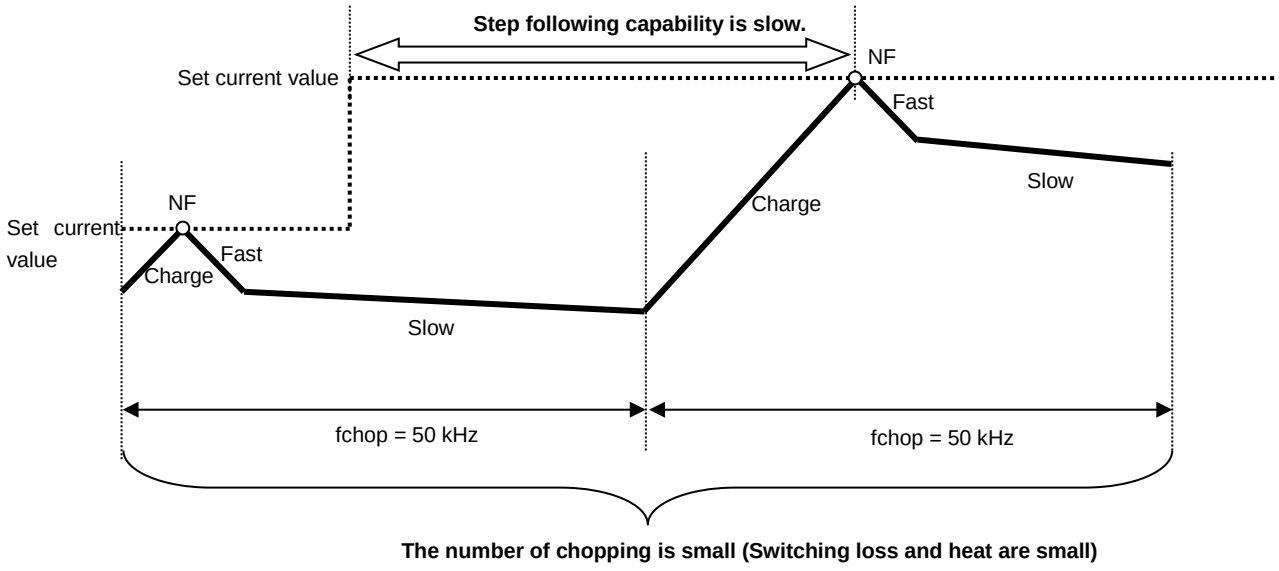


Figure 4.3 Chopping frequency (50 kHz)

Generally, it is recommended to configure the frequency in the range of 50 kHz to 100 kHz on the basis of 70kHz.

5. Current waveform of each current control system

TB67S103A builds in four kinds of current control systems. A current control system can be changed in a serial-data input (BANK1 < D7:D6>).

« 1 » Mixed decay mode current waveform

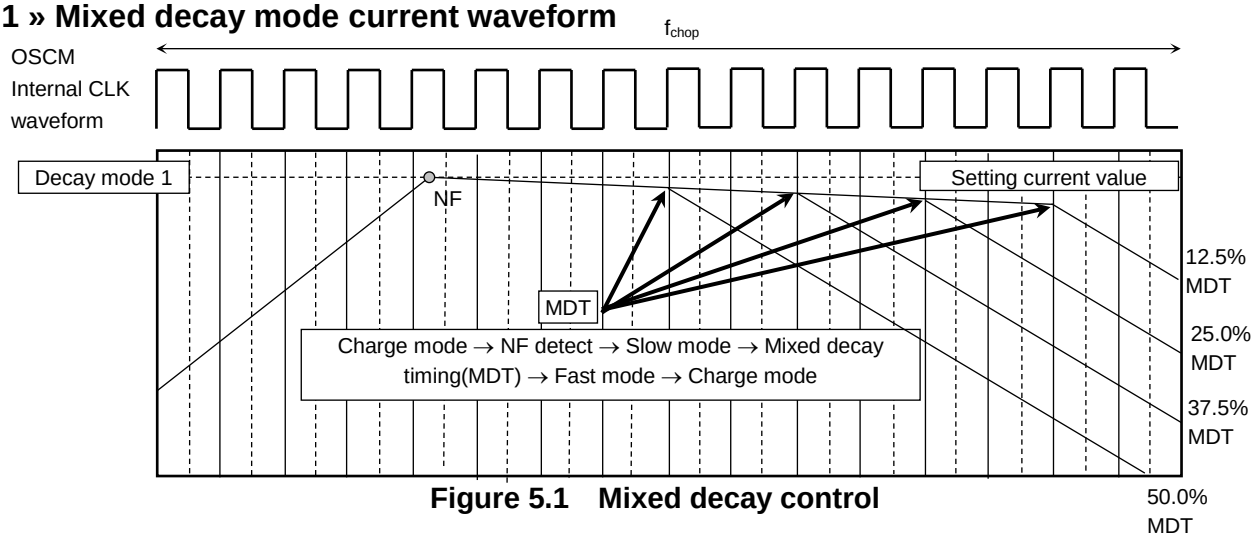


Figure 5.1 Mixed decay control

« 2 » Fast decay mode current waveform

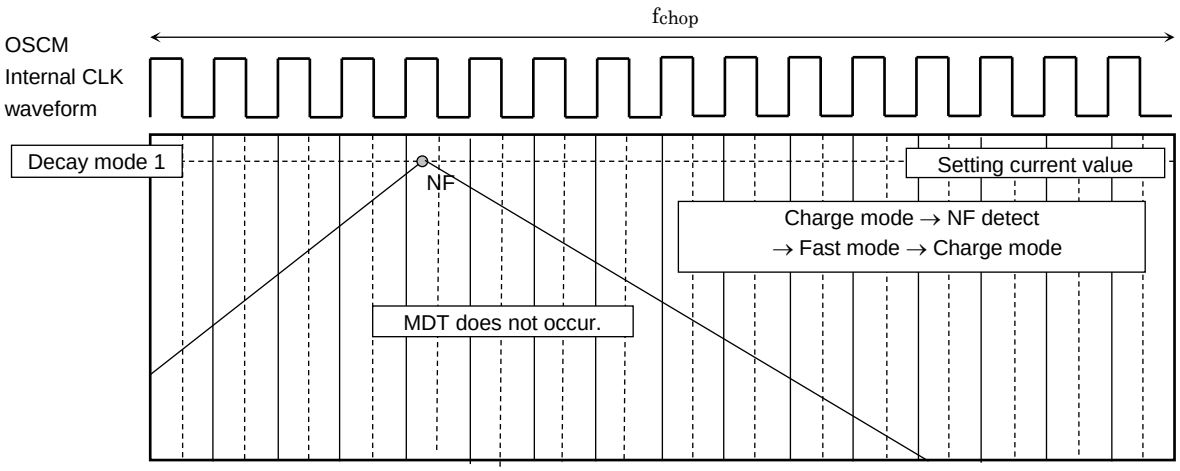


Figure 5.2 Fast decay control

« 3 » Slow decay mode current waveform

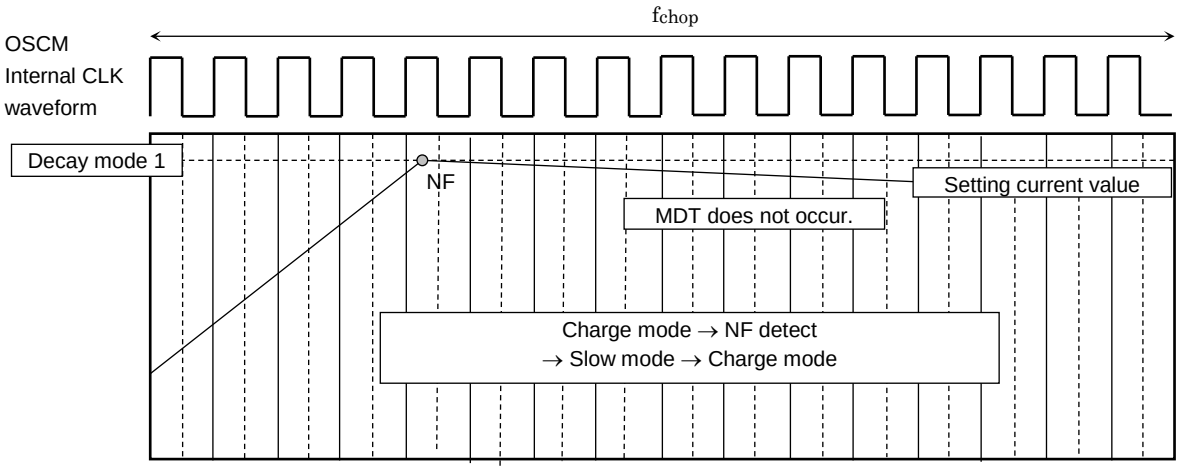


Figure 5.3 Slow decay control

Timing charts may be simplified for explanatory purpose.

« 4 » ADMD current waveform

The Advanced Dynamic Mixed Decay threshold, which determines the current ripple level during current feedback control, is a unique value.

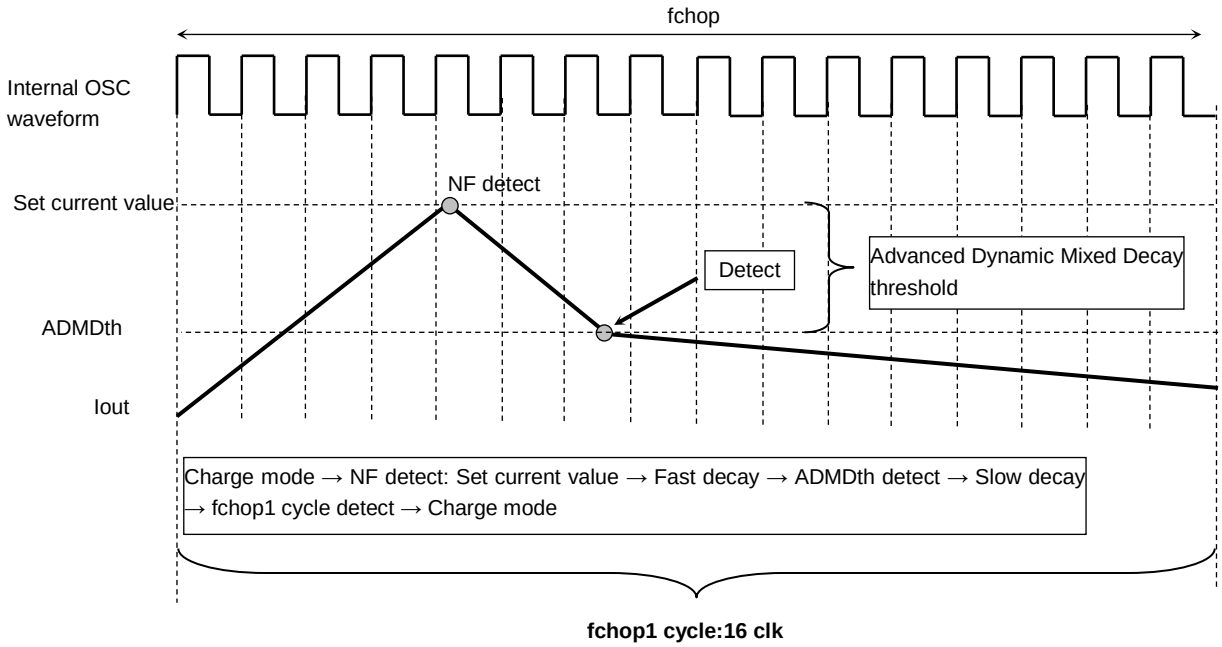
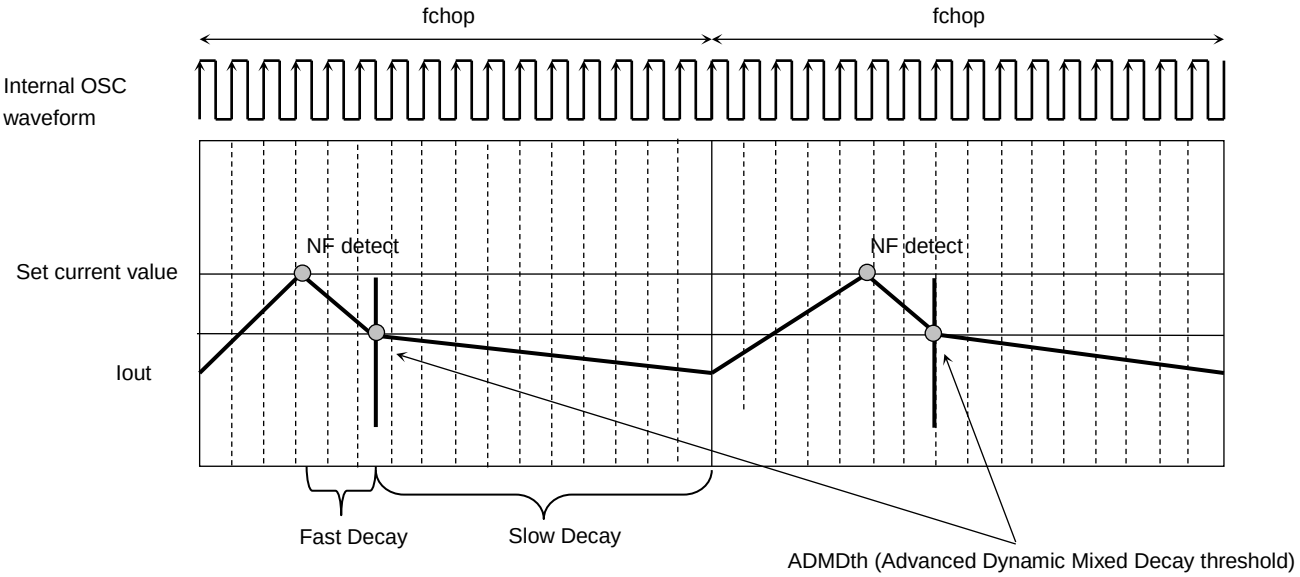


Figure 5.4 ADMD control

ADMD waveform (current waveform)



Timing charts may be simplified for explanatory purpose.

Figure 5.5 ADMD waveform

ADMD current waveform

- **When the next current step is higher:**

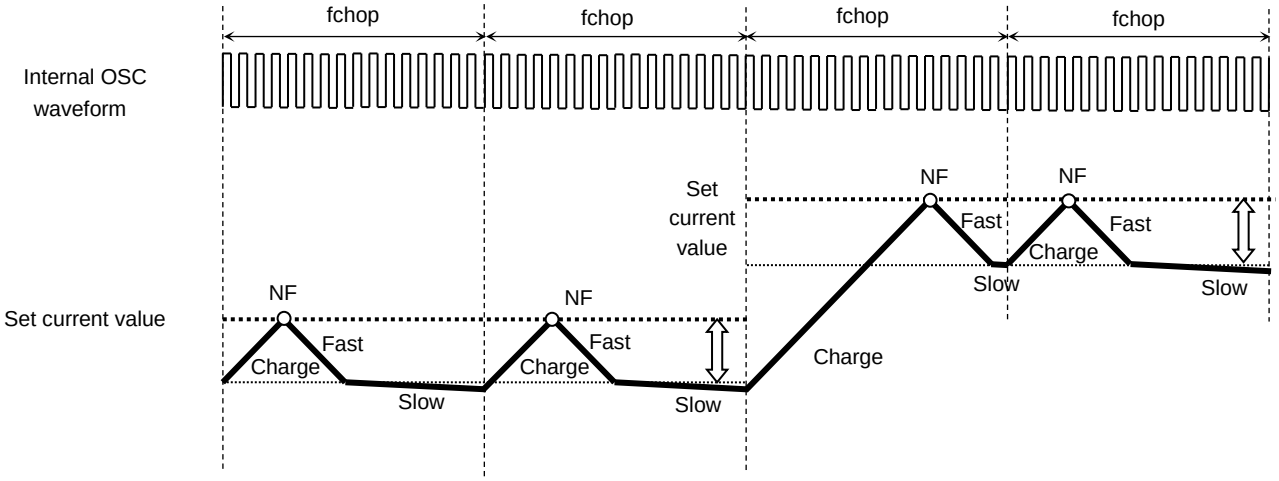


Figure 5.6 ADMD current waveform

- **When Charge period is more than 1 fchop cycle:**

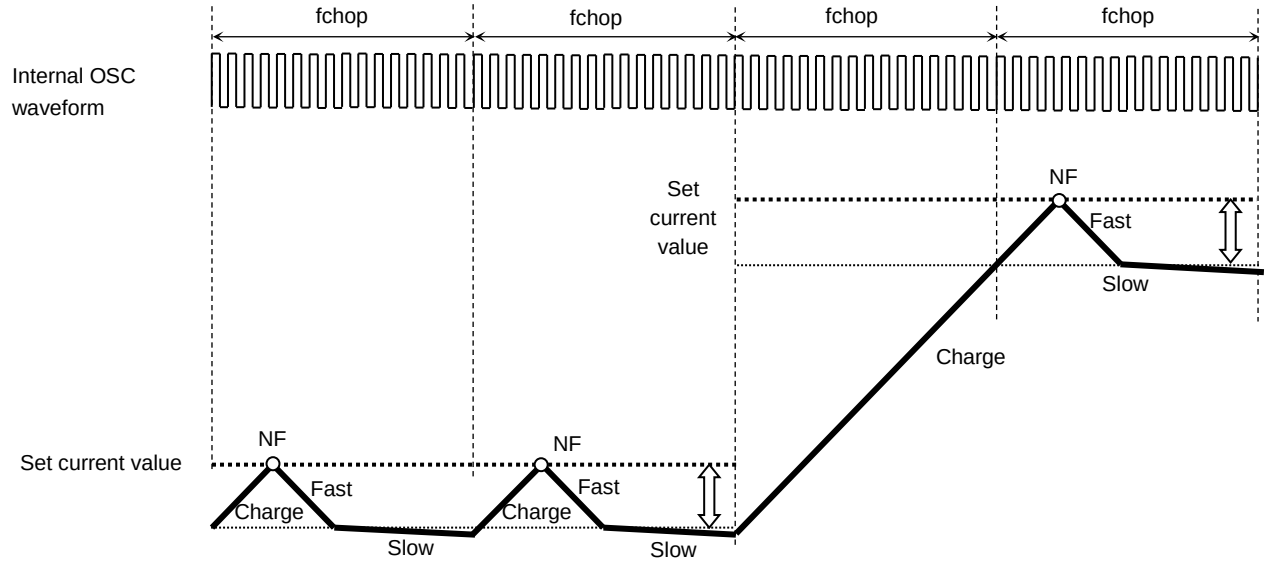


Figure 5.7 ADMD current waveform (When Charge period is more than 1 fchop cycle)

When the Charge period is longer than fchop cycle, the Charge period will be extended until the motor current reaches the NF threshold. Once the current reaches the next current step, then the sequence will go on to decay mode.

- **When the next current step is lower:**

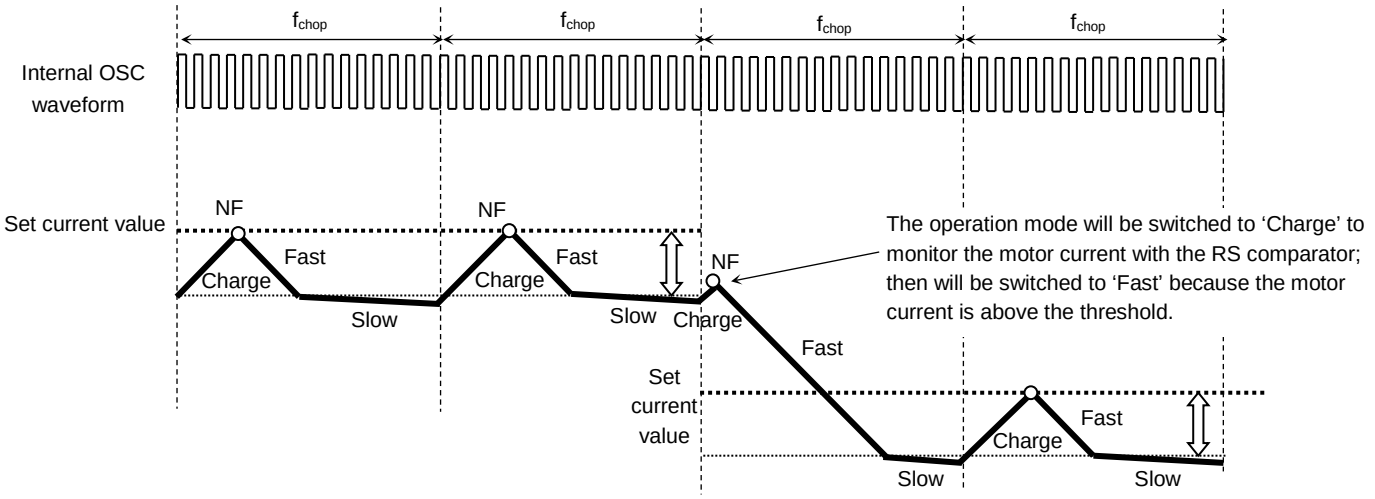


Figure 5.8 ADMD current waveform (When the next current step is lower)

- **When the Fast continues past 1 fchop cycle (the motor current not reaching the ADMD threshold during 1 fchop cycle)**

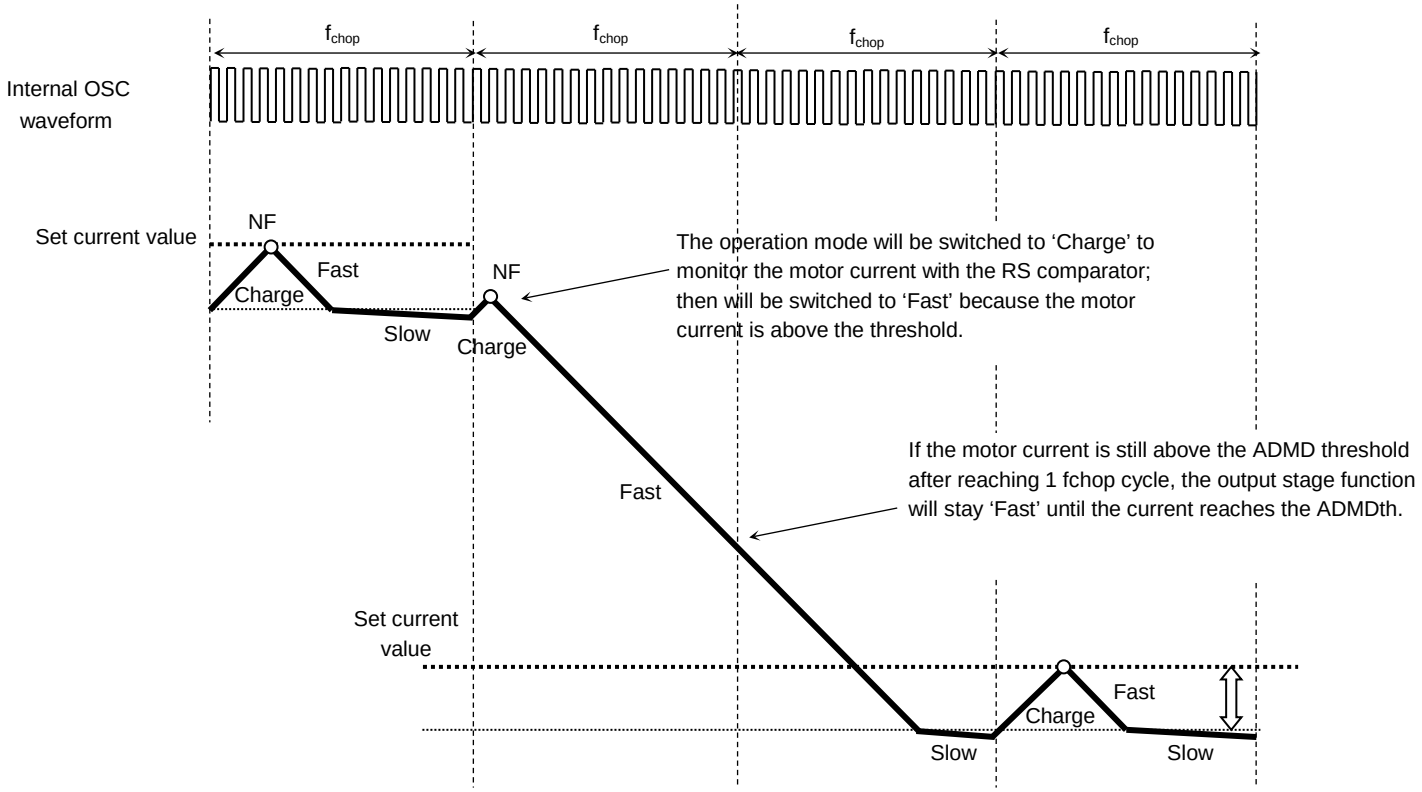


Figure 5.9 ADMD current waveform (When the Fast continues past 1 fchop cycle)

6. Switching characteristics

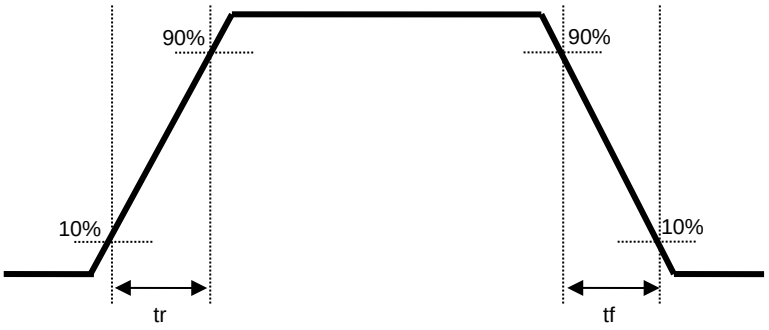


Figure 6.1 Switching characteristics

Table 6.1 Switching characteristics

T_a = 25°C, VM = 24 V, No load

Item	Typ.	Unit
tr	80	ns
tf	90	ns

7. Function explanation

(1) CLK function

Each up-edge of the CLK signal will shift the motor's electrical angle per step.

Table 7.1 CLK function

CLK input	Function
Up-edge	Shifts the electrical angle per step.
Down-edge	- (State of the electrical angle does not change.)

(2) ENABLE function

The ENABLE pin controls the ON and OFF of the corresponding output stage. This pin serves to select if the motor is stopped in Off (High impedance) mode or activated. Please set the ENABLE pin to 'L' during VM power-on and power-off sequence.

Table 7.2 ENABLE function

ENABLE Input	Function
H	Output stage='ON' (Normal operation mode)
L	Output stage='OFF' (High impedance mode)

(3) ID pin function

Table 7.3 ID function

ID	<ID1:ID0>			
	<0:0>	<0:1>	<1:0>	<1:1>
R_ID=GND	O	-	-	-
R_ID=33kΩ(1.25V set)	-	O	-	-
R_ID=100kΩ(2.5V set)	-	-	O	-
R_ID=Open	-	-	-	O

It is possible to change ID setup of a device by attaching resistance (or GND short-circuit / Open) to ID terminal. When <ID1:ID0> set up with ID terminal and <ID1:ID0> of a serial input are in agreement, the serial data inputted to the device are made to reflect.

(4)About serial input function

A serial input is effective only when a SSET pin is "H". A setup of operation is possible by 3 line serial input of "SCLK", "SDATA", and "SSET."

■Specification of Setup Mode (timing chart)

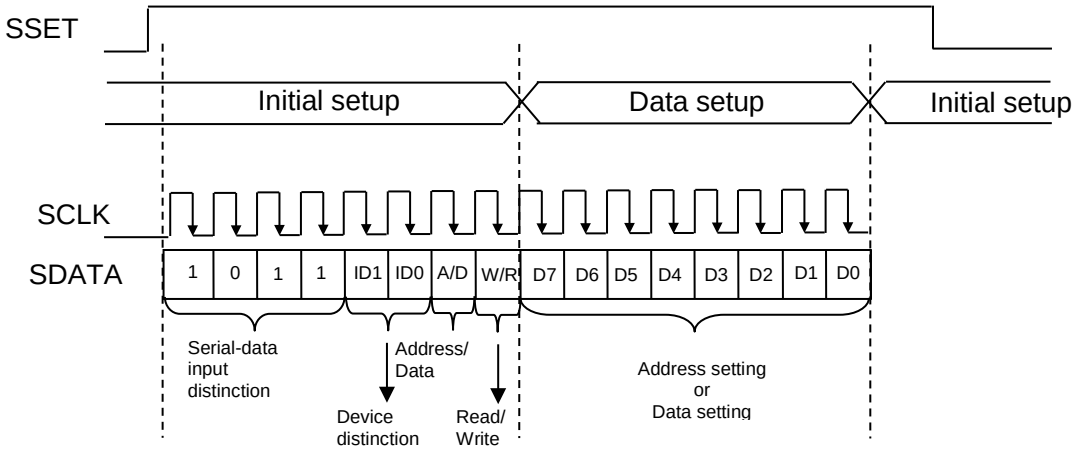


Figure 7.1 Timing chart of serial input

Timing charts may be simplified for explanatory purpose.

Input data is 16-bit composition (it decodes every 8 bits).
Please input serial data in order of the following.
(SSET input is switched to H from L)→ (Initial setup input) → (Data setup input)

In order that TB67S103A may prevent the incorrect input of serial data, it is checked whether serial data have been normally inputted in Initial setup.

(Example) The case of IC of ID setup ='00'
Data setup is received when Initial setup='1011 0000' is inputted.
Data setup is not received when Initial setup='1011 0100' is inputted.
Data setup is not received when Initial setup='1010 0000' is inputted.
Please input “1011(S103 characteristic value)” into 4 bits of heads.

In 1 to 4 bits=”1011” and 5 to 6 bits=”ID setup”, serial data are received.
7 bits is an A/D setup. (0: Address Setup and 1: Data Setup)
8 bits is a W/R setup. (0: Write mode and 1: Read mode)
In Write mode, an address or data is set up by [Data setup].
In Read mode, it is possible to output the value (an address or data) of a register from SO pin.

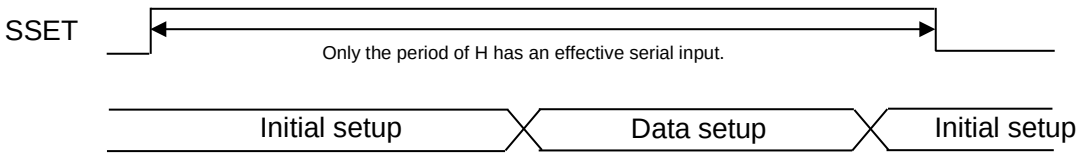


Figure 7.2 Timing chart of SSET signal input

The input of serial data becomes effective only in SSET=H. The serial data inputted between SSET=L are not received.

■About a serial input (Initial setup to Data setup Flow chart)

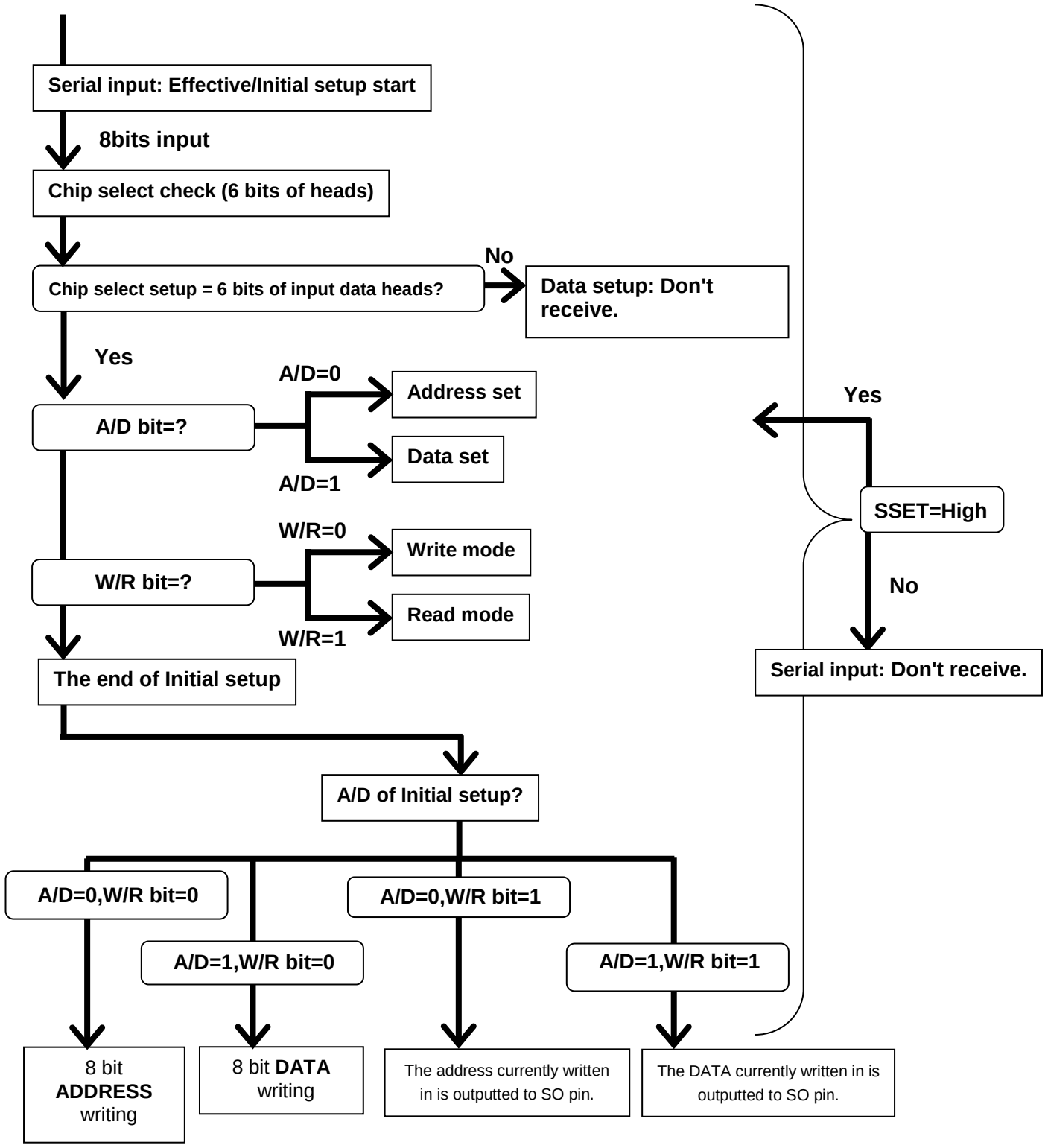


Figure 7.3 Flow chart of serial input

■The change of a Serial bank

Table 7.4 Serial bank change function

DATA Bit			Function
[A2]	[A1]	[A0]	
0	0	0	It is a serial-data input to BANK0.
0	0	1	It is a serial-data input to BANK1.
0	1	0	It is a serial-data input to BANK2.
0	1	1	It is a serial-data input to BANK3.
1	0	0	It is a serial-data input to BANK4.
1	0	1	It is a serial-data input to BANK5.
1	1	0	It is a serial-data input to BANK6.
1	1	1	It is a serial-data input to BANK7.

BANK0: Motor drive: Setup 1 (basic setup)

Table 7.5 BANK0<D7:D6> function

<D7:D6>

DATA Bit		Function
[D7]	[D6]	
0	0	- Don't care
0	1	- Don't care
1	0	- Don't care
1	1	- Don't care

fOSCM=1.6MHz(typ)

Table 7.6 BANK0<D5:D4> function

<D5:D4> Motor drive: torque setting

DATA Bit		Function
[D5]	[D4]	
0	0	Iout×40% **(*Initial)**
0	1	Iout×60%
1	0	Iout×80%
1	1	Iout×100%

Table 7.7 BANK0<D3> function

< D3> Motor drive: CW/CCW setting

DATA Bit	Function
[D3]	
0	CCW (At the time of charge OUT+pin: L, OUT-pin: H) (***Initial)**
1	CW (At the time of charge OUT+pin: H, OUT-pin: L)

Table **7.8 BANK0<D2:D0> function**

<D2:D0> Motor drive: Step resolution setting

DATA Bit			Function
[D2]	[D1]	[D0]	
0	0	0	Standby mode (Power-saving mode) **(*Initial)** (Note)
0	0	1	Full step resolution
0	1	0	Half step resolution(Type (A))
0	1	1	Quarter step resolution
1	0	0	Half step resolution(Type (B))
1	0	1	1/8 step resolution
1	1	0	1/16 step resolution
1	1	1	1/32 step resolution

(Note) Standby mode: the OSCM is disabled and the output stage is set to 'OFF' status.

BANK1: Motor drive: Setup 2 (basic setup)

Table 7.9 BANK1<D7:D6> function

< D7:D6> Motor drive: Decay mode setting

DATA Bit		Function
[D7]	[D6]	
0	0	Mixed Decay mode **(*Initial)**
0	1	Slow Decay only
1	0	Fast Decay only
1	1	ADMD mode

***About a Decay mode setting: Please carry out change to Auto Decay mode(<D7:D6>=[1,1]) after stopping a motor.**

Table 7.10 BANK1<D5:D4> function

<D5:D4> Motor drive: fchop setting

DATA Bit		Function
[D5]	[D4]	
0	0	fchop=100kHz **(*Initial)**
0	1	fchop=50kHz
1	0	fchop=66.6kHz
1	1	Test mode (Don't use)

At the time of fOSCM=1.6MHz(typ) setting, fchop=100kHz

Table 7.11 BANK0<D3:D2> function

< D3:D2> Motor drive: Mixed decay timing(MDT) setting

DATA Bit		Function
[D3]	[D2]	
0	0	MDT=37.5% **(*Initial)**
0	1	MDT=50%
1	0	MDT=25%
1	1	MDT=12.5%

***About MDTsetting: Only in Mixed Decay mode(<D7:D6>=[0,0]), this setup is effective.**

Table 7.12 BANK1<D1:D0> function

<D1:D0> Motor drive: revolving speed setting

DATA Bit		Function
[D1]	[D0]	
0	0	fCLK×100% **(*Initial)**
0	1	fCLK×50%
1	0	fCLK×25%
1	1	fCLK×12.5%

***When a setup of BANK is changed during operation, it is reflected in the timing of the next fchop start.**

BANK2 Others: Option setup (Reference value)

Table 7.13 BANK2<D7:D6> function

< D7:D6> Error detection function: ISD Masking time setting

DATA Bit		Function
[D7]	[D6]	
0	0	8×1/foscs (1.25μs) **(*Initial)**
0	1	4×1/foscs (0.625μs)
1	0	16×1/foscs (2.5μs)
1	1	32×1/foscs (5.0μs)

Table 7.14 BANK2<D5:D4> function

< D5:D4> Error detection function: TSD Masking time setting

DATA Bit		Function
[D5]	[D4]	
0	0	16×1/foscs (2.5μs) **(*Initial)**
0	1	4×1/foscs (0.625μs)
1	0	8×1/foscs (1.25μs)
1	1	32×1/foscs (5.0μs)

Table 7.15 BANK2<D3:D2> function

< D3:D2> Error detection function: VRS Masking time setting

DATA Bit		Function
[D3]	[D2]	
0	0	8×1/foscs (1.25μs) **(*Initial)**
0	1	4×1/foscs (0.625μs)
1	0	16×1/foscs (2.5μs)
1	1	32×1/foscs (5.0μs)

*foscs=6.4MHz(typ) internal clock
SERIAL DATA: BANK2 <D7:D6>(ISD Masking time)/<D3:D2>(VRS Masking time)
In the case of ”0,0”: About 1/foscs×7 to 8clk(1.09μs to 1.25μs)
In the case of ”0,1”: About 1/foscs×3 to 4clk(0.47μs to 0.63μs)
In the case of ”1,0”: About 1/(foscs/2) ×7 to 8clk=1/foscs×14 to 16clk(2.5μs to 2.8μs)
In the case of ”1,1”: About 1/(foscs/4) ×7 to 8clk=1/foscs×32 to 36clk(5.0μs to 5.6μs)
*foscs=6.4MHz(typ) internal clock
SERIAL DATA: BANK2 <D:5/D4>(TSD Masking time)
In the case of ”0,0”: About 1/(foscs/2) ×7 to 8clk=1/foscs×14 to 16clk(2.5μs to 2.8μs)
In the case of ”0,1”: About 1/foscs×3 to 4clk(0.47μs to 0.63μs)
In the case of ”1,0”: About 1/foscs×7 to 8clk(1.09μs to 1.25μs)
In the case of ”1,1”: About 1/(foscs/4) ×7 to 8clk=1/foscs×32 to 36clk(5.0μs to 5.6μs)

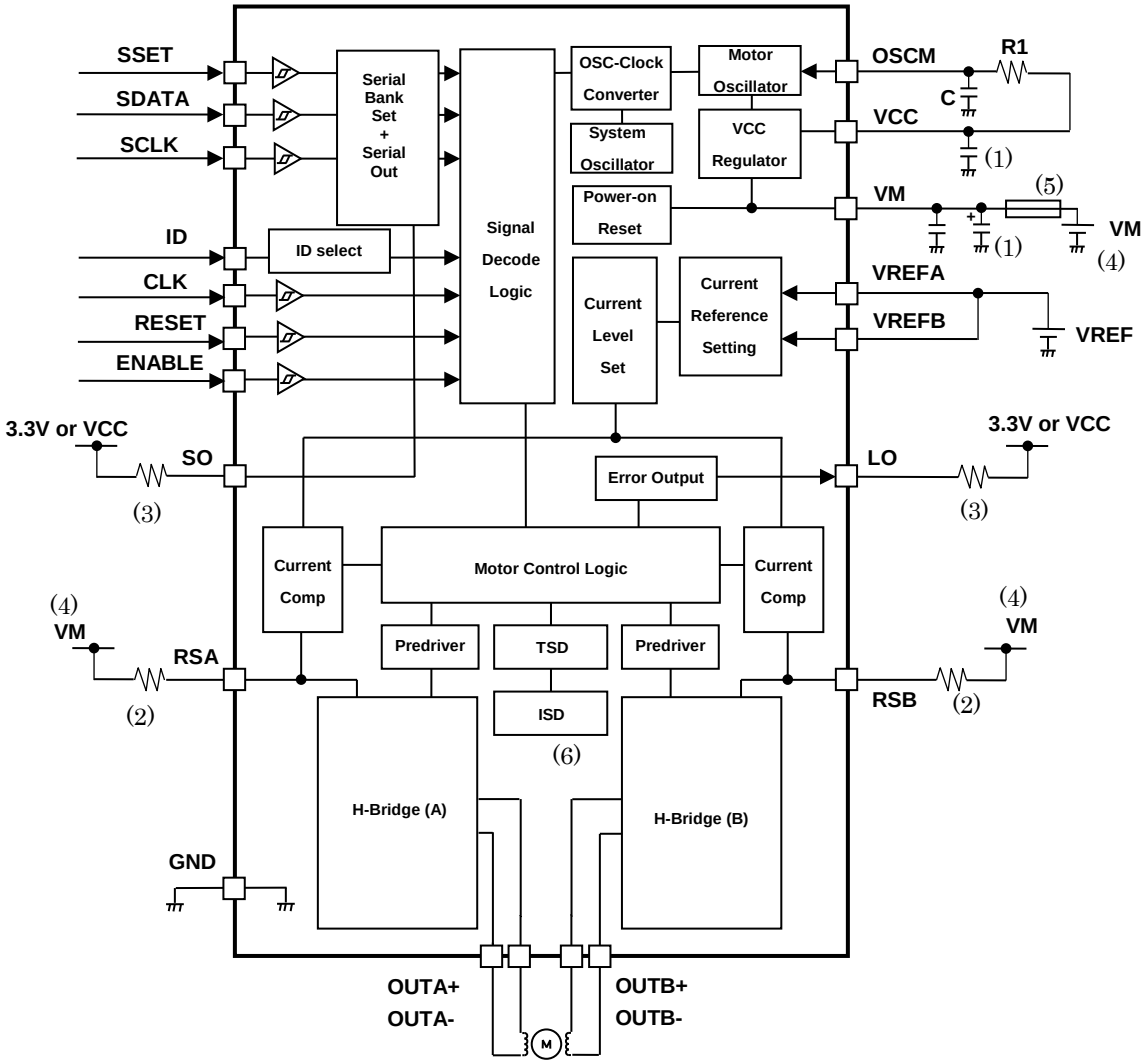
Table 7.16 BANK2<D1:D0> function

< D1:D0> Motor drive: Digital tblank setting

DATA Bit		Function
[D1]	[D0]	
0	0	2×1/fOSCM **(*Initial)**
0	1	3×1/fOSCM
1	0	4×1/fOSCM
1	1	6×1/fOSCM

fOSCM=1.6MHz(typ)
***When a setup of BANK is changed during operation, it is reflected in the timing of the next fchop start.**

8. Example of application circuit



The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass-production design stage.

Figure 8.1 Example of application circuit

(1) Capacitor for power supply terminal

To stabilize the power supply voltage of the IC and reduce the noise, connect the appropriate capacitor to each terminal. It is recommended to connect the capacitor as close to the IC as possible. Especially, by connecting the ceramic capacitor near the IC, the change of the power supply at the high frequency range and the noise can be reduced.

Table 8.1 Recommended capacitor values for power supply terminal

Item	Parts	Typ.	Recommended range
VM-GND	Electrolytic capacitor	100 μF	47 to 100 μF
	Ceramic capacitor	0.1 μF	0.01 to 1 μF
VCC-GND	Ceramic / Electrolytic capacitor	0.1 μF	0.01 to 1 μF
(VREF-GND)	Ceramic capacitor	0.1 μF	0.01 to 1 μF

* VREF-GND: Connect the capacitor in necessary depending on the usage environment.
* It is possible to use the capacitor, which is not the recommended capacitor, depending on the motor load condition and the design pattern of the board.

(2) Resistance of current detection

This IC configures the threshold of the constant current detection by connecting the resistance of current detection between VM and RS terminals. The detection resistance is recommended to connect near the IC. (The motor can be controlled with the accurate current because the influence of the wire resistance of the board can be reduced.)

Table 8.2 Recommended resistance values for current detection

Item	Parts	Typ.	Recommended range
VM-RS	Chip / Lead resistance	0.22 Ω (1.5 to 3.0 A)	0.22 to 1.0 Ω
VM-RS	Chip / Lead resistance	0.51 Ω (0 to 1.5 A)	0.22 to 1.0 Ω

The relation equation of the threshold of the constant current detection, Vref voltage, and the resistance of RS detection is as follows;

$$Iout(max) = Vref(gain) \times \frac{Vref(V)}{RRS(\Omega)}$$

Vref(gain): Vref decay ratio is 1 / 5.0(typ.).

As for the resistance of current detection, the constant number which is out of recommended range can be adopted. In this case, please pay attentions to the followings when the used resistance is high and low.

- When the detection resistance is low, the difference voltage between VM and RS comparing to the internal reference voltage becomes small. So, the current may be largely different from the configured current value.
- When the detection resistance is high, the power applied to the detection resistance increases in motor operation (P=I^2×R). So, in case the same current flows as the case of low resistance, the power dissipation should be larger.

(3) Resistance for monitor terminal

This IC has two open-drain terminals of SO and LO. When internal MOSFET is turned off, it is high impedance as a terminal level. In order to operate the IC with accurate high and low levels, connect the pull-up resistance to the power supply of 3.3 V or 5 V in using.

Table 8.3 Recommended resistance for monitor terminal

Item	Parts	Typ.	Recommended range
SO,LO- (3.3V or VCC)	Chip / Lead resistance	10 kΩ	10 to 100 kΩ

(4) Wiring pattern for power supply and GND

Since large current may flow in VM, RS, and GND pattern especially, design the appropriate wiring pattern to avoid the influence of wiring impedance. It is very important for surface mounting package to radiate the heat from the heat sink of the back side of the IC to the GND. So, design the pattern by considering the heat design.

(5) Fuse

Use an appropriate power supply fuse for the power supply line to ensure that a large current does not continuously flow in the case of over-current and/or IC failure.

The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead to smoke or ignition. To minimize the effects of the flow of a large current in the case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

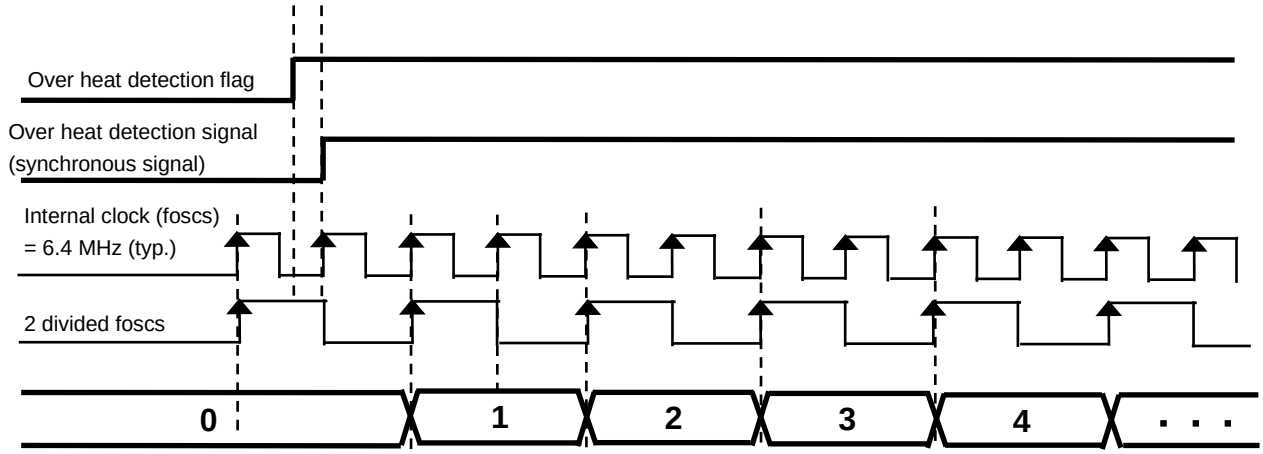
This IC incorporates over current detection circuit (ISD) that turns off the output of the IC when over current is detected in the IC. However, it does not necessarily protect ICs under all circumstances. If the Over current detection circuits operate against the over current, clear the over current status immediately. Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the over current detection circuit to not operate properly or IC breakdown before operation. In addition, depending on the method of use and usage conditions, if over current continues to flow for a long time after operation, the IC may generate heat resulting in breakdown.

To avoid above IC destruction and malfunctions caused by noise, the over current detection circuit has a dead band time. So, it is concerned that the over current detection circuit may not operate depending on the output load conditions because of the dead band time. Therefore, in order to avoid continuing this abnormal state, use the fuse for the power supply line.

(6) Abnormality detection function

- Thermal shutdown circuit (TSD)
  When the IC detects an over temperature, the internal circuit turns off the output MOSFETs. It has a dead band time to avoid TSD misdetection, which may be triggered by external noise. Reassert the VM power supply or use the standby mode to release this function. The TSD is triggered when the device is over heated irregularly. Make sure not to use the TSD function aggressively.

Dead band time of TSD



Timing charts may be simplified for explanatory purposes.

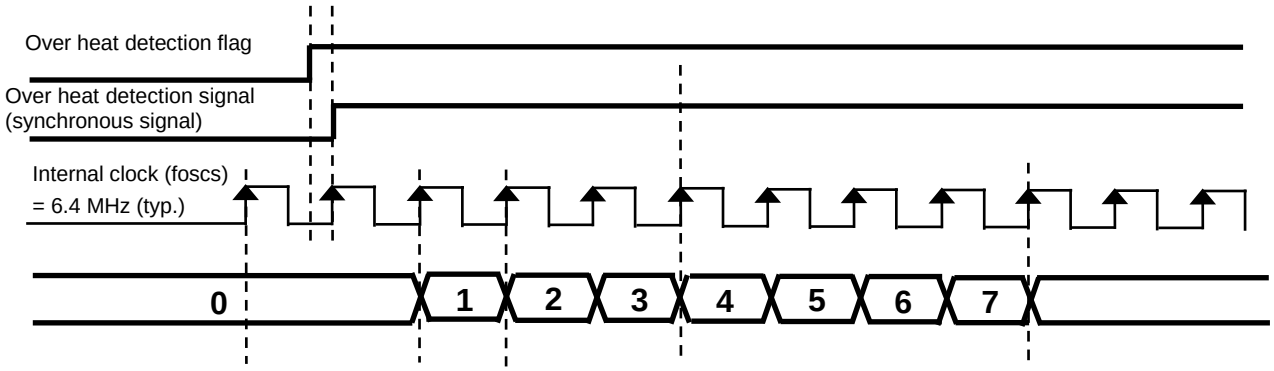
Figure 8.2 Dead band time of thermal shutdown circuit

Thermal shutdown circuit has a dead band time to avoid false detection. This dead band time is configured by counting up the internal counter by the fixed frequency (6.4 MHz(typ.)) in the IC.

※ foscs = 6.4 MHz(typ.) internal clock
1 / (foscs / 2) × 7 to 8 clk = 1 / foscs × 14 to 16 clk (2.5 to 2.8 μs)

- Over current detection (ISD)
  When the IC detects an over current, the internal circuits turns off the output MOSFETs. It has a dead band time to avoid ISD misdetection, which may be triggered by external noise. Reassert the VM power supply or use the standby mode to release this function.

Dead band time of ISD



Timing charts may be simplified for explanatory purposes.

Figure 8.3 Dead band time of ISD

ISD has a dead band time to avoid false detection caused by spike current in switching. This dead band time is configured by counting up the internal counter by the fixed frequency (6.4 MHz(typ.)) in the IC.

※ foscs = 6.4 MHz(typ.) internal clock
1 / foscs × 7 to 8 clk (1.09 to 1.25 μs)

9. Power consumption of the IC

Power of the IC is consumed by the transistor of the output block and that of the logic block mainly.

P(total) = P(out) + P(bias)

- Power consumption of the motor output block
  Power of the output block (P(out)) is consumed by MOSFET of upper and lower H-Bridge.

  P(out) =Number of H-Bridge × Iout (A) × VDS (V) = 2 (ch) × Iout (A) × Iout (A) × Ron (Ω).....(1)

When the current waveform of the motor output corresponds to the ideal waveform (2-phase excitation / square wave), average power of output block can be provided as follows;

When Ron = 0.49Ω, Iout (peak: Max) = 1.5 A, VM = 24 V
P(out) = 2 (ch) × 1.5 (A) × 1.5 (A) × 0.49 (Ω).....(2)
= 2.205 (W)

- Power consumption of logic and IM systems.
  Power consumptions of logic and IM systems are calculated by separating the states (operating and stopping).

  I (IM3) = 5.5 mA (typ.) : Operating
  I (IM2) = 3.5 mA (typ.) : Stopping

Output system is connected to VM (24V). (Output system: Current consumed by the circuit connected to VM + Current consumed by switching output steps)

Power consumption is calculated as follows;

P(bias) = 24 (V) × 0.0055 (A).....(3)
= 0.132 (W)

- Power consumption
  Total power consumption P(total) is calculated from the values of formula (2) and (3).

  P(total) = P(out) + P(bias) = 2.205 + 0.132 = 2.337 (W)

Standby mode is released. The power consumption in non-operation mode of the motor (waiting mode) is calculated as follows;

P = 24 (V) × 0.0035 (A) = 0.084 (W)

In actual motor operation, the average current becomes lower than the calculated value because of transition time of the current steps and the ripple of the constant current PWM. Refer to the above equations, evaluate the heat design of the board by the actual board enough, and configure the appropriate margin.

10. Power dissipation

Relation equation of the ambient temperature (T_a), junction temperature (T_j), and the heat resistance ($R_{th(j-a)}$) between junction temperature to ambient temperature is as follows;

$$T_j = T_a + P \times R_{th(j-a)}$$

(Example) When 4-layer mounting board ($R_{th(j-a)}$ = 25°C/W), T_a = 25°C, P(total) = 2.337 W (I_{out} = 1.5 A, 2-phase excitation)

T_j = 25 (°C) + 25 (°C/W) × 2.337 (W) = 83.425°C

(Reference) Relation between the power dissipation and the ambient temperature

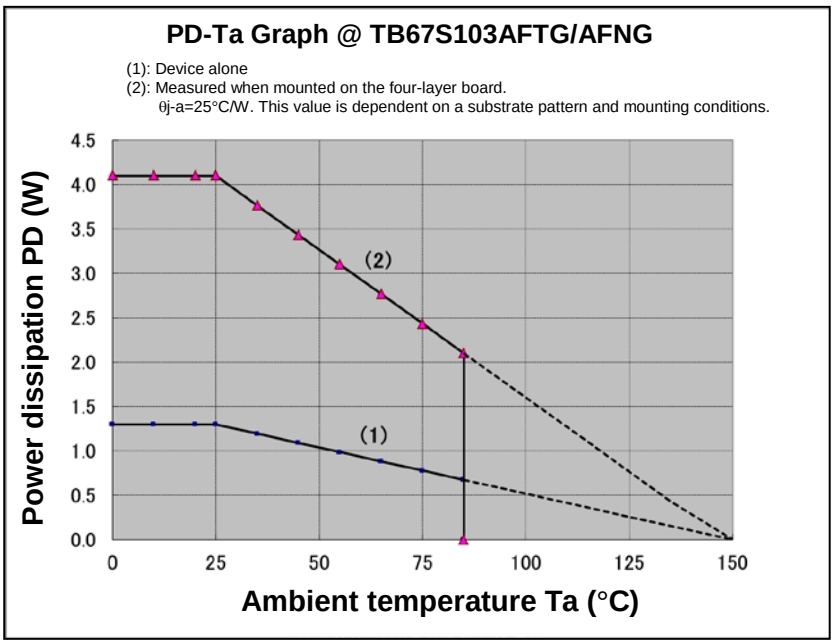


Figure 10.1 Power dissipation

※ Pay attention that T_a, $R_{th(j-a)}$, and P(total) depend on the usage environment. When ambient temperature is high, the allowable power consumption decreases.

11. Example of reference foot pattern

(1) QFN48 foot pattern (unit: mm)

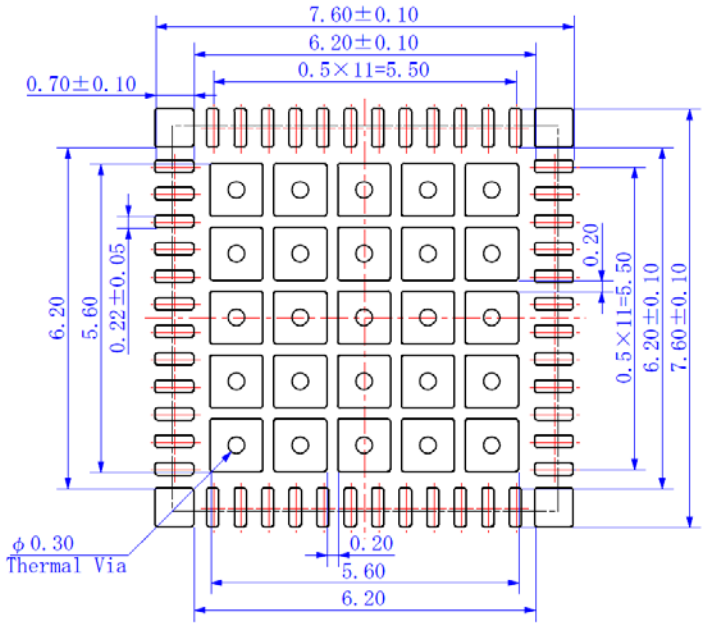


Figure 11.1 QFN48 foot pattern

(2) HTSSOP48 foot pattern (unit: mm)

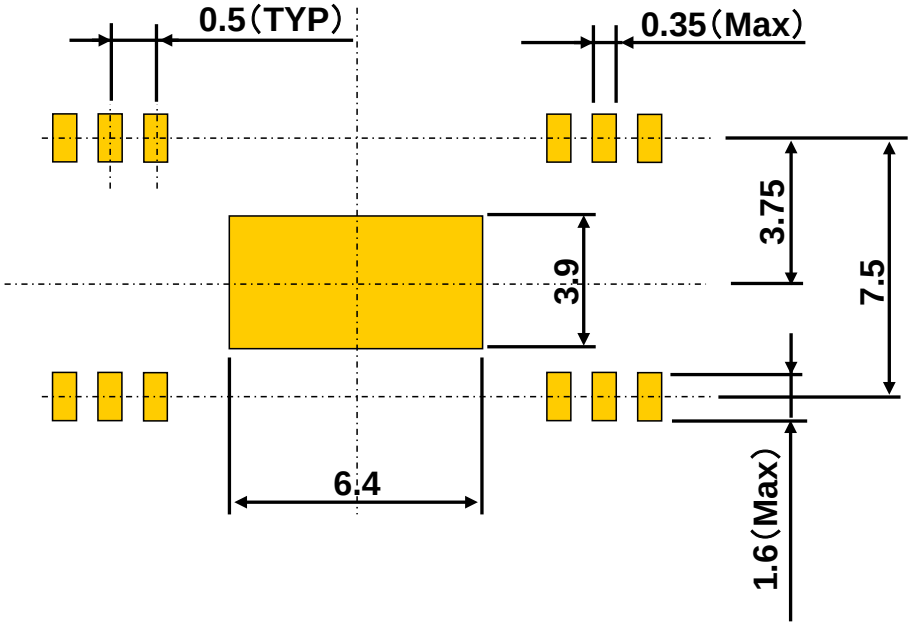


Figure 11.2 HTSSOP48 foot pattern

Toshiba does not guarantee the data for mass production. Please use the data as reference data for customer's application.

Note: In determining the size of mounting board, design the most appropriate pattern by considering the solder bridge, the solder connecting strength, the pattern accuracy in making board, the heat sink of leads, and the mounting accuracy of the IC board.

12. Board dimensions

12.1. Input

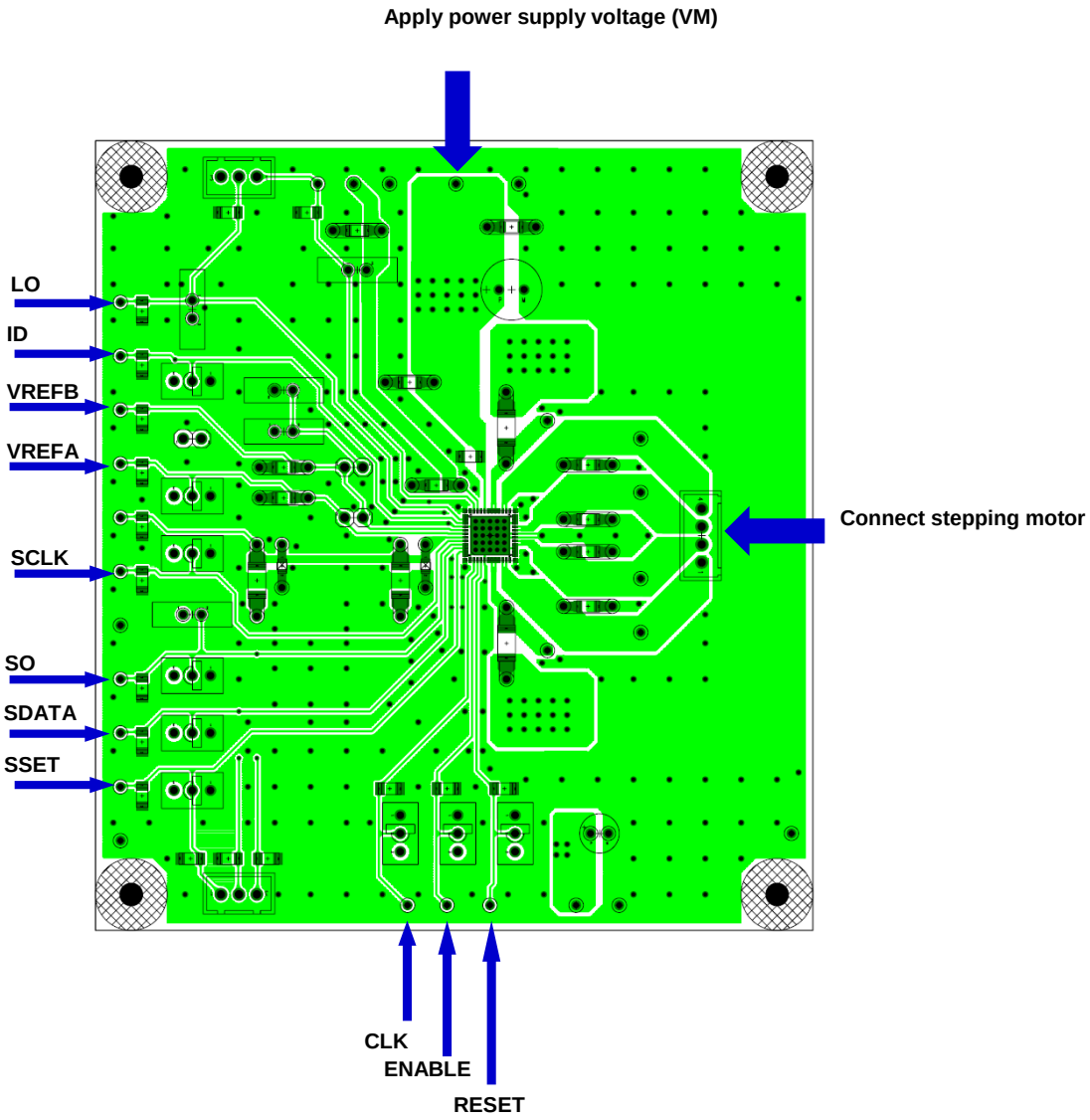


Figure 12.1 Input

Input each power supply and control signal according to above figure.

12.2. Main part

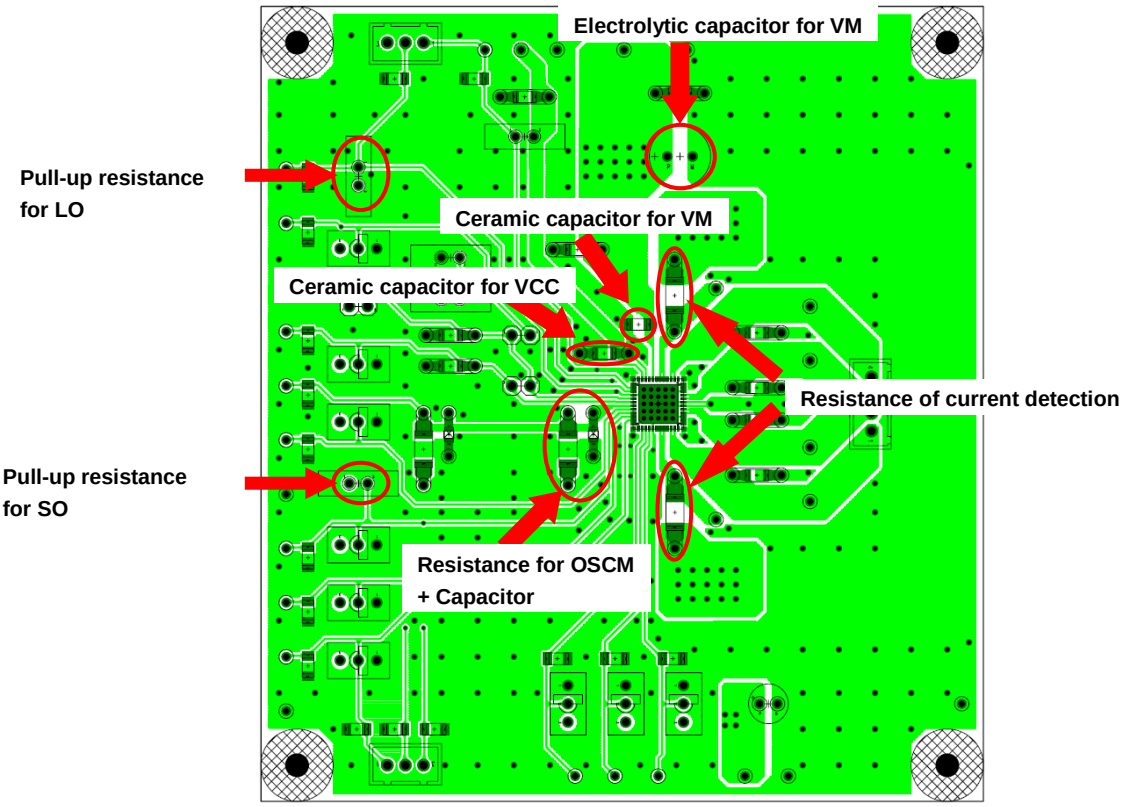


Figure 12.2 Main part

Connect each part referring to “Example of application circuit”.

12.3. Options

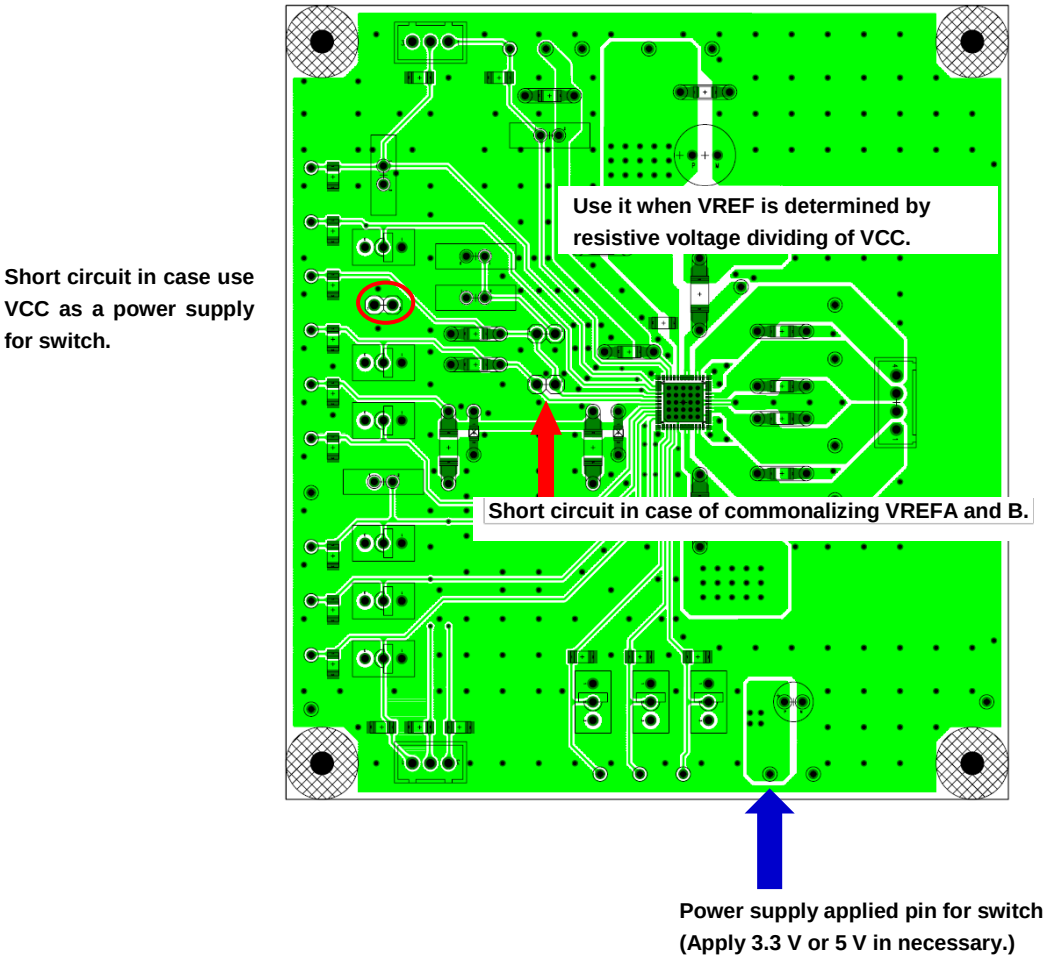


Figure 12.3 Options

Notes on Contents

Block Diagrams

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

Timing Charts

Timing charts may be simplified for explanatory purposes.

Application Circuits

The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass-production design stage.
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Test Circuits

Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

IC Usage Considerations

Notes on handling of ICs

(1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.Exceeding the rating(s) may cause device breakdown, damage or deterioration, and may result in injury by explosion or combustion.

(2) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in the case of overcurrent and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead to smoke or ignition. To minimize the effects of the flow of a large current in the case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

(3) If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition. Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

(4) Do not insert devices in the wrong orientation or incorrectly. Make sure that the positive and negative terminals of power supplies are connected properly.
Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause device breakdown, damage or deterioration, and may result in injury by explosion or combustion.
In addition, do not use any device inserted in the wrong orientation or incorrectly to which current is applied even just once.

(5) Carefully select external components (such as inputs and negative feedback capacitors) and load components (such as speakers), for example, power amp and regulator.
If there is a large amount of leakage current such as from input or negative feedback condenser, the IC output DC voltage will increase. If this output voltage is connected to a speaker with low input withstand voltage, overcurrent or IC failure may cause smoke or ignition. (The overcurrent may cause smoke or ignition from the IC itself.) In particular, please pay attention when using a Bridge Tied Load (BTL) connection-type IC that inputs output DC voltage to a speaker directly.

Points to remember on handling of ICs

Overcurrent detection Circuit

Overcurrent detection circuits (referred to as current limiter circuits) do not necessarily protect ICs under all circumstances. If the overcurrent detection circuits operate against the overcurrent, clear the overcurrent status immediately.
Depending on the method of use and usage conditions, exceeding absolute maximum ratings may cause the overcurrent detection circuit to operate improperly or IC breakdown may occur before operation. In addition, depending on the method of use and usage conditions, if overcurrent continues to flow for a long time after operation, the IC may generate heat resulting in breakdown.

Thermal Shutdown Circuit

Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over-temperature, clear the heat generation status immediately.
Depending on the method of use and usage conditions, exceeding absolute maximum ratings may cause the thermal shutdown circuit to operate improperly or IC breakdown to occur before operation.

Heat Radiation Design

When using an IC with large current flow such as power amp, regulator or driver, design the device so that heat is appropriately radiated, in order not to exceed the specified junction temperature (TJ) at any time or under any condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, when designing the device, take into consideration the effect of IC heat radiation with peripheral components.

Back-EMF

When a motor rotates in the reverse direction, stops or slows abruptly, current flows back to the motor's power supply owing to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond the absolute maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

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