

MOSFETs Silicon P-Channel MOS (U-MOSVI)

# SSM3J352F

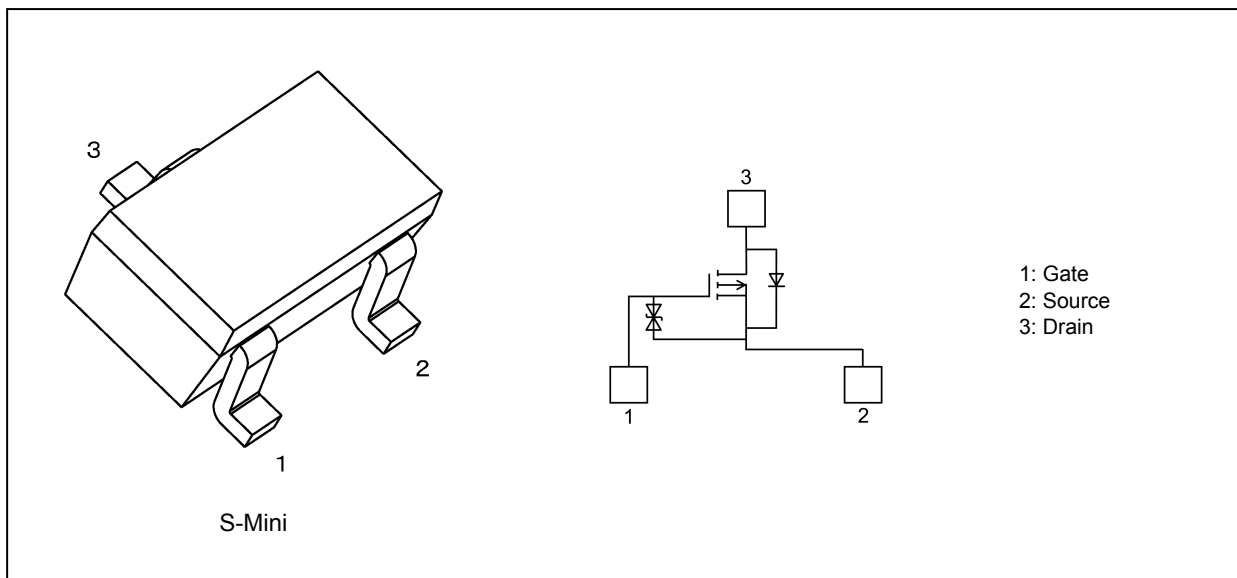
## 1. Applications

- Power Management Switches

## 2. Features

- (1) 1.8 V gate drive voltage.
- (2) Low drain-source on-resistance
  - :  $R_{DS(ON)} = 443 \text{ m}\Omega$  (max) (@ $V_{GS} = -1.8 \text{ V}$ )
  - $R_{DS(ON)} = 199 \text{ m}\Omega$  (max) (@ $V_{GS} = -2.5 \text{ V}$ )
  - $R_{DS(ON)} = 136 \text{ m}\Omega$  (max) (@ $V_{GS} = -4.5 \text{ V}$ )
  - $R_{DS(ON)} = 110 \text{ m}\Omega$  (max) (@ $V_{GS} = -10 \text{ V}$ )

## 3. Packaging and Pin Assignment



Start of commercial production  
2015-12

### 4. Absolute Maximum Ratings (Note) (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$ )

Characteristics	Symbol	Rating	Unit
Drain-source voltage	$V_{DSS}$	-20	V
Gate-source voltage	$V_{GSS}$	$\pm 12$	
Drain current (DC) (Note 1)	$I_D$	-2	A
Drain current (pulsed) (Note 1), (Note 2)	$I_{DP}$	-4	
Power dissipation (Note 3)	$P_D$	600	mW
Power dissipation $t \leq 1\text{ s}$ (Note 3)		1200	
Channel temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage temperature	$T_{stg}$	-55 to 150	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Ensure that the channel temperature does not exceed  $150\text{ }^\circ\text{C}$ .

Note 2: Repetitive rating; pulse width limited by maximum channel temperature.

Note 3: Device mounted on an FR4 board.(25.4 mm × 25.4 mm × 1.6 mm, Cu pad: 645 mm<sup>2</sup>)

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.

Note: The MOSFETs in this device are sensitive to electrostatic discharge. When handling this device, the worktables, operators, soldering irons and other objects should be protected against anti-static discharge.

Note: The channel-to-ambient thermal resistance,  $R_{th(ch-a)}$ , and the drain power dissipation,  $P_D$ , vary according to the board material, board area, board thickness and pad area. When using this device, be sure to take heat dissipation fully into account.

### 5. Electrical Characteristics

#### 5.1. Static Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$ )

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 10\text{ V}$	—	—	$\pm 1$	$\mu\text{A}$
Drain cut-off current	$I_{DSS}$	$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}$	—	—	-1	
Drain-source breakdown voltage	$V_{(BR)DSS}$	$I_D = -1\text{ mA}, V_{GS} = 0\text{ V}$	-20	—	—	V
Drain-source breakdown voltage (Note 1)	$V_{(BR)DSX}$	$I_D = -1\text{ mA}, V_{GS} = 8\text{ V}$	-12	—	—	
Gate threshold voltage	$V_{th}$	$V_{DS} = -3\text{ V}, I_D = -1\text{ mA}$	-0.50	—	-1.20	
Drain-source on-resistance (Note 2)	$R_{DS(ON)}$	$I_D = -0.4\text{ A}, V_{GS} = -1.8\text{ V}$	—	210	443	$\text{m}\Omega$
		$I_D = -0.6\text{ A}, V_{GS} = -2.5\text{ V}$	—	147	199	
		$I_D = -2.0\text{ A}, V_{GS} = -4.5\text{ V}$	—	108	136	
		$I_D = -2.0\text{ A}, V_{GS} = -10\text{ V}$	—	90	110	
Forward transfer admittance (Note 2)	$ Y_{fs} $	$V_{DS} = -3\text{ V}, I_D = -1\text{ A}$	—	3.8	—	S

Note 1: If a reverse bias is applied between gate and source, this device enters  $V_{(BR)DSX}$  mode. Note that the drain-source breakdown voltage is lowered in this mode.

Note 2: Pulse measurement.

#### 5.2. Dynamic Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$ )

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Input capacitance	$C_{iss}$	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V},$ $f = 1\text{ MHz}$	—	210	—	$\text{pF}$
Reverse transfer capacitance	$C_{rss}$		—	31	—	
Output capacitance	$C_{oss}$		—	39	—	
Switching time (turn-on time)	$t_{on}$	$V_{DD} = -10\text{ V}, I_D = -1\text{ A},$ $V_{GS} = 0\text{ to }-2.5\text{ V}, R_{GS} = 10\text{ }\Omega$	—	31	—	ns
Switching time (turn-off time)	$t_{off}$		—	54	—	

#### 5.3. Switching Time Test Circuit

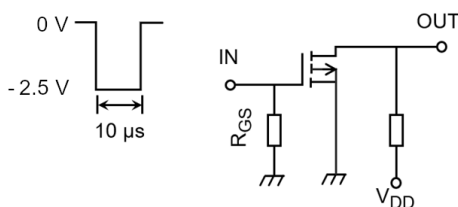


Fig. 5.3.1 Switching Time Test Circuit

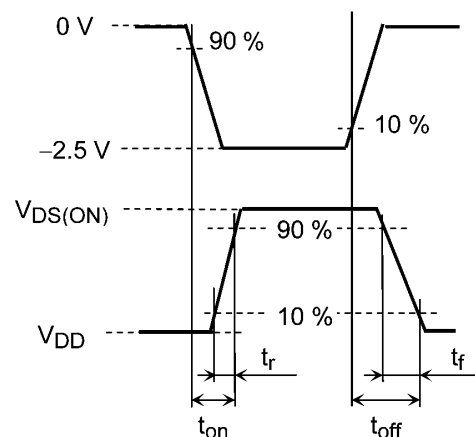


Fig. 5.3.2 Input Waveform/Output Waveform

#### 5.4. Gate Charge Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$ )

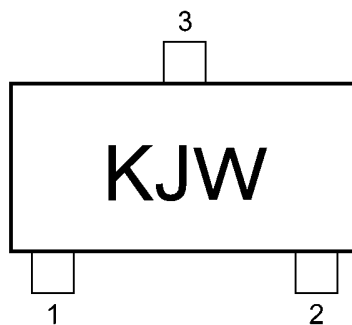
Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Total gate charge (gate-source plus gate-drain)	$Q_g$	$V_{DD} = -10\text{ V}, I_D = -2.0\text{ A},$ $V_{GS} = -4.5\text{ V}$	—	5.1	—	nC
Gate-source charge 1	$Q_{gs1}$		—	2.3	—	
Gate-drain charge	$Q_{gd}$		—	1.5	—	

## 5.5. Source-Drain Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$ )

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Diode forward voltage (Note 1)	$V_{DSF}$	$I_D = 2\text{ A}, V_{GS} = 0\text{ V}$	—	0.9	1.2	V

Note 1: Pulse measurement.

## 6. Marking



### 7. Characteristics Curves (Note)

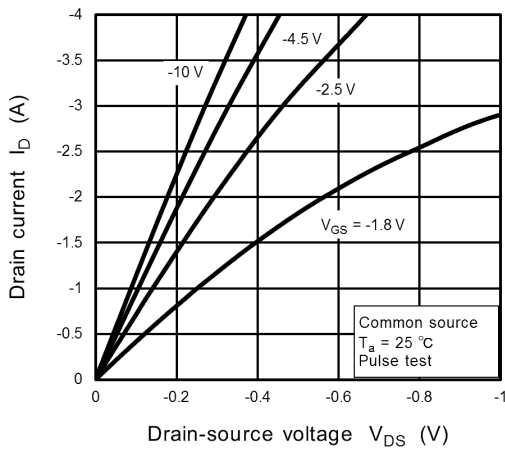


Fig. 7.1  $I_D - V_{DS}$

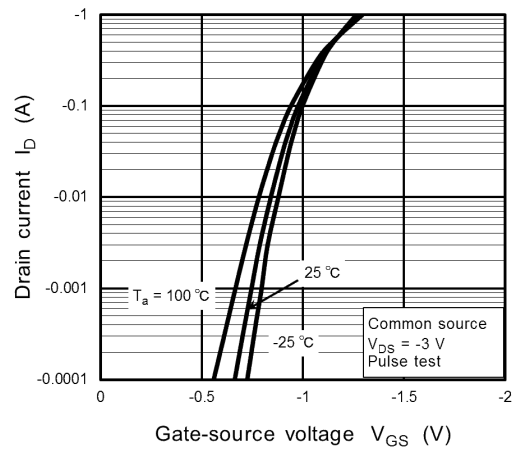


Fig. 7.2  $I_D - V_{GS}$

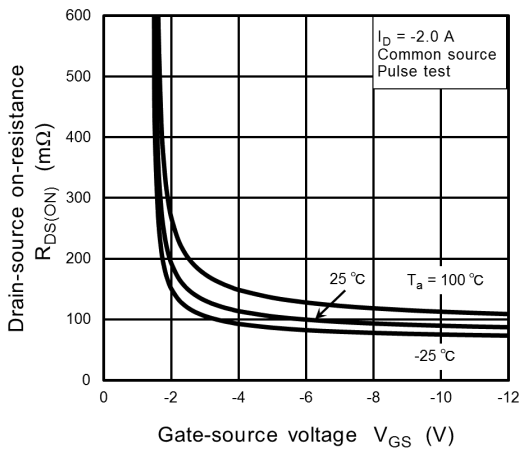


Fig. 7.3  $R_{DS(ON)} - V_{GS}$

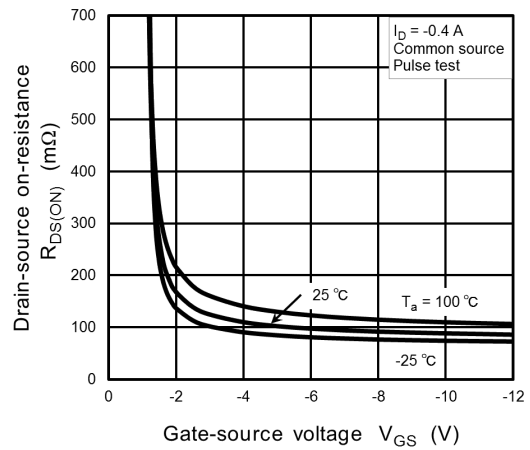


Fig. 7.4  $R_{DS(ON)} - V_{GS}$

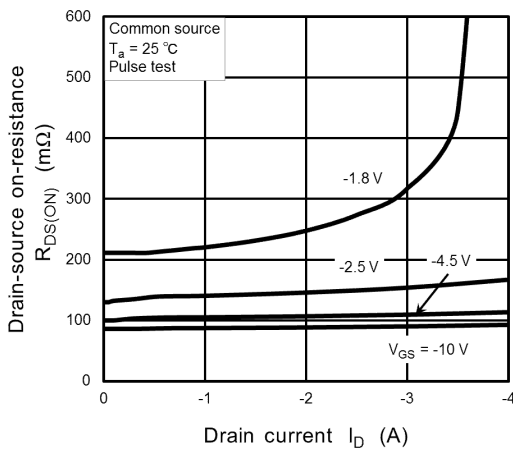


Fig. 7.5  $R_{DS(ON)} - I_D$

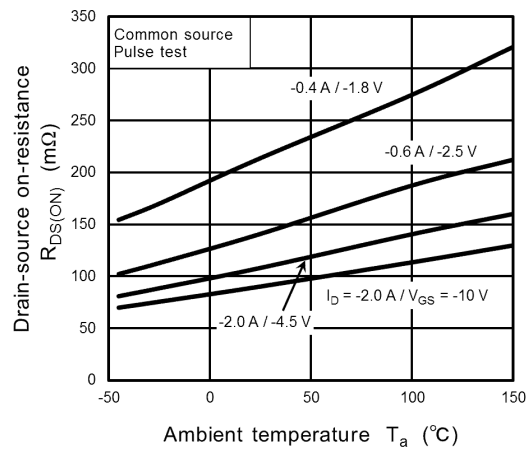
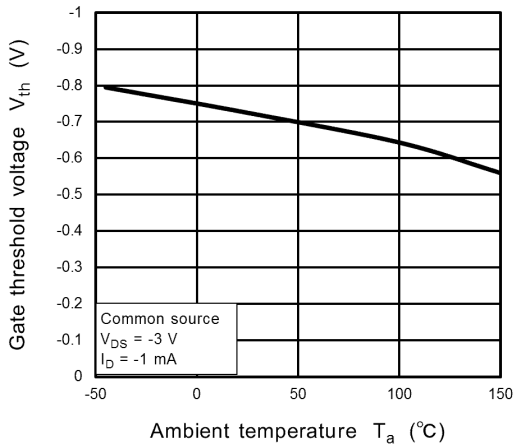
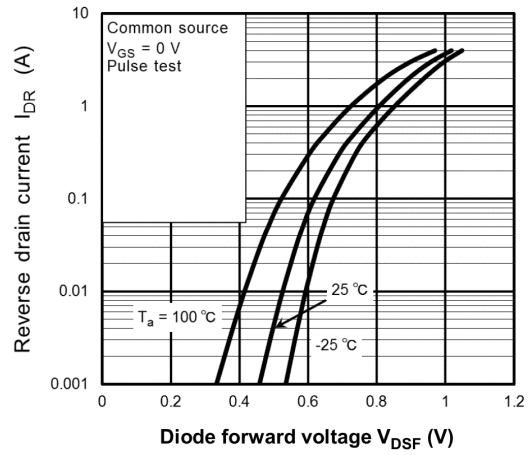


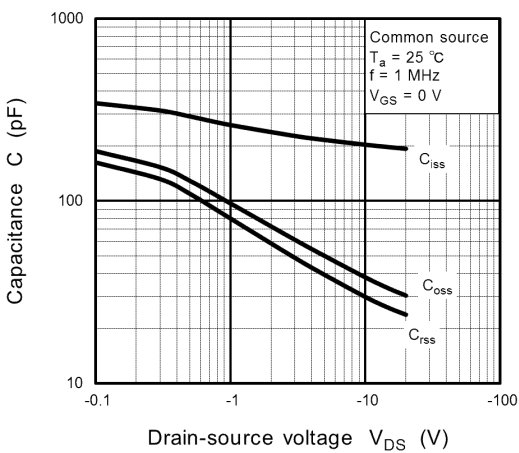
Fig. 7.6  $R_{DS(ON)} - T_a$



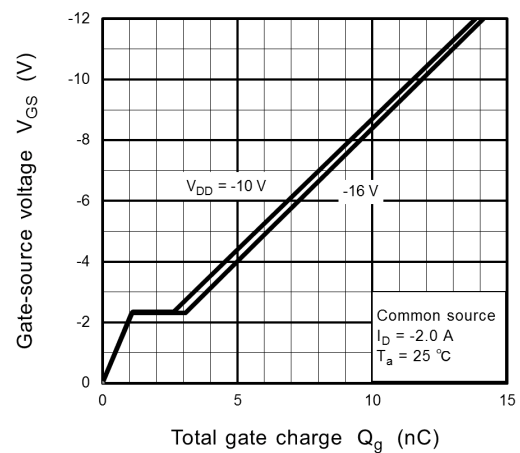
**Fig. 7.7  $V_{th} - T_a$**



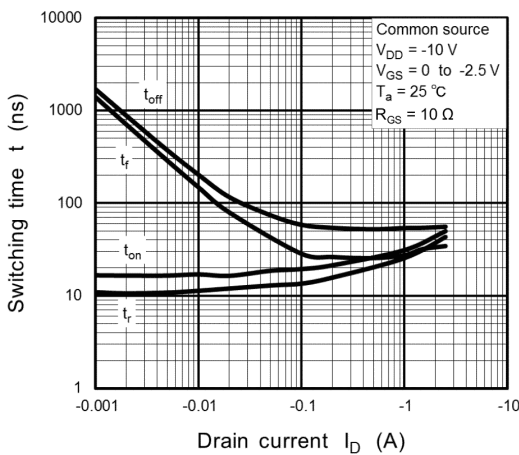
**Fig. 7.8  $I_{DR} - V_{DSF}$**



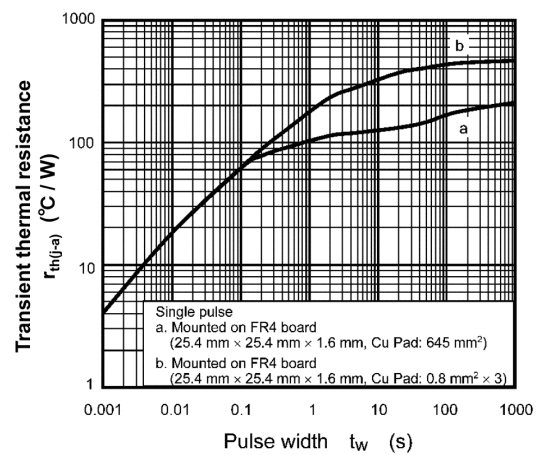
**Fig. 7.9  $C - V_{DS}$**



**Fig. 7.10 Dynamic Input Characteristics**



**Fig. 7.11  $t - I_D$**

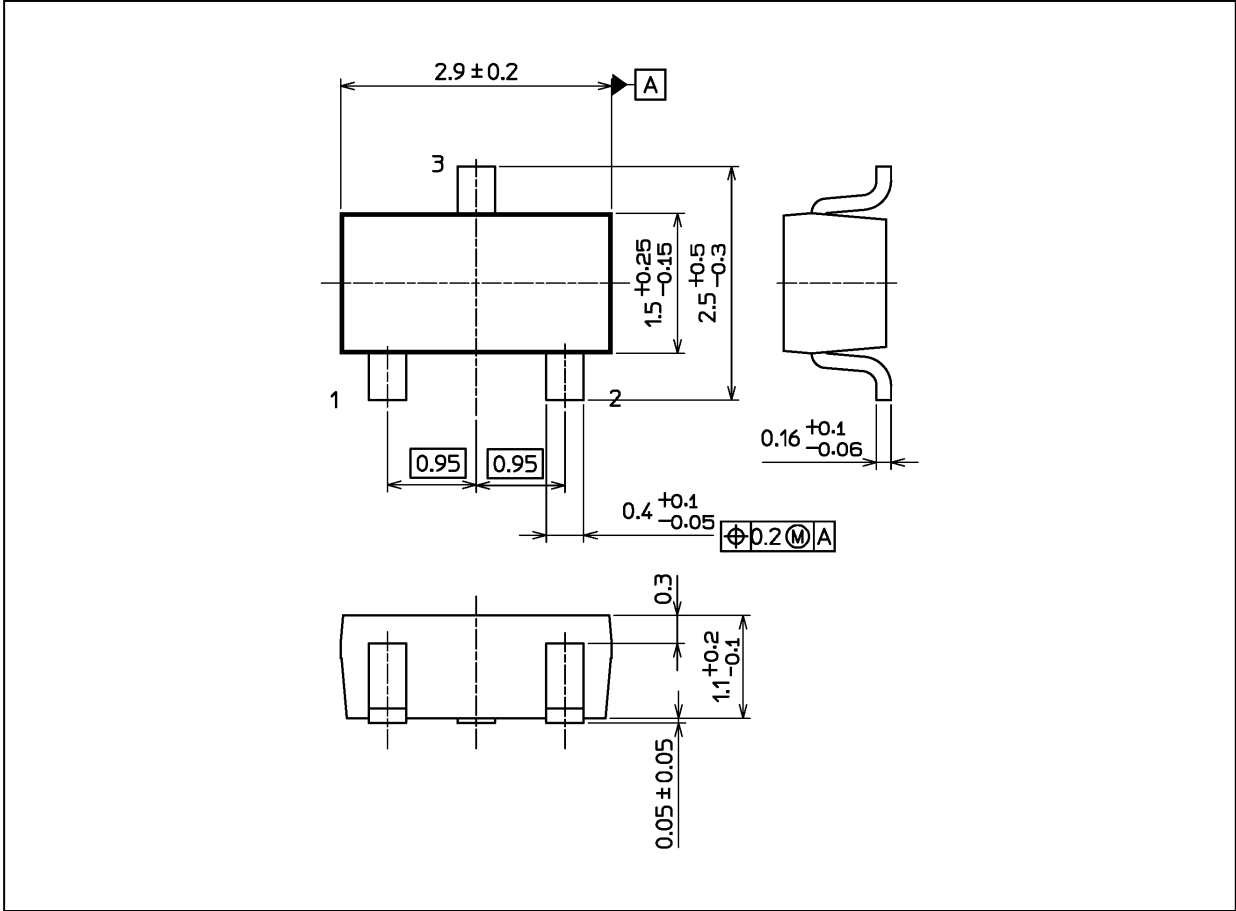


**Fig. 7.12  $r_{th(j-a)} - t_w$**

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

Package Dimensions

Unit: mm



Weight: 12 mg (typ.)

Package Name(s)
Nickname: S-Mini

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