

TOSHIBA Diode Silicon Epitaxial Planar Type

1SS337

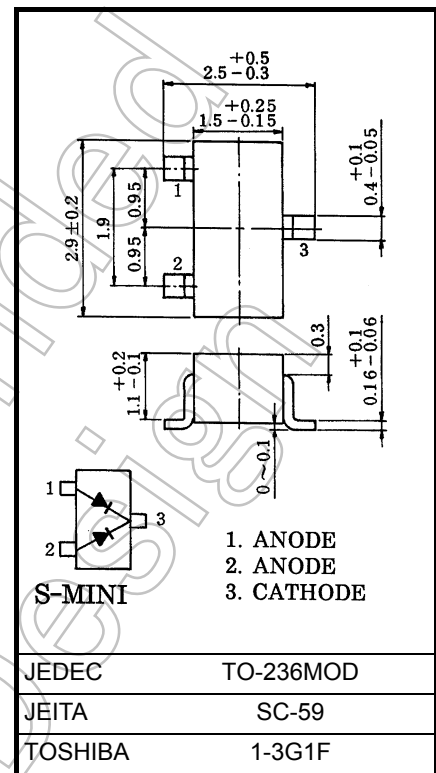
Ultra High-Speed Switching Applications

Unit: mm

- Small package: SC-59
- Low forward voltage: $V_F(3) = 0.88\text{ V}$ (typ.)
- Fast reverse recovery time: $t_{rr} = 6\text{ ns}$ (typ.)
- Small total capacitance: $C_T = 1.6\text{ pF}$ (typ.)

Absolute Maximum Ratings ($T_a = 25^\circ\text{C}$)

Characteristics	Symbol	Rating	Unit
Maximum (peak) reverse voltage	V_{RM}	85	V
Reverse voltage	V_R	80	V
Maximum (peak) forward current	I_{FM}	600 *	mA
Average forward current	I_O	200 *	mA
Surge current (10 ms)	I_{FSM}	6 *	A
Power dissipation	P	150	mW
Junction temperature	T_j	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to 150	$^\circ\text{C}$



Weight: 0.012 g (typ.)

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions", "Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

*: Unit rating. Total rating = unit rating × 1.5

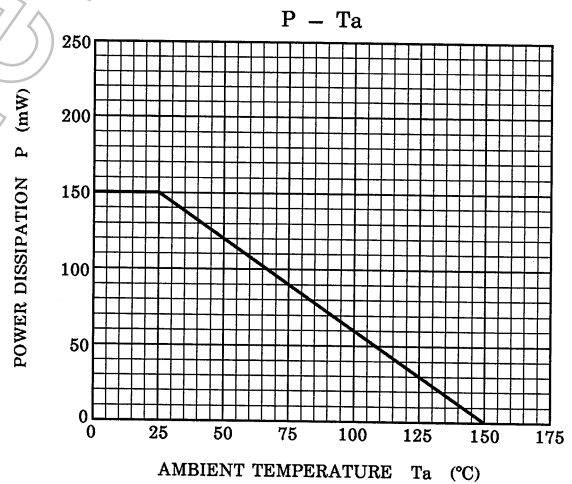
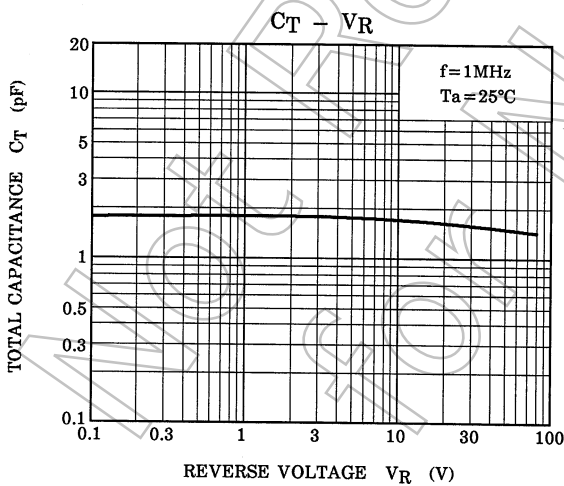
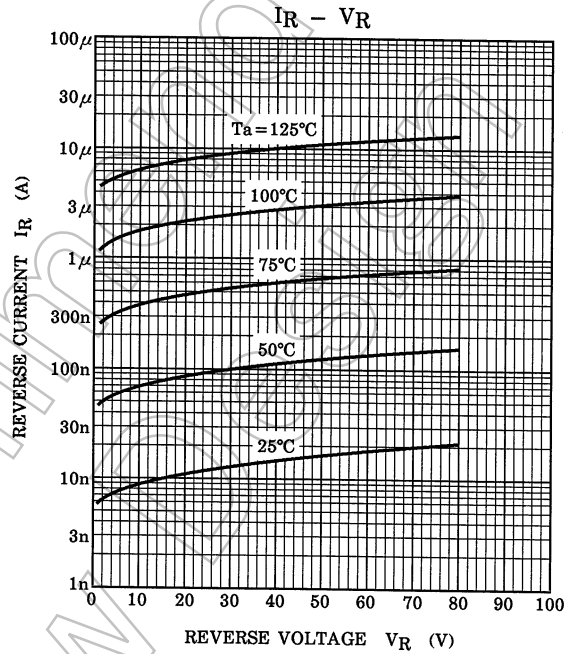
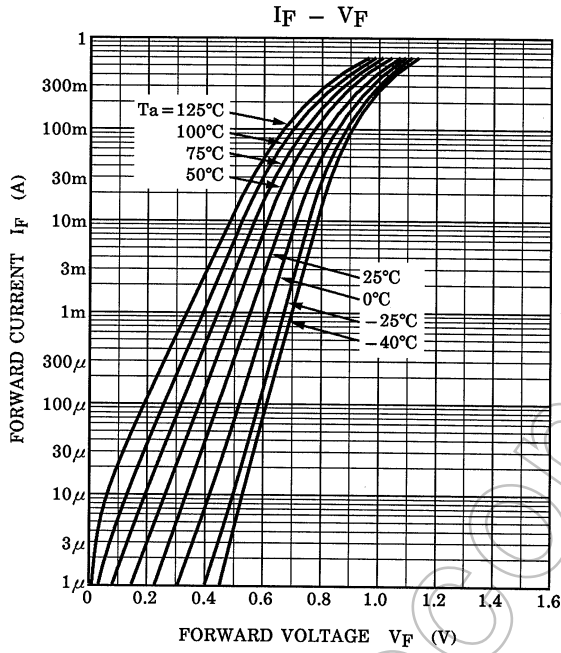
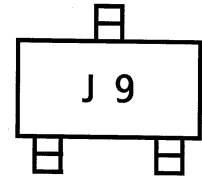
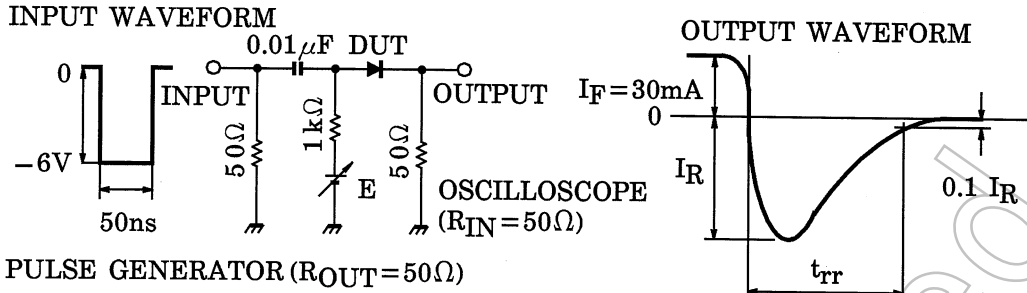
Electrical Characteristics ($T_a = 25^\circ\text{C}$)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Forward voltage	$V_F(1)$	—	$I_F = 10\text{ mA}$	—	0.66	—	V
	$V_F(2)$	—	$I_F = 100\text{ mA}$	—	0.80	—	
	$V_F(3)$	—	$I_F = 200\text{ mA}$	—	0.88	1.20	
Reverse current	$I_R(1)$	—	$V_R = 30\text{ V}$	—	—	0.25	μA
	$I_R(2)$	—	$V_R = 80\text{ V}$	—	—	0.50	
Total capacitance	C_T	—	$V_R = 0, f = 1\text{ MHz}$	—	1.6	—	pF
Reverse recovery time	t_{rr}	—	$I_F = 30\text{ mA}, \text{Fig.1}$	—	6	20	ns

Start of commercial production
1989-11

Fig.1 Reverse Recovery Time (t_{rr}) Test Circuit

Marking



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