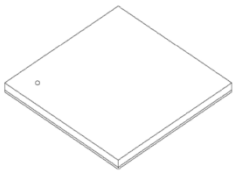
CMOS Digital Integrated Circuit Silicon Monolithic

TC358743XBG

Mobile Peripheral Devices



P-TFBGA64-0606-0.65-001
Weight: 76 mg (Typ.)

Overview

The HDMI®-RX to MIPI® CSI-2-TX is a bridge device that converts HDMI stream to MIPI CSI-2 TX.

The current and next generation Application Processors and Baseband chips have been designed without video streaming input port except CSI-2 for Camcorder input. Smart Phone Processors are being used in several applications that required Video Input

TC358743XBG takes in HDMI input and converts to CSI-2 that looks like a Camcorder input.

Features

- HDMI-RX Interface
  - ✧ HDMI 1.4
    - Video Formats Support (Up to 1080P @60fps)
      - ➢ RGB, YCbCr444: 24-bpp @60fps
      - ➢ YCbCr422 24-bpp @60fps
    - Audio Supports
      - ➢ Internal Audio PLL to track N/CTS value transmitted by the ACR packet.
    - 3D Support
    - Support HDCP (optional)
    - DDC Support
    - EDID Support
      - ➢ Release A, Revision 1 (Feb 9, 2000)
      - ➢ First 128 byte (EDID 1.3 structure)
      - ➢ First E-EDID Extension: 128 bytes of CEA Extension version 3 (specified in CEA-861-D)
      - ➢ Embedded 1K-byte SRAM (EDID_SRAM)
    - Maximum HDMI clock speed: 165 MHz
  - ✧ Does not support Audio Return Path and HDMI Ethernet Channels
- CSI-2 TX Interface
  - ✧ MIPI CSI-2 compliant (Version 1.01 Revision 0.04 – 2 April 2009)
  - ✧ Supports up to 1 Gbps per data lane
    - Video, Audio and InfoFrame data can be transmit over MIPI CSI-2
  - ✧ Supports up to 4 data lanes
- I^2C Slave Interface
  - ✧ Support for Normal-mode (100 kHz) and Fast-mode (400 kHz)
  - ✧ Support Ultra Fast-mode (2 MHz)
  - ✧ Configure all TC358743XBG internal registers
- Audio Output Interface

  Either I2S or TDM Audio interface available (pins are multiplexed)

  I2S Audio Interface
  - ✧ Single data lane for stereo data
  - ✧ Support Master Clock mode only
  - ✧ Support 16, 18, 20 or 24-bit data (depend on HDMI input stream)
  - ✧ Support Left or Right-justify with MSB first
  - ✧ Support 32 bit-wide time-slot only
  - ✧ Output Audio Oversampling clock (256fs)

  TDM (Time Division Multiplexed) Audio Interface
  - ✧ Fixed to 8 channels (depend on HDMI input stream)
  - ✧ Support 32 bit-wide time slot only
  - ✧ Support Master Clock mode only
  - ✧ Support 16, 18, 20 or 24-bit PCM audio data word (depend on HDMI input stream)
  - ✧ Output Audio Oversampling clock (256fs)
- InfraRed (IR)
  - ✧ Support NEC Infrared protocol.
- System
  - ✧ Internal core has two power domains (VDDC1 and VDDC2)
    - VDDC1 is always on power domain
    - VDDC2 can be shut-off during deep sleep mode
- Power supply inputs
  - ✧ Core and MIPI D-PHY: 1.2 V
  - ✧ I/O: 1.8V – 3.3 V
  - ✧ HDMI: 3.3 V
  - ✧ APLL: 3.3 V/2.5 V
- Power Consumption during typical operations
  - ✧ 720P: 0.48 W
  - ✧ 1080P @30fps: 0.48 W
  - ✧ 1080P @60fps: 0.54 W

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REFERENCES

1. MIPI D-PHY, “MIPI_D-PHY_specification_v01-00-00, May 14, 2009"
2. MIPI CSI-2, "MIPI Alliance Standard for Camera Serial Interface 2 (CSI-2) Version 1.01 Revision Nov 2010"
3. VESA Mobile Display Digital Interface Standard (Version 1.2, Type II)
4. I^2C bus specification, version 2.1, January 2000, Philips Semiconductor

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TC358743XBG System Overview block diagram is shown below.

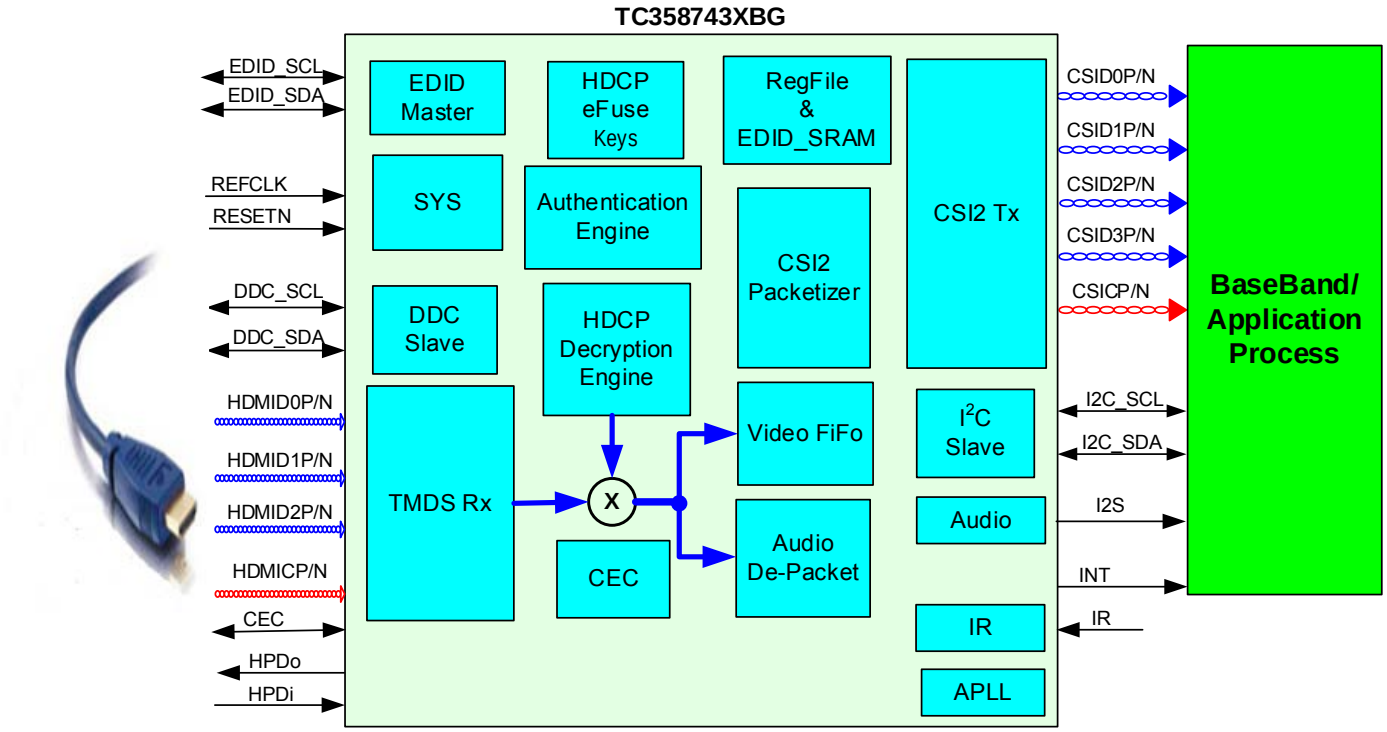

Figure 1.1 TC358743XBG System Overview

2. Features

Below are the main features supported by TC358743XBG.

- HDMI-RX Interface
  - ✧ HDMI 1.4
    - Video Formats Support (Up to 1080P @60fps)
      - ➢ RGB, YCbCr444: 24-bpp @60fps
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    - Audio Supports
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    - EDID Support
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  - ✧ Support for Normal-mode (100 kHz) and Fast-mode (400 kHz)
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  - ✧ Configure all TC358743XBG internal registers

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  Either I2S or TDM Audio interface available (pins are multiplexed)

  I2S Audio Interface
  - ✧ Single data lane for stereo data
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  - ✧ Support NEC Infrared protocol.

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  - ✧ Internal core has two power domains (VDDC1 and VDDC2)
    - VDDC1 is always on power domain
    - VDDC2 can be shut-off during deep sleep mode

- Power supply inputs
  - ✧ Core and MIPI D-PHY: 1.2 V
  - ✧ I/O: 1.8 V – 3.3 V
  - ✧ HDMI: 3.3 V
  - ✧ APLL: 3.3 V/2.5 V

- Power Consumption during typical operations
  - ✧ 720P: 0.48 W
  - ✧ 1080P @30fps: 0.48 W
  - ✧ 1080P @60fps: 0.54 W

Table 2.1 TC358743XBG Power Consumption during typical operations

		VDDC1	VDDC2	VDDIO1	VDDIO2	VDDMIPI	AVDD33	AVDD12	AVDD25	Total Power	Unit
		1.2	1.2	3.3	1.8	1.2	3.3	1.2	2.5		
720P @60Frames	Current (A)	0.0472		0	0.0009	0.0178	0.0879	0.0656	0.0128	480.47	mW
	Power (W)	0.05664		0	0.0017	0.0214	0.2901	0.0787	0.032		
1080P @60Frames	Current (A)	0.0766		0	0.0009	0.0228	0.0881	0.0829	0.0128	543.19	mW
	Power (W)	0.09192		0	0.0017	0.0274	0.2907	0.0995	0.032		
Sleep 0x0002 = 0x0001	Current (μA)	0.91		0.002	0.0430	0.0490	32.3700	0.3200	0.2	108.94	μW
	Power (μW)	1.092		0.0066	0.0774	0.0588	106.8210	0.3840	0.5		

Note:

- Attention about ESD. This product is weak against ESD. Please handle it carefully.
- TC358743XBG does not perform YCbCr ↔ YUV conversion. In this document they are used interchangeably.
- TC358743XBG is provided with and without HDCP keys. They are identified with package mark shown below.
  - Figure 2.1, indicates HDCP keys are burned into the device.
  - Figure 2.2, shows HDCP key is not included, please ignore all the registers field related to HDCP functionality.

Figure 2.1 Package Marking with HDCP Key, HAL is appended to lot code

Figure 2.2 Package Marking without HDCP Key, HNL is appended to lot code

3. External Pins

TC358743XBG resides in BGA64 pin packages. The following table gives the signals of TC358743XBG and their function.

Table 3.1 TC358743XBG Functional Signal List

Group	Pin Name	I/O	Init (O)	Type	Function	Voltage Supply	Note
System: Reset & Clock (4)	RESETN	I	-	Sch	System reset input, active low	VDDIO2	1.8V -3.3V
	REFCLK	I	-	N	Reference clock input (27/26 MHz or 42 MHz)	VDDIO2	1.8V -3.3V
	TEST	I	-	N	TEST mode select 0: Normal mode 1: Test mode	VDDIO2	1.8V -3.3V
	INT	O	L	N	Interrupt Output signal – active high (Level)	VDDIO2	1.8V -3.3V
CSI-2 TX (10)	CSICP	-	H	MIPI-PHY	MIPI-CSI-2 clock positive	VDD_MIPI	1.2V
	CSICN	-	H	MIPI-PHY	MIPI-CSI-2 clock negative	VDD_MIPI	1.2V
	CSID0P	-	H	MIPI-PHY	MIPI-CSI-2 Data 0 positive	VDD_MIPI	1.2V
	CSID0N	-	H	MIPI-PHY	MIPI-CSI-2 Data 0 negative	VDD_MIPI	1.2V
	CSID1P	-	H	MIPI-PHY	MIPI-CSI-2 Data 1 positive	VDD_MIPI	1.2V
	CSID1N	-	H	MIPI-PHY	MIPI-CSI-2 Data 1 negative	VDD_MIPI	1.2V
	CSID2P	-	H	MIPI-PHY	MIPI-CSI-2 Data 2 positive	VDD_MIPI	1.2V
	CSID2N	-	H	MIPI-PHY	MIPI-CSI-2 Data 2 negative	VDD_MIPI	1.2V
	CSID3P	-	H	MIPI-PHY	MIPI-CSI-2 Data 3 positive	VDD_MIPI	1.2V
	CSID3N	-	H	MIPI-PHY	MIPI-CSI-2 Data 3 negative	VDD_MIPI	1.2V
HDMI-RX (8)	HDMICP	-	-	HDMI-PHY	HDMI Clock channel positive	AVDD33	3.3V
	HDMICN	-	-	HDMI-PHY	HDMI Clock channel negative	AVDD33	3.3V
	HDMID0P	-	-	HDMI-PHY	HDMI Data 0 channel positive	AVDD33	3.3V
	HDMID0N	-	-	HDMI-PHY	HDMI Data 0 channel negative	AVDD33	3.3V
	HDMID1P	-	-	HDMI-PHY	HDMI Data 1 channel positive	AVDD33	3.3V
	HDMID1N	-	-	HDMI-PHY	HDMI Data 1 channel negative	AVDD33	3.3V
	HDMID2P	-	-	HDMI-PHY	HDMI Data 2 channel positive	AVDD33	3.3V
	HDMID2N	-	-	HDMI-PHY	HDMI Data 2 channel negative	AVDD33	3.3V
DDC (2)	DDC_SCL	IO	-	N (Note2)	DDC Slave Clock	VDDIO1	3.3V (Note1)
	DDC_SDA	IO	-	N (Note2)	DDC Slave data	VDDIO1	3.3V (Note1)
EDID (2)	EDID_SCL	IO	-	N (Note2)	EDID Master Clock	VDDIO2	1.8V -3.3V
	EDID_SDA	IO	-	N (Note2)	EDID Master Data	VDDIO2	1.8V -3.3V
CEC	CEC	IO	-	N (Note2)	CEC signal	VDDIO1	3.3V
HPD (2)	HPDI	I	-	N	Hot Plug Detect Input	VDDIO1	3.3V (Note1)
	HPDO	O	L	N	Hot Plug Detect Output	VDDIO1	3.3V
Audio (4)	A_SCK	O	L	N	I2S/TDM Bit Clock signal	VDDIO2	1.8V -3.3V
	A_WFS	O	L	N	I2S Word Clock or TDM Frame Sync signal	VDDIO2	1.8V -3.3V
	A_SD	O	L	N	I2S/TDM data signal	VDDIO2	1.8V -3.3V
	A_OSCK	O	L	N	Audio Oversampling Clock	VDDIO2	1.8V -3.3V
IR	IR	I	-	Sch	Infrared signal	VDDIO2	1.8V -3.3V
I2C (2)	I2C_SCL	IO	-	N (Note2)	I^2C serial clock	VDDIO2	1.8V -3.3V
	I2C_SDA	IO	-	N (Note2)	I^2C serial data	VDDIO2	1.8V -3.3V
APLL (4)	BIASDA	O	L	-	BIAS signal Connect to AVSS through 0.1µF when not used	-	-
	DAOUT	O	H	-	Audio PLL clock Reference Output clock Please leave open when not used	-	-
	PCKIN	I	-	-	Audio PLL Reference Input clock Connect to AVSS through 0.1µF when not used	-	-
	PFIL	O	L	-	Audio PLL Low Pass Filter signal Connect to AVSS through 0.1µF when not used	-	-
POWER (12)	VDDC1, VDDC2	-	-	-	VDD for Internal Core (3)	-	1.2V
	VDDIO1	-	-	-	VDDIO1 IO power supply (1)	-	3.3V
	VDDIO2	-	-	-	VDDIO2 IO power supply (1)	-	1.8V -3.3V
	VDD_MIPI	-	-	-	VDD for the MIPI CSI-2 (2)	-	1.2V
	AVDD12	-	-	-	HDMI Phy 1.2 V power supply (2)	-	1.2V
	AVDD33	-	-	-	HDMI Phy 3.3 V power supply (2)	-	3.3V
	AVDD25	-	-	-	APLL 2.5 V power supply (1)	-	2.5V
Ground (10)	VSS	-	-	-	Ground	-	-

Group	Pin Name	I/O	Init (O)	Type	Function	Voltage Supply	Note
Misc (2)	REXT	-	-	-	External Reference Resistor, Please connect to AVDD33 with a 2 kΩ resistor (± 1%)	-	-
	VPGM	-	-	-	eFuse program power supply, please tie to ground	-	-

Total 64 pins

Note1: These IO are 5 V tolerant.
Note2: Bi-directional IO with Schmitt triggered input.

Buffer Type Abbreviation:

N: Normal IO
N_{PD}: Normal IO with weak Internal Pull-Down
N_{PU}: Normal IO with weak Internal Pull-Up
FS-SOD: Failed Safe Pseudo open-drain output, Schmitt input
FS: Failed Safe IO
Sch: Schmitt input buffer
MIPI-PHY: front-end analog IO for CSI-2
HDMI-PHY: front-end analog IO for HDMI

3.1. TC358743XBG BGA64 Pin Count Summary

Table 3.2 BGA64 Pin Count Summary

Group Name	Pin Count
System	4
CSI-2 TX	10
HDMI-RX	8
DDC	2
EDID	2
CEC	1
HPD	2
Audio	4
IR	1
I2C	2
APLL	4
POWER	12
Ground	10
Misc	2
TOTAL	**64**

3.2. Pin Layout

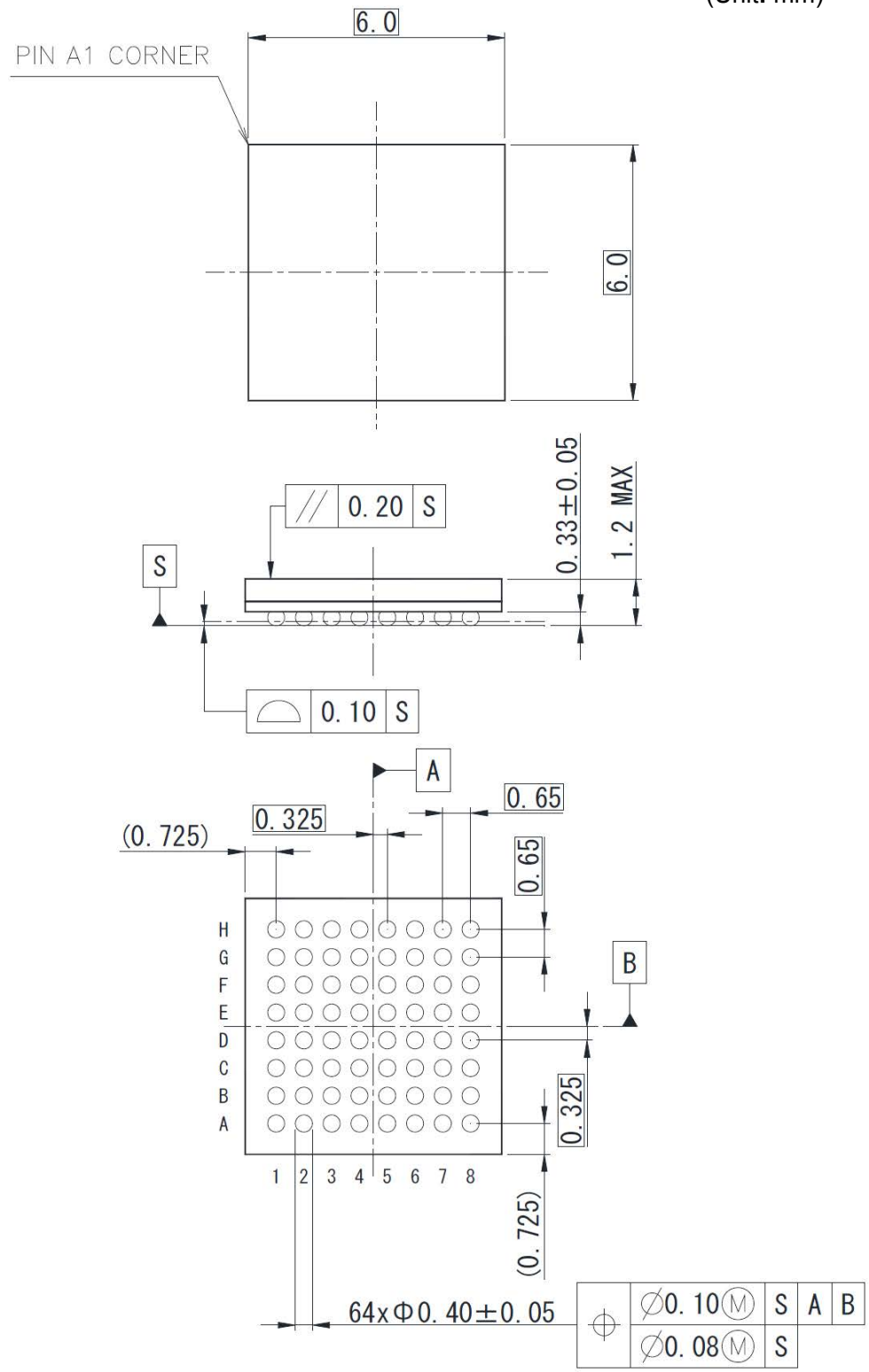
A1 REXT	A2 VSS	A3 VPGM	A4 BIASDA	A5 DAOUT	A6 PFIL	A7 CSID3N	A8 CSID3P
B1 AVDD33	B2 AVDD12	B3 INT	B4 IR	B5 AVDD25	B6 PCKIN	B7 CSID2N	B8 CSID2P
C1 HDMICP	C2 HDMICN	C3 VDDC2	C4 VSS	C5 VSS	C6 VDD_MIPI	C7 CSICN	C8 CSICP
D1 HDMID0P	D2 HDMID0N	D3 AVDD12	D4 VSS	D5 VSS	D6 VSS	D7 CSID1N	D8 CSID1P
E1 HDMID1P	E2 HDMID1N	E3 VSS	E4 VSS	E5 TEST	E6 VSS	E7 CSID0N	E8 CSID0P
F1 HDMID2P	F2 HDMID2N	F3 AVDD33	F4 VDDIO1	F5 VDDC2	F6 VDD_MIPI	F7 A_SCK	F8 A_SD
G1 CEC	G2 VDDC1	G3 DDC_SDA	G4 I2C_SDA	G5 RESETN	G6 EDID_SDA	G7 A_WFS	G8 A_OSCK
H1 HPDO	H2 HPDI	H3 DDC_SCL	H4 I2C_SCL	H5 REFCLK	H6 EDID_SCL	H7 VDDIO2	H8 VSS

Figure 3.1 TC358743XBG 64-Pin Layout (Top View)

4. Package

The packages for TC358743XBG are described in the figures below.

P-TFBGA64-0606-0.65-001 (Unit: mm)



Weight: 76 mg (Typ.)

Figure 4.1 TC358743XBG package (64 pins)

Table 4.1 Mechanical Dimension

Dimension	Min	Typ.	Max
Solder ball pitch	-	0.65 mm	-
Package dimension	-	6.0 × 6.0 mm^2	-
Package height	-	-	1.2 mm

5. Electrical Characteristics

5.1. Absolute Maximum Ratings

VSS = 0 V reference

Parameter	Symbol	Rating	Unit
Supply voltage (1.8 V - Digital IO)	VDDIO	-0.3 to +3.9	V
Supply voltage (1.2 V – Digital Core)	VDDC	-0.3 to +1.8	V
Supply voltage (1.2 V – MIPI CSI PHY)	VDD_MIPI	-0.3 to +1.8	V
Supply voltage (3.3 V – HDMIRX Phy)	AVDD33	-0.3 to +3.9	V
Supply voltage (1.2 V – HDMIRX Phy)	AVDD12	-0.3 to +1.8	V
Supply voltage (2.5 V – APLL)	AVDD25	-0.3 to +2.75	V
Input voltage (CSI IO)	V_{IN_CSI}	-0.3 to VDD_MIPI + 0.3	V
Output voltage (CSI IO)	V_{OUT_CSI}	-0.3 to VDD_MIPI + 0.3	V
Input voltage (Digital IO)	V_{IN_IO}	-0.3 to VDDIO + 0.3	V
Output voltage (Digital IO)	V_{OUT_IO}	-0.3 to VDDIO + 0.3	V
Output voltage (APLL)	V_{OUT_APLL}	-0.3 to AVDD25 + 0.3	V
Junction temperature	Tj	125	°C
Storage temperature	Tstg	-40 to +125	°C

5.2. Operating Condition

VSS = 0 V reference

Parameter	Symbol	Min	Typ.	Max	Unit
Supply voltage (1.8/3.3 V – Digital IO)	VDDIO2	1.65	1.8	3.6	V
Supply voltage (3.3 V – HDMI Digital IO)	VDDIO1	3.0	3.3	3.6	V
Supply voltage (1.2 V – Digital Core)	VDDC	1.1	1.2	1.3	V
Supply voltage (1.2 V – MIPI CSI PHY)	VDD_MIPI	1.1	1.2	1.3	V
Supply voltage (2.5 V – APLL)	AVDD25	2.25	2.5	2.75	V
Operating temperature (ambient temperature with voltage applied)	Ta	-30	25	70	°C
Supply Noise Voltage	VSN	-	-	0.1	Vpp
Supply voltage (3.3 V – HDMIRX PHY)	AVDD33	3.135	3.3	3.465	V
Supply Noise Voltage for AVDD33	VSN33	-	-	0.08	Vpp
Supply voltage (1.2 V – HDMIRX PHY)	AVDD12	1.15	1.2	1.25	V
Supply Noise Voltage for AVDD12	VSN12	-	-	0.04	Vpp

5.3. DC Electrical Specification

Parameter	Symbol	Min	Typ.	Max	Unit
Input voltage, High level input Note1	V_{IH}	0.7 x VDDIO	-	VDDIO	V
Input voltage, Low level input Note1	V_{IL}	0	-	0.3 x VDDIO	V
Input voltage High level CMOS Schmitt Trigger Note1,2	V_{IHS}	0.7 x VDDIO	-	VDDIO	V
Input voltage Low level CMOS Schmitt Trigger Note1,2	V_{ILS}	0	-	0.3 x VDDIO	V
Output voltage High level Note1, Note2	V_{OH}	0.8 x VDDIO	-	VDDIO	V
Output voltage Low level Note1, Note2	V_{OL}	0	-	0.2 x VDDIO	V
Input leak current, High level (Condition: V_{IN} = +VDDIO, VDDIO = 3.6 V)	I_{ILH1} (Note4)	-10	-	10	µA
Input leak current, Low level (Condition: V_{IN} = 0 V, VDDIO = 3.6 V)	I_{ILL1} (Note5)	-10	-	10	µA

Note1: Each power source is operating within recommended operation condition.

Note2: Current output value is specified to each IO buffer individually. Output voltage changes with output current value.

Note4: Normal pin or Pull-up IO pin applied VDDIO supply voltage to Vin (input voltage)

Note5: Normal pin applied VSS (0 V) to Vin (input voltage)

6. Revision History

Table 6.1 Revision History

Revision	Date	Description
0.582	2014-05-16	Newly released
0.621	2015-12-18	Typo Init(O) DAOUT pin in External Pins
0.622	2016-04-01	Package's weight is rounding up digits after the decimal point to form an integer.
1.0	2017-10-26	Added comment to HDCP in Features. Changed header, footer and the last page. Changed corporate name.

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