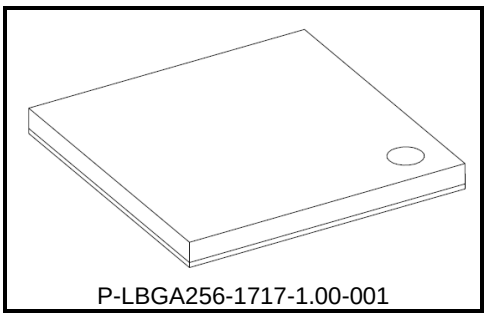
CMOS Digital Integrated Circuit Silicon Monolithic

TC90197XBG

Dual screen signal processing IC for small panel

1. Description

TC90197XBG is a highly integrated, high performance picture processor for small LCD panel (W-VGA). It adapts analog component, composite Video, digital RGB, digital YUV signal format, and it has a video output of digital RGB.
In addition timing control signal output for W-VGA panel.



P-LBGA256-1717-1.00-001

Weight: 0.63 g (typ.)

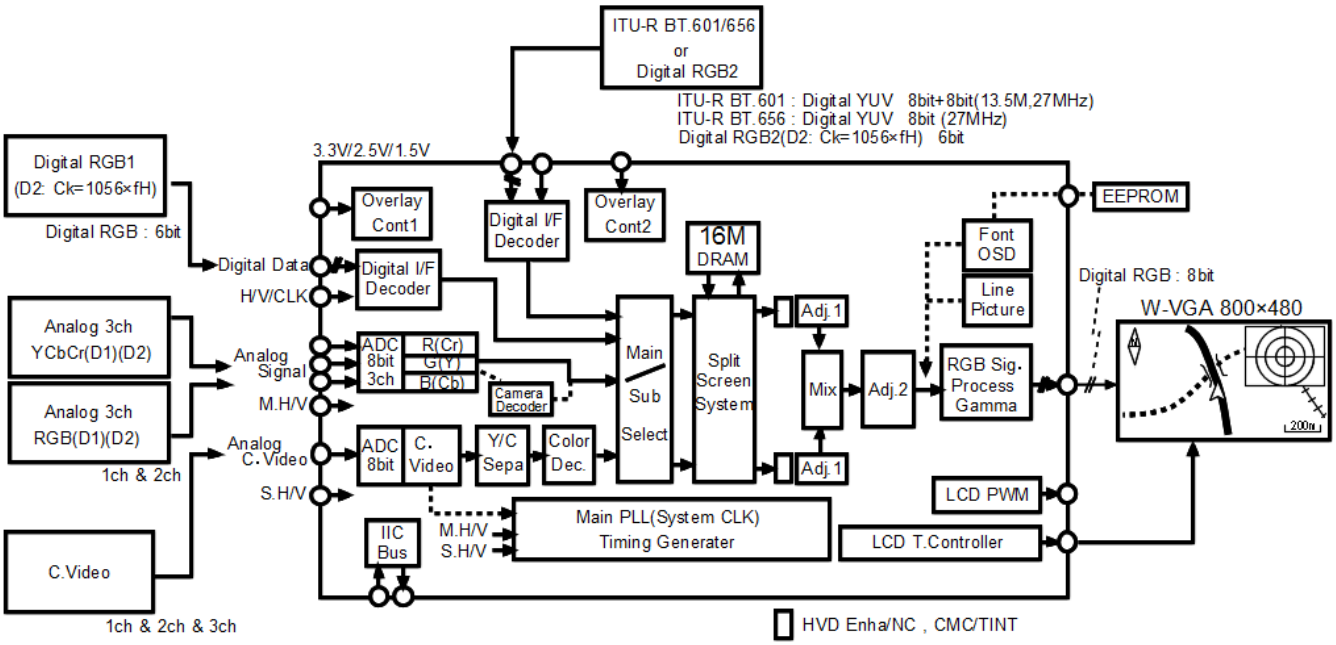
2. Applications

Car navigation / Car entertainment

3. Features

- **Input interface**
  - 2ch Component video signal input (selectable RGB and YCbCr, 525i / 625i / 525p / 625p)
    - 8bit ADC 3ch
    - Gch IN input t pin **:** Extra car camera mode pin (for NTSC / PAL color decoder)
  - Composite video input with 3ch selector (NTSC / PAL / SECAM / PAL-M / PAL-N / PAL60 / 443NTSC)
    - 8bit ADC 1ch
  - Digital input interface 1 (RGB (525p / 625p)**:** 6bit × 3ch)
  - Digital input interface 2 (Selectable RGB (525p / 625p)**:** 6bit × 3ch and YUV**:** ITU-R BT.601 (525i / 625i / 525p / 625p) or ITU-R BT.656 (525i / 625i))
- **Output interface**
  - Digital RGB Output (8bit × 3ch)
  - LCD Timing Control Output for WVGA panel (W-VGA**:** 800 dot × 480 Line)
  - LED Back Light Control Output (Dimmer (PWM))
- **Key Features**
  - 3 line Digital comb filter (NTSC / PAL)
  - Color decoder for Multi-color system (NTSC / PAL / SECAM / PAL-M / PAL-N / PAL60 / 443NTSC)
  - Digital PLL (for Clock Generator)
  - Scaling function (built in 16 Mbit DRAM)
  - Super impose function
    - Overlay function (Timing pulse control / Chroma Key)
    - Line drawing OSD
    - Built in SRAM font and fixed characters font OSD
  - YCbCr Picture quality control functions
    - Y**:** HVD Enhancer, H/V Enhancer, LTI, Noise canceller, Contrast, Brightness
    - C**:** Color management, Skin color correction, CTI, Noise canceller, Gain control, Cb/Cr offset
  - RGB Picture quality control functions (RGB Contrast , Brightness)
  - Y-Dynamic gamma
  - Picture gamma (8 inflection points setting)
  - RGB static gamma(8 inflection points setting)
  - I^2C Bus control (Fast mode)
  - EEPROM interface (64 kbit / 128 kbit / 256 kbit)
- **Power Supply**
  - 1.5 V (for logic circuit and DRAM) / 2.5 V (for analog circuit and DRAM) / 3.3 V (for I/O block)

4. Functional Block Diagram



5. Pin Layout (top view)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	DG2 RIN4	DG2 RIN2	DG2 RIN0	D-B0 Out	D-B2 Out	D-B4 Out	D-B6 Out	D-G0 Out	D-G2 Out	D-G4 Out	D-G6 Out	D-R0 Out	D-R2 Out	D-R4 Out	D-R6 Out	CPH Out	A
B	DG2 RIN5	DG2 RIN3	DG2 RIN1	D-B1 Out	D-B3 Out	D-B5 Out	D-B7 Out	D-G1 Out	D-G3 Out	D-G5 Out	D-G7 Out	D-R1 Out	D-R3 Out	D-R5 Out	D-R7 Out	STH Out	B
C	DG2 GIN0	DG2 GIN1	1.5V DRAM	Test Pin-A	1.5V DRAM	VDD-IO 3.3V	VSS-D	VSS-D	VDD-D 1.5V	VDD-D 1.5V	VDD-IO 3.3V	VSS-D	VSS-D	Dimmer	Enable Out	Load Out	C
D	DG2 GIN2	DG2 GIN3	2.5V DRAM	Drect Access	2.5V DRAM	VDD-IO 3.3V	VSS-D	VSS-D	VDD-D 1.5V	VDD-D 1.5V	VDD-IO 3.3V	VSS-D	VSS-D	Monitor Out2	STV2 Out	GOE Out	D
E	DG2 GIN4	DG2 GIN5	VSS-D	I2C Salve Sel	VSS-D	VDD-IO 3.3V	VSS-D	VDD-D 1.5V	VDD-D 1.5V	VDD-IO 3.3V	VDD-IO 3.3V	VSS-D	VSS-D	VSS-D	Hcom (Dot REV)	CPV Out	E
F	DG2 BIN0	DG2 BIN1	VSS-D	VSS-D	VDD-IO 3.3V	VDD-IO 3.3V	VSS-D	VSS-D	VDD-IO 3.3V	VDD-IO 3.3V	VSS-D	VSS-D	MBIST	Vcom2 Out	U/D Out	STV1 Out	F
G	DG2 BIN2	DG2 BIN3	1.5V DRAM	VSS-D	VSS-D	VSS-D	VSS-D	VSS-D	VSS-D	VSS-D	(DRAM) MB	Test mode-4 SW	Test mode-3 SW	V-Load	Vcom1 Out	Monitor Out1	G
H	DG2 BIN4	DG2 BIN5	2.5V DRAM	VDD-D 1.5V	VDD-D 1.5V	VDD-D 1.5V	VSS-D	VSS-D	VSS-D	VSS-D	Test mode-2 SW	Test mode-1 SW	VSS_MA DC	2.5V MADC	MADC VREFB	MADC BIAS	H
J	DG2 Clock IN	DG2 H IN	VSS-D	VDD-D 1.5V	VDD-D 1.5V	VDD-D 1.5V	VSS-D	VSS-D	VSS-D	VSS-D	VSS-D	VSS-D	VSS_MA DC	2.5V MADC	G/Y IN2	B/Cb IN2	J
K	DG2 V IN	DG2 OVL Cont IN2	VSS-D	VDD-IO 3.3V	VDD-IO 3.3V	VDD-IO 3.3V	VSS-D	VSS-D	VSS-D	VDD-D 1.5V	VDD-D 1.5V	VSS-D	VSS_MA DC	2.5V MADC	B/Cb IN1	R/Cr IN2	K
L	EE-P Ck Out	I2C-Bus Clock IN	1.5V DRAM	VDD-IO 3.3V	VDD-IO 3.3V	VSS-D	VDD-D 1.5V	VDD-D 1.5V	VDD-D 1.5V	VDD-D 1.5V	VDD-D 1.5V	VSS-D	VSS_MA DC	2.5V MADC	R/Cr IN1	G/Y IN1	L
M	EE-P DA	I2C-Bus DA/ACK	Panel Select IN	VDD-IO 3.3V	VSS-D	VDD-D 1.5V	VDD-D 1.5V	VDD-IO 3.3V	VDD-IO 3.3V	VSS-D	VDD-D 1.5V	VSS-D	VSS SADC	2.5V SADC/ Logic	SADC VREFB	MADC VREFT	M
N	OVL Cont IN1	EE-P Slave Sel	Test Scan	VSS-D	VSS-D	VDD-D 1.5V	VDD-D 1.5V	VDD-IO 3.3V	VDD-IO 3.3V	VSS-D	VSS-D	VSS-D	VSS-PLL1/2	VSS DSEP/DA C	CVBS IN3	CVBS IN2	N
P	Reset IN	Display Mute IN	VSS-D	VSS-D	VSS-D	VDD-D 1.5V	VDD-D 1.5V	VDD-IO 3.3V	VDD-IO 3.3V	VSS-D	VSS-D	2.5V XTAL1/2	2.5V PLL	2.5V DSEP/ DAC	CVBS IN1	SADC BIAS	P
R	CVBS3 Force	DG1 V IN	DG1 RIN4	DG1 RIN2	DG1 RIN0	DG1 GIN4	DG1 GIN2	DG1 GIN0	DG1 BIN4	DG1 BIN2	DG1 BIN0	XTAL OUT	CVBS Sync IN	DAC OUT	A-3ch H/C IN1	SADC VREFT	R
T	DG1 H. IN	DG1 Clock IN	DG1 RIN5	DG1 RIN3	DG1 RIN1	DG1 GIN5	DG1 GIN3	DG1 GIN1	DG1 BIN5	DG1 BIN3	DG1 BIN1	XTAL IN	PLL FILTER	PLL IN	DAC BIAS	A-3ch V/C IN2	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

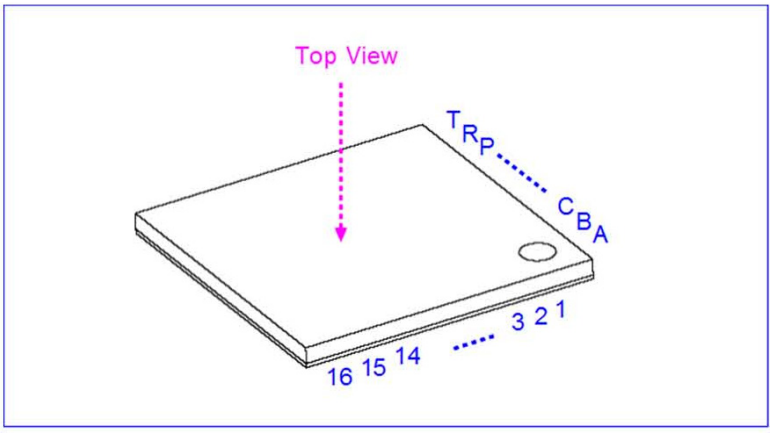


Figure 5-1 BGA Package Pin Layout

6. Pin Description

Table 6-1 Pin description

Chip Pad No.	Package pin No.	Pin name	Function	I/O	Voltage [V]	When not in use.
1	VSS-D		GND	GND	GND	—
2	—	NC	Not connected	—	—	—
3	VDD-D		1.5 V Power Supply for Logic circuit.	VDD	1.5	—
4	—	NC	Not connected	—	—	—
5	VDD1.5-DRAM		1.5 V Power Supply for internal DRAM.	VDD	1.5	—
6	—	NC	Not connected.	—	—	—
7	VSS-D		DRAM GND	GND	GND	—
8	—	NC	Not connected	—	—	—
9	VDD2.5-DRAM		2.5 V Power Supply for internal DRAM.	VDD	2.5	—
10	—	NC	Not connected	—	—	—
11	VDD-IO	VDD-IO	3.3 V Power Supply for I/O.	VDD	3.3	—
12	A3	DG2 RIN0	Digital RGB.2 R-0bit (LSB) or Digital YUV ITU-R BT.601 Y-0bit (LSB) / ITU-R BT.656 YUV-0bit (LSB) input.	IN	0 / 3.3	(*1)
13	B3	DG2 RIN1	Digital RGB.2 R-1bit or Digital YUV ITU-R BT.601 Y-1bit / ITU-R BT.656 YUV-1bit input.	IN	0 / 3.3	(*1)
14	A2	DG2 RIN2	Digital RGB.2 R-2bit or Digital YUV ITU-R BT.601 Y-2bit / ITU-R BT.656 YUV-2bit input.	IN	0 / 3.3	(*1)
15	B2	DG2 RIN3	Digital RGB.2 R-3bit or Digital YUV ITU-R BT.601 Y-3bit / ITU-R BT.656 YUV-3bit input.	IN	0 / 3.3	(*1)
16	VDD-D		1.5V Power Supply for Logic circuit.	VDD	1.5	—
17	VSS-D		GND	GND	GND	—
18	A1	DG2 RIN4	Digital RGB.2 R-4bit or Digital YUV ITU-R BT.601 Y-4bit / ITU-R BT.656 YUV-4bit input.	IN	0 / 3.3	(*1)
19	B1	DG2 RIN5	Digital RGB.2 R-5bit (MSB) or Digital YUV ITU-R BT.601 Y-5bit / ITU-R BT.656 YUV-5bit input.	IN	0 / 3.3	(*1)
20	C1	DG2 GIN0	Digital RGB.2 G-0bit (LSB) or Digital YUV ITU-R BT.601 Y-6bit / ITU-R BT.656 YUV-6bit input.	IN	0 / 3.3	(*1)
21	C2	DG2 GIN1	Digital RGB.2 G-1bit or Digital YUV ITU-R BT.601 Y-7bit (MSB) / ITU-R BT.656 YUV-7bit (MSB) input.	IN	0 / 3.3	(*1)
22	VDD1.5-DRAM		1.5 V Power Supply for internal DRAM.	VDD	1.5	—
23	VSS-D		DRAM GND	GND	GND	—
24	VDD-IO		3.3 V Power Supply for I/O.	VDD	3.3	—
25	D1	DG2 GIN2	Digital RGB.2 G-2bit or Digital YUV ITU-R BT.601 UV-0bit (LSB) input.	IN	0 / 3.3	(*1)
26	D2	DG2 GIN3	Digital RGB.2 G-3bit or Digital YUV ITU-R BT.601 UV-1bit input.	IN	0 / 3.3	(*1)

(*1): Please refer to page 11.

Chip Pad No.	Package pin No.	Pin name	Function	I/O	Voltage [V]	When not in use.
27	E1	DG2 GIN4	Digital RGB.2 G-4bit or Digital YUV ITU-R BT.601 UV-2bit input.	IN	0 / 3.3	(*1)
28	E2	DG2 GIN5	Digital RGB.2 G-5bit (MSB) or Digital YUV ITU-R BT.601 UV-3bit input.	IN	0 / 3.3	(*1)
29	VDD-D		1.5V Power Supply for Logic circuit.	VDD	1.5	—
30	F1	DG2 BIN0	Digital RGB.2 B-0bit (LSB) or Digital YUV ITU-R BT.601 UV-4bit input.	IN	0 / 3.3	(*1)
31	F2	DG2 BIN1	Digital RGB.2 B-1bit or Digital YUV ITU-R BT.601 UV-5bit input.	IN	0 / 3.3	(*1)
32	G1	DG2 BIN2	Digital RGB.2 B-2bit or Digital YUV ITU-R BT.601 UV-6bit input.	IN	0 / 3.3	(*1)
33	G2	DG2 BIN3	Digital RGB.2 B-3bit or Digital YUV ITU-R BT.601 UV-7bit (MSB) input.	IN	0 / 3.3	(*1)
34	VDD1.5-DRAM		1.5 V Power Supply for internal DRAM.	VDD	1.5	—
35	VSS-D		DRAM GND	GND	GND	—
36	VDD2.5-DRAM		2.5 V Power Supply for internal DRAM.	VDD	2.5	—
37	VDD-IO		3.3 V Power Supply for I/O.	VDD	3.3	—
38	H1	DG2 BIN4	Digital RGB.2 B-4bit input.	IN	0 / 3.3	(*1)
39	H2	DG2 BIN5	Digital RGB.2 B-5bit (MSB) input.	IN	0 / 3.3	(*1)
40	VDD-D		1.5 V Power Supply for Logic circuit.	VDD	1.5	—
41	J1	DG2 Clock IN	Clock input for Digital RGB.2 or Digital YUV.	IN	0 / 3.3	(*2)
42	J2	DG2 H.Sync IN	Horizontal Sync signal input for Digital RGB.2 or Digital YUV.	IN	0 / 3.3	(*2)
43	K1	DG2 V.Sync IN	Vertical Sync signal input for Digital RGB.2 or Digital YUV.	IN	0 / 3.3	(*2)
44	K2	DG2 Overlay Cont IN2	Overlay control signal input for Digital RGB.2.	IN	0 / 3.3	(*2)
45	VDD-IO		3.3 V Power Supply for I/O.	VDD	3.3	—
46	L2	I2C-Bus Clock IN	I^2C-Bus SCL input. (Clock input) (up to 5 V)	IN	0 / 3.3	—
47	L1	EEPROM Clock Out	I^2C-Bus SCL for EEPROM control. (up to 5V)	IN / OUT	0 / 3.3	GND
48	M2	I2C-Bus Data IN / ACK / Read Out	I^2C-Bus SDA terminal. (up to 5V)	IN / OUT	0 / 3.3	—
49	M1	EEPROM Data IN / Out	I^2C-Bus SDA for EEPROM control. (up to 5 V)	IN / OUT	0 / 3.3	GND
50	VDD1.5-DRAM		1.5 V Power Supply for DRAM.	VDD	1.5	—
51	VSS-D		DRAM GND	GND	GND	—
52	M3	Panel Select IN	Set up GOE (D16 pin) operation at power on.	IN	0 / 3.3	—
53	N3	Test Scan	Set up Test mode. (Normally connect to GND)	IN	0 / 3.3	GND
54	VSS-D		GND	GND	GND	—
55	VDD-D		1.5 V Power Supply for Logic circuit.	VDD	1.5	—
56	N2	EEPROM Slave Select	Slave address select for EEPROM. Write (Low **:** A0h / High **:** A2h) Read (Low **:** A1h / High **:** A3h)	IN	0 / 3.3	GND

(*1), (*2)**:** Please refer to page 11.

Chip Pad No.	Package pin No	Pin name	Function	I/O	Voltage [V]	When not in use.
57	N1	Overlay Cont IN1	Overlay control signal input for Digital RGB.1 or Analog RGB.	IN	0 / 3.3	(*2)
58	P2	Display Mute IN	External mute. (Low : Off / High : Mute)	IN	0 / 3.3	GND
59	P1	Reset IN	Reset. (Low: Reset / High: Off) (up to 5 V)	IN	0 / 3.3	—
60	VDD-IO		3.3 V Power Supply for I/O.	VDD	3.3	—
61	VDD-D		1.5 V Power Supply for Logic circuit.	VDD	1.5	—
62	VSS-D		GND	GND	GND	—
63	—	ACTEG_1	Not connected (for Test mode)	—	—	—
64	—	ACTEG_2	Not connected (for Test mode)	—	—	—
65	—	ACTEG_3	Not connected (for Test mode)	—	—	—
66	—	ACTEG_4	Not connected (for Test mode)	—	—	—
67	VSS-D		GND	GND	GND	—
68	VDD-IO		3.3 V Power Supply for I/O.	VDD	3.3	—
69	R1	C.Video IN3 Force cont	The terminal which inputs Composite Video 3ch IN input forcibly. (High: Input signal at N15 pin is displayed by force in 800x480 panel without Overlay mode.)	IN	3.3	(*2)
70	T1	DG1 H.Sync IN	Horizontal Sync signal input for Digital RGB.1.	IN	3.3	(*2)
71	R2	DG1 V.Sync IN	Vertical Sync signal input for Digital RGB.1.	IN	3.3	(*2)
72	VDD-D		1.5 V Power Supply for Logic circuit.	VDD	1.5	—
73	T2	DG1 Clock IN	Clock input for Digital RGB.1.	IN	3.3	(*2)
74	VSS-D		GND	GND	GND	—
75	VDD-IO		3.3 V Power Supply for I/O.	VDD	3.3	—
76	T3	DG1 RIN5	Digital RGB.1 R-5bit (MSB) input.	IN	0 / 3.3	(*1)
77	R3	DG1 RIN4	Digital RGB.1 R-4bit input.	IN	0 / 3.3	(*1)
78	T4	DG1 RIN3	Digital RGB.1 R-3bit input.	IN	0 / 3.3	(*1)
79	VSS-D		GND	GND	GND	—
80	R4	DG1 RIN2	Digital RGB.1 R-2bit input.	IN	0 / 3.3	(*1)
81	T5	DG1 RIN1	Digital RGB.1 R-1bit input.	IN	0 / 3.3	(*1)
82	R5	DG1 RIN0	Digital RGB.1 R-0bit (LSB) input.	IN	0 / 3.3	(*1)
83	VDD-IO		3.3 V Power Supply for I/O.	VDD	0 / 3.3	—
84	VSS-D		GND	GND	GND	—
85	VDD-D		1.5 V Power Supply for Logic circuit	VDD	1.5	—
86	T6	DG1 GIN5	Digital RGB.1 G-5bit (MSB) input.	IN	0 / 3.3	(*1)
87	R6	DG1 GIN4	Digital RGB.1 G-4bit input.	IN	0 / 3.3	(*1)
88	T7	DG1 GIN3	Digital RGB.1 G-3bit input.	IN	0 / 3.3	(*1)
89	VSS-D		GND	GND	GND	—
90	R7	DG1 GIN2	Digital RGB.1 G-2bit input.	IN	0 / 3.3	(*1)
91	T8	DG1 GIN1	Digital RGB.1 G-1bit input.	IN	0 / 3.3	(*1)
92	R8	DG1 GIN0	Digital RGB.1 G-0bit (LSB) input.	IN	0 / 3.3	(*1)
93	VDD-IO		3.3 V Power Supply for I/O.	VDD	3.3	—
94	VSS-D		GND	GND	GND	—
95	VDD-D		1.5 V Power Supply for Logic circuit.	VDD	1.5	—

(*1), (*2): Please refer to page 11.

Chip Pad No.	Package pin No.	Pin name	Function	I/O	Voltage [V]	When not in use.
96	T9	DG1 BIN5	Digital RGB.1 B-5bit (MSB) input.	IN	0 / 3.3	(*1)
97	R9	DG1 BIN4	Digital RGB.1 B-4bit input.	IN	0 / 3.3	(*1)
98	T10	DG1 BIN3	Digital RGB.1 B-3bit input.	IN	0 / 3.3	(*1)
99	VSS-D		GND	GND	GND	—
100	R10	DG1 BIN2	Digital RGB.1 B-2bit input.	IN	0 / 3.3	(*1)
101	T11	DG1 BIN1	Digital RGB.1 B-1bit input.	IN	0 / 3.3	(*1)
102	R11	DG1 BIN0	Digital RGB.1 B-0bit (LSB) input.	IN	0 / 3.3	(*1)
103	VDD-IO		3.3 V Power Supply for I/O.	VDD	3.3	—
104	VSS-D		GND	GND	GND	—
105	VDD-D		1.5 V Power Supply for Logic circuit.	VDD	1.5	—
106	R13	C.Video Sync IN	Sync signal input for Composite Video 1ch, 2ch and 3ch.	IN	0 / 3.3	(*2)
107	VDD-XTAL		2.5 V Power Supply for Xtal.	VDD	2.5	—
108	VDD-XTAL		2.5 V Power Supply for Xtal.	VDD	2.5	—
109	T12	X'TAL IN	Input pin for Xtal circuit.	IN	AC 0.5 (min)	—
110	R12	X'TAL OUT	Output pin for Xtal circuit.	OUT	0 / 3.3	—
111	VSS-XTAL		Xtal GND (= VSS-D)	GND	GND	—
112	VSS-XTAL		Xtal GND (= VSS-D)	GND	GND	—
113	VSS-PLL		PLL GND	GND	GND	—
114	VDD-PLL		2.5 V Power Supply for PLL.	VDD	2.5	—
115	T14	PLL IN	PLL input.	IN	(*4)	—
116	T13	PLL FILTER	Filter pin for PLL.	—	typ. 1.0	—
117	VSS-PLL		PLL GND	GND	GND	—
118	VDD-DSEP / DAC	VDD-DAC	2.5 V Power Supply for DA Converter.	VDD	2.5	—
119	R14	DAC OUT	Output pin for fundamental 8.3 MHz of PLL.	OUT	(*4)	—
120	VSS-DSEP / DAC	VSS-DAC	DA Converter GND	GND	GND	—
121	T15	DAC BIAS	Capacitor connection pin for Bias stabilization of DA Converter. (Normally connect to Capacitor (0.1 µF) before GND)	OUT	—	—
122	VDD-DSEP / DAC	VDD-DSEP	2.5 V Power Supply for Component video input circuit.	VDD	2.5	—
123	R15	A-3ch H.Sync IN1 / C.Sync IN1	Horizontal Sync signal input for Component Video 1ch or Mix Sync signal input for Component Video 1ch.	IN	(*5)	(*2)
124	T16	A-3ch V.Sync IN1 / C.Sync IN2	Vertical Sync signal input for Component Video 1ch or Mix Sync signal input for Component Video 2ch.	IN	(*5)	(*2)
125	VSS-DSEP / DAC	VSS-DESP	GND for Sync generation of Component video signal.	GND	GND	—
126	R16	SADC VREFT	Reference top voltage pin of Composite Video ADC . (Normally connect to Capacitor (0.1 µF) before GND)	OUT	—	—
127	P16	SADC BIAS	Bias pin of Composite Video ADC. (Normally connect to Capacitor (0.1 µF) before GND)	OUT	—	—

(*1), (*2), (*4), (*5) : Please refer to page 11.

Chip Pad No.	Package pin No.	Pin name	Function	I/O	Voltage [V]	When not in use.
128	VDD-SADC / ADC Logic	VDD-ADC Logic	2.5 V Power Supply for logic block of ADC.	VDD	2.5	—
129	P15	CVBS IN1	Composite Video 1ch input.	IN	(*6)	(*3)
130	VSS-SADC		Composite Video ADC GND	GND	GND	—
131	N16	CVBS IN2	Composite Video 2ch input.	IN	(*6)	(*3)
132	VDD-SADC / ADC Logic	VDD-SADC	2.5 V Power Supply for Composite Video ADC.	VDD	2.5	—
133	N15	CVBS IN3	Composite Video 3ch input.	IN	(*6)	(*3)
134	M15	SADC VREFB	Reference bottom voltage pin of Composite Video ADC. (Normally connect to Capacitor (0.1 µF) before GND)	OUT	—	—
135	VSS-SADC		Composite Video ADC GND	GND	GND	—
136	VSS-MADC		Component Video (R/Cr) ADC GND	GND	GND	—
137	VDD-MADC		2.5 V Power Supply for Component Video (R/Cr) ADC.	VDD	2.5	—
138	M16	MADC VREFT	Reference top voltage pin of Component Video ADC. (Normally connect to Capacitor (0.1µF) before GND)	OUT	—	—
139	L15	R/Cr IN1	Component Video 1ch R or Cr input.	IN	(*7)	(*3)
140	L16	G/Y IN1	Component Video 1ch G or Y input. (Combined use Camera mode)	IN	(*7)	(*3)
141	K15	B/Cb IN1	Component Video 1ch B or Cb input.	IN	(*7)	(*3)
142	VSS-MADC		Component Video (G/Y) ADC GND	GND	GND	—
143	VDD-MADC		2.5 V Power Supply for Component Video (G/Y) ADC.	VDD	2.5	—
144	K16	R/Cr IN2	Component Video 2ch R or Cr input.	IN	(*7)	(*3)
145	J15	G/Y IN2	Component Video 2ch G or Y input. (Combined use Camera mode)	IN	(*7)	(*3)
146	J16	B/Cb IN2	Component Video 2ch B or Cb input.	IN	(*7)	(*3)
147	H15	MADC VREFB	Reference bottom voltage pin of Component Video ADC. (Normally connect to Capacitor (0.1µF) before GND)	OUT	—	—
148	H16	MADC BIAS	Bias pin of Component Video ADC. (Normally connect to Capacitor (0.1µF) before GND)	OUT	—	—
149	VSS-MADC		Component Video (B/Cb) ADC GND	GND	GND	—
150	VDD-MADC		2.5 V Power Supply for Component Video (B/Cb) ADC.	VDD	2.5	—
151	H12	Test mode1	Set up Test mode. (Normally connect to GND)	IN	0 / 3.3	GND
152	H11	Test mode2	Set up Test mode. (Normally connect to GND)	IN	0 / 3.3	GND
153	G13	Test mode3	Set up Test mode. (Normally connect to GND)	IN	0 / 3.3	GND
154	G12	Test mode4	Set up Test mode. (Normally connect to GND)	IN	0 / 3.3	GND
155	VDD-D		1.5 V Power Supply for Logic circuit.	VDD	1.5	—
156	VSS-D		GND	GND	GND	—
157	VDD-IO		3.3 V Power Supply for I/O.	VDD	3.3	—
158	G11	(DRAM)MB	Set up Test mode. (Normally connect to GND)	IN	0 / 3.3	GND

(*3), (*6), (*7) : Please refer to page 11.

Chip Pad No.	Package pin No.	Pin name	Function	I/O	Voltage [V]	When not in use.
159	F13	MBIST	Set up Test mode (Normally connect to GND)	IN	0 / 3.3	GND
160	VDD-D		1.5 V Power Supply for Logic circuit.	VDD	1.5	—
161	VSS-D		GND	GND	GND	—
162	VDD-IO		3.3 V Power Supply for I/O.	VDD	3.3	—
163	G16	Monitor Out1	Internal test signal monitor output 1.	OUT	0 / 3.3	Open
164	G15	Vcom1 Out	Control signal for LCD. (Common Electrode output)	OUT	0 / 3.3	Open
165	G14	V-Load	Control signal for LCD. (Latch signal for Gate)	OUT	0 / 3.3	Open
166	F14	Vcom2 Out	Control signal for LCD. (Common Electrode output)	OUT	0 / 3.3	Open
167	VDD-D		1.5 V Power Supply for Logic circuit	VDD	1.5	—
168	VSS-D		GND	GND	GND	—
169	VDD-IO		3.3 V Power Supply for I/O	VDD	3.3	—
170	F16	STV1 Out	Control signal for LCD. (Start signal for Gate) (Three state buffer terminal.)	OUT	0 / 3.3	Open
171	F15	U/D Out	Control signal for LCD. (Vertical panel control)	OUT	0 / 3.3	Open
172	E16	CPV Out	Control signal for LCD. (Gate clock signal)	OUT	0 / 3.3	Open
173	E15	Hcom(Dot REV)	Control signal for LCD. (Data invert signal)	OUT	0 / 3.3	Open
174	VDD-D		1.5 V Power Supply for Logic circuit.	VDD	1.5	—
175	VSS-D		GND	GND	GND	—
176	VDD-IO		3.3 V Power Supply for I/O.	VDD	3.3	—
177	D16	GOE Out	Reset signal output for LCD.	OUT	0 / 3.3	Open
178	D15	STV2 Out	Control signal for LCD. (Start signal for Gate) (Three state buffer terminal.)	OUT	0 / 3.3	Open
179	C15	Enable Out	Control signal for LCD. (Data Enable)	OUT	0 / 3.3	Open
180	C16	Load Out	Control signal for LCD. (Latch signal for Source)	OUT	0 / 3.3	Open
181	VSS-D		GND	GND	GND	—
182	B16	STH Out	Control signal for LCD. (Start signal for Source)	OUT	0 / 3.3	Open
183	VDD-D		1.5 V Power Supply for Logic circuit.	VDD	1.5	—
184	VDD-IO		3.3 V Power Supply for I/O.	VDD	3.3	—
185	VSS-D		GND	GND	GND	—
186	C14	Dimmer(PWM)	LED back light control signal output.	OUT	0 / 3.3	Open
187	VSS-D		GND	GND	GND	—
188	VDD-D		1.5 V Power Supply for Logic circuit.	VDD	1.5	—
189	VDD-IO		3.3 V Power Supply for I/O.	VDD	3.3	—
190	A16	CPH Out	Control signal for LCD. (Horizontal clock signal)	OUT	0 / 3.3	Open
191	VSS-D		GND	GND	GND	—
192	VDD-D		1.5 V Power Supply for Logic circuit.	VDD	1.5	—
193	D14	Monitor Out2	Internal test signal monitor output 2.	OUT	0 / 3.3	Open
194	B15	D-R7 Out	R-7bit (MSB) output.	OUT	0 / 3.3	Open
195	A15	D-R6 Out	R-6bit output.	OUT	0 / 3.3	Open
196	B14	D-R5 Out	R-5bit output.	OUT	0 / 3.3	Open
197	VSS-D		GND	GND	GND	—
198	A14	D-R4 Out	R-4bit output.	OUT	0 / 3.3	Open

Chip Pad No.	Package pin No.	Pin name	Function	I/O	Voltage [V]	When not in use.
199	B13	D-R3 Out	R-3bit output.	OUT	0 / 3.3	Open
200	A13	D-R2 Out	R-2bit output.	OUT	0 / 3.3	Open
201	VDD-IO		3.3 V Power Supply for I/O.	VDD	3.3	—
202	VSS-D		GND	GND	GND	—
203	VDD-D		1.5 V Power Supply for Logic circuit.	VDD	1.5	—
204	B12	D-R1 Out	R-1bit output.	OUT	0 / 3.3	Open
205	A12	D-R0 Out	R-0bit (LSB) output.	OUT	0 / 3.3	Open
206	VDD-IO		3.3 V Power Supply for I/O.	VDD	3.3	—
207	VSS-D		GND	GND	GND	—
208	B11	D-G7 Out	G-7bit (MSB) output.	OUT	0 / 3.3	Open
209	A11	D-G6 Out	G-6bit output.	OUT	0 / 3.3	Open
210	B10	D-G5 Out	G-5bit output.	OUT	0 / 3.3	Open
211	VSS-D		GND	GND	GND	—
212	A10	D-G4 Out	G-4bit output.	OUT	0 / 3.3	Open
213	B9	D-G3 Out	G-3bit output.	OUT	0 / 3.3	Open
214	A9	D-G2 Out	G-2bit output.	OUT	0 / 3.3	Open
215	VDD-IO		3.3 V Power Supply for I/O.	VDD	3.3	—
216	VSS-D		GND	GND	GND	—
217	VDD-D		1.5 V Power Supply for Logic circuit.	VDD	1.5	—
218	B8	D-G1 Out	G-1bit output.	OUT	0 / 3.3	Open
219	A8	D-G0 Out	G-0bit (LSB) output.	OUT	0 / 3.3	Open
220	VDD-IO		3.3 V Power Supply for I/O.	VDD	3.3	—
221	VSS-D		GND	GND	GND	—
222	VDD-D		1.5 V Power Supply for Logic circuit.	VDD	1.5	—
223	B7	D-B7 Out	B-7bit (MSB) output.	OUT	0 / 3.3	Open
224	A7	D-B6 Out	B-6bit output.	OUT	0 / 3.3	Open
225	B6	D-B5 Out	B-5bit output.	OUT	0 / 3.3	Open
226	VSS-D		GND	GND	GND	—
227	A6	D-B4 Out	B-4bit output.	OUT	0 / 3.3	Open
228	B5	D-B3 Out	B-3bit output.	OUT	0 / 3.3	Open
229	A5	D-B2 Out	B-2bit output.	OUT	0 / 3.3	Open
230	VDD-D		1.5 V Power Supply for Logic circuit.	VDD	1.5	—
231	VDD1.5-DRAM		1.5 V Power Supply for DRAM.	VDD	1.5	—
232	VSS-D		DRAM GND	GND	GND	—
233	VDD2.5-DRAM		2.5 V Power Supply for DRAM.	VDD	2.5	—
234	VDD-IO		3.3 V Power Supply for I/O.	VDD	3.3	—
235	B4	D-B1 Out	B-1bit output.	OUT	0 / 3.3	Open
236	A4	D-B0 Out	B-0bit (LSB) output.	OUT	0 / 3.3	Open
237	VDD-D		1.5 V Power Supply for Logic circuit.	VDD	1.5	—
238	VSS-D		GND	GND	GND	—
239	VDD-IO		3.3 V Power Supply for I/O.	VDD	3.3	—
240	C4	Test Pin-A	Set up Test mode. (Normally connect to GND)	IN	0 / 3.3	GND

Chip Pad No.	Package pin No.	Pin name	Function	I/O	Voltage [V]	When not in use.
241	D4	Direct Access	The control terminal for direct write mode of EEPROM (High : Direct connection between the terminal of I^2C bus and control terminal of EEPROM)	IN	0 / 3.3	GND (Note1)
242	E4	I2C Slave Select	I^2C-Bus Slave address select. Write (Low : 2Eh / High : 2Ch) Read (Low : 2Fh / High : 2Dh)	IN	0 / 3.3	—
243	VDD-IO		3.3 V Power Supply for I/O.	VDD	3.3	—
244	VDD-D		1.5 V Power Supply for Logic circuit.	VDD	1.5	—
245	VSS-D		GND	GND	GND	—

Note1: If Direct Access terminal becomes “High Level”, I^2C-Bus control terminal and EEPROM control terminal are connected at internal circuit. When it is not used Direct Access mode, it must be connected to GND.

(*1): Connect to GND or Open. Some of terminals are active as below, connect to GND for unused terminals.

Example: DG1 RIN5 to RIN0

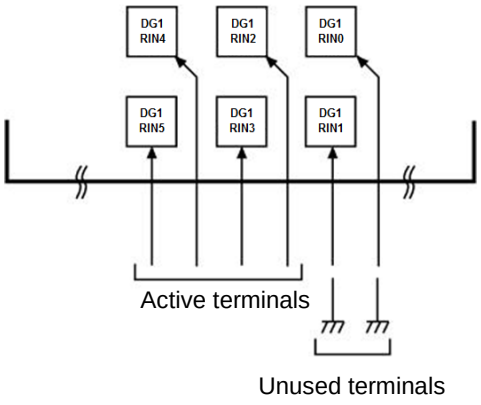


Figure 6-1 Disposal method of terminal

(*2): It better to connect to GND rather than open, when signal does not input.

(*3): It better to connect to GND with Capacitor (0.1 µF) rather than open, when do not input signal.

(*4): DAC Out (R14 pin) outputs sine wave (8.3 MHz frequency, 1.0 V_{P-P} amplitude). It is inputted to PLL IN (T14 pin) after reduce high frequency component (noise component) by external LPF as below.

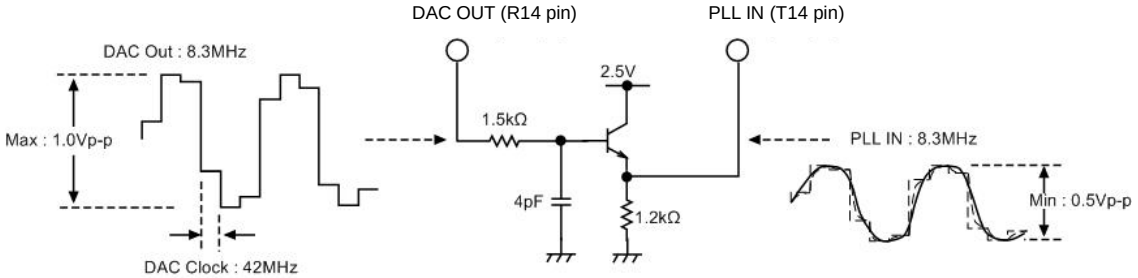


Figure 6-2 Low pass filter circuit for DAC Out

(*5): Refer to Figure 8-12 for synchronous signal of component video signal

(*6): Recommended amplitude of input Video signal is 0.7 V_{P-P} at 140IRE. Refer to Figure 8-15.

(*7): Recommended amplitude of input component video signal (YCbCr) and RGB signal, refer to Figure 8-10.

7. Signal flow diagram

7.1 Video signal flow

Block Diagram Signal Flow

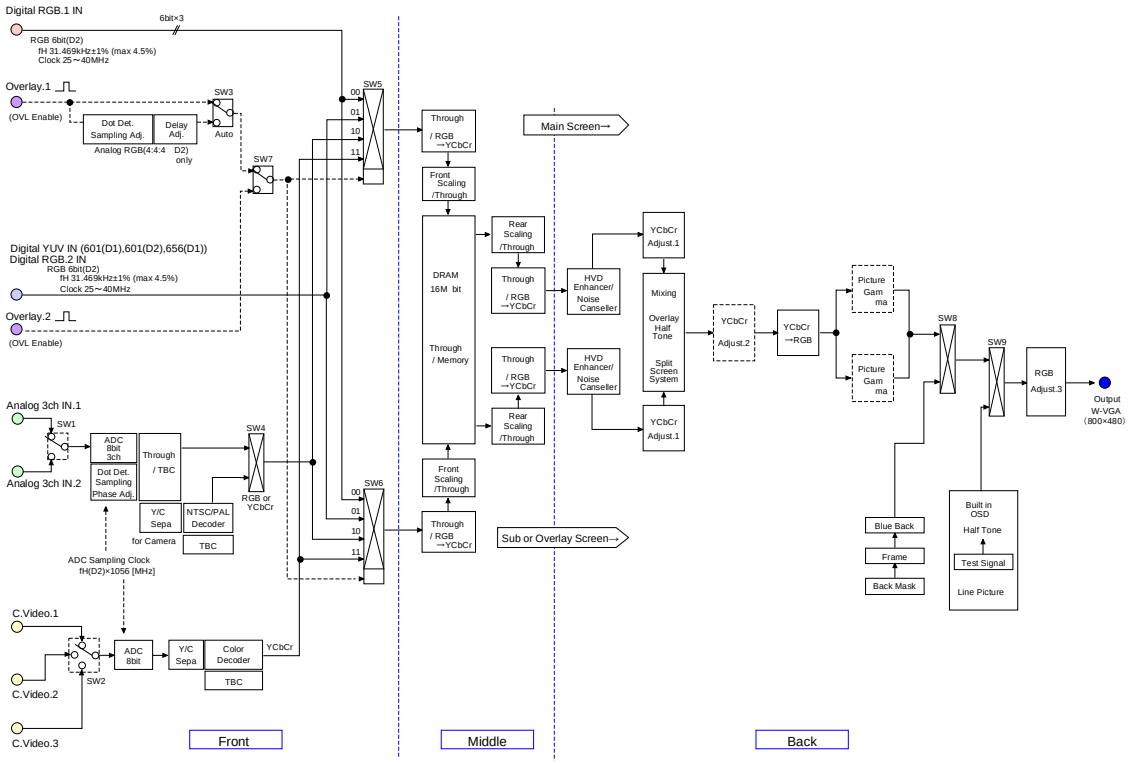


Figure 7-1 Video signal flow

7.2 Synchronous signal flow

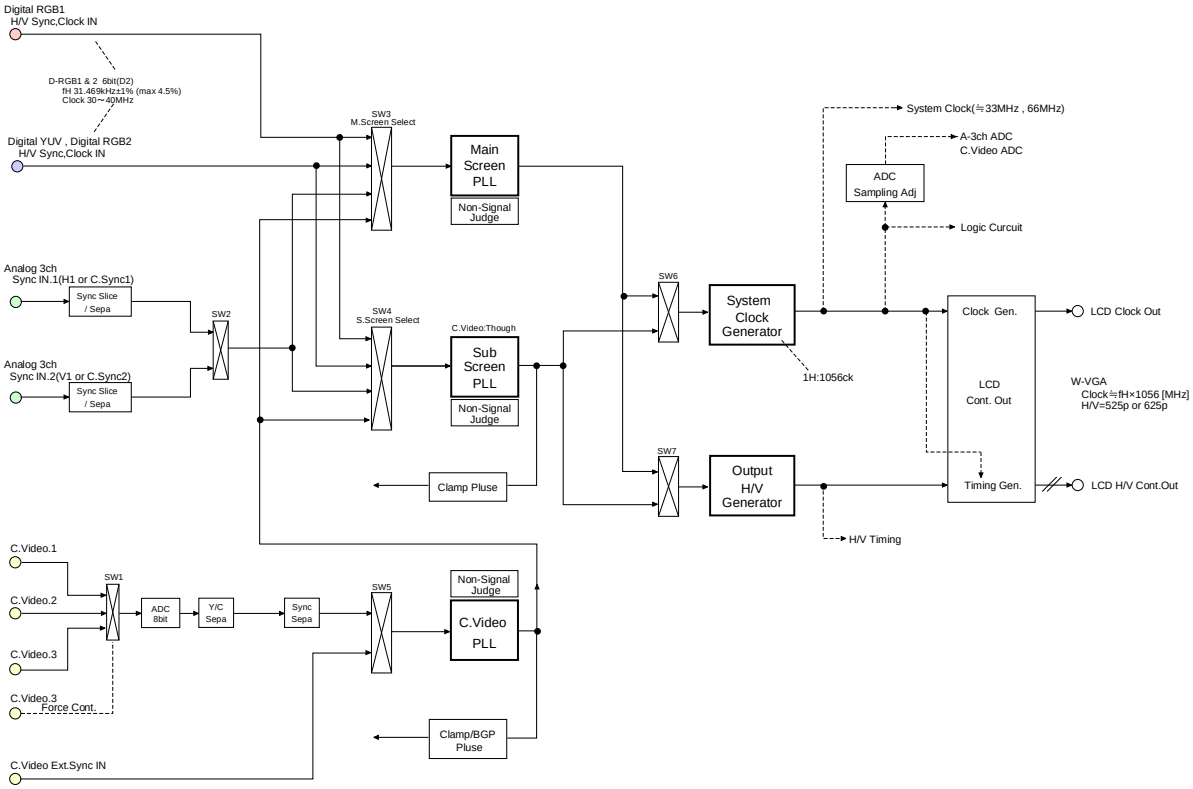


Figure 7-2 Synchronous signal flow

8. Functional description

8.1 Input signal format

TC90197 has input interface as below.

Table 8-1 Input signal and correspondence format

Input signal		Format
Digital RGB		525p, 625p
Digital YUV	ITU-R BT.601	525i, 625i, 525p, 625p
	ITU-R BT.656	525i, 625i
Analog Component	RGB	525i, 625i, 525p, 625p
	YCbCr	525i, 625i, 525p, 625p
	Camera mode	NTSC, PAL
Composite Video		NTSC, PAL, SECAM, PAL-M, PAL-N, PAL60, 443NTSC

8.1.1 The frequency range of the input horizontal synchronous signal

It must be used within ±4% frequency for center frequency of horizontal synchronous signal (f_H).
Recommended frequency deviation is within ±1%.

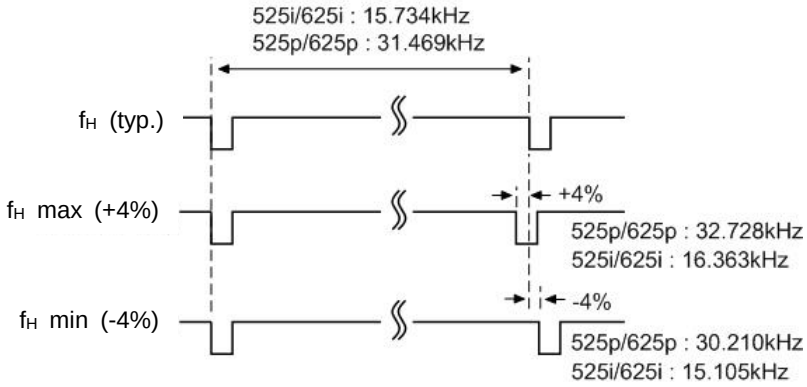


Figure 8-1 Horizontal sync signal input level

It can change the range of frequency for horizontal synchronous signal by Bank-1 3E hex [D13]. When input signal is over the range mentioned at table 8-2, H.PLL become unlock status and it cannot display the screen normally.
In addition, when input H-sync signal changes to non-signal, H.PLL switches free-run mode.
(±1% mode)**:** The free run frequency of it is more stable than ±4.5% mode at non-H-sync.

Table 8-2 Input range of horizontal synchronous frequency

Range of frequency for horizontal synchronous signal Bank-1 3E hex [13]		Input H-sync frequency f_H [kHz]		
		Min	Typ.	Max
0 **:** ±1% mode	525i / 625i	15.578	15.734	15.891
	525p / 625p	31.155	31.469	31.783
1 **:** ±4.5% mode	525i / 625i	15.106	15.734	16.363
	525p / 625p	30.211	31.469	32.727

8.1.2 Setup and Hold time for Digital signal input

The sampling timing for data with clock at input stage, it is used center phase of data. (Reference condition)
The specification of Setup and Hold time for Data and clock is minimum 5ns and for input synchronous signal is minimum 7 ns.

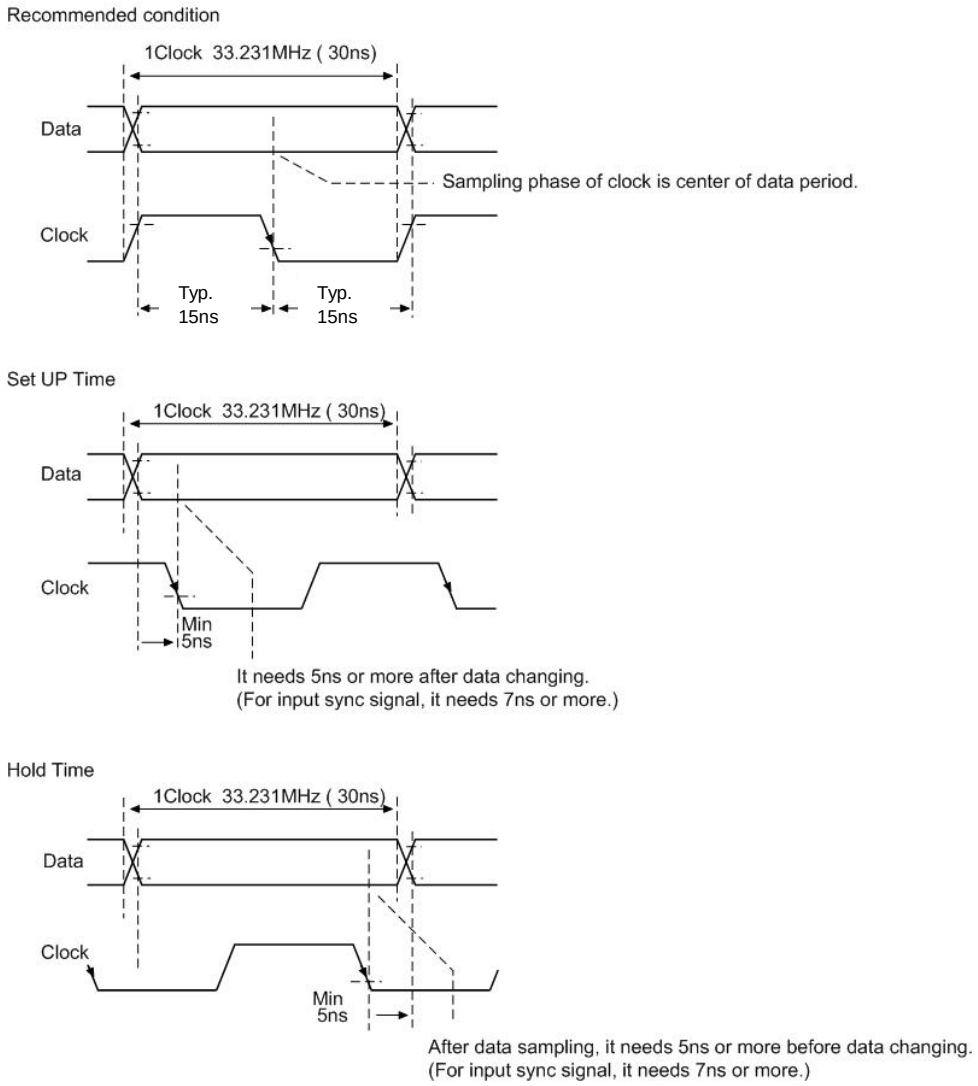


Figure 8-2 Setup and Hold time for Digital input signal

8.1.3 Digital RGB input

Input interface for Digital RGB. It adopts 525p / 625p signal format.
The range of digital RGB input is 6bit (6bit×3).

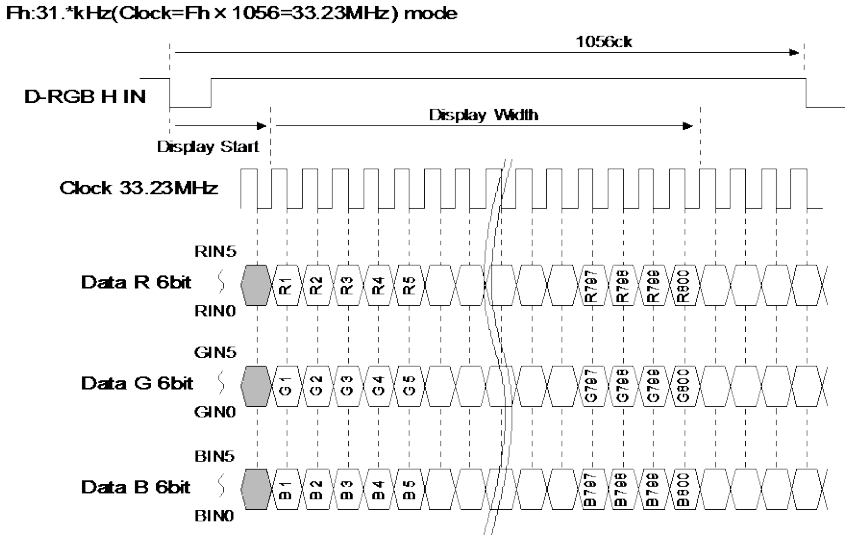


Figure 8-3 Input timing for Digital RGB

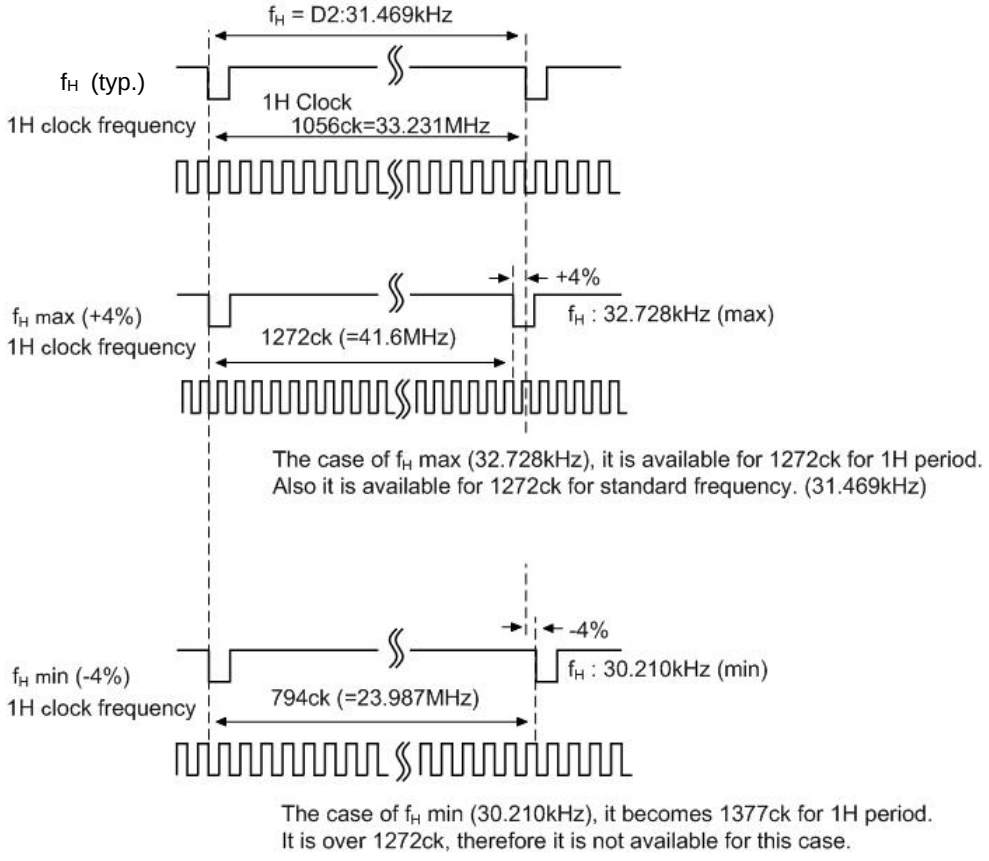


Figure 8-4 Input horizontal frequency and clock specific for Digital RGB

8.1.4 Digital YUV input

Digital YUV input can input a format of ITU-R BT.601 and ITU-R BT.656.

ITU-R BT.601

Input interface for ITU-R BT.601. It adopts 525i / 625i / 525p / 625p signal format.
The range of digital YUV input is 8bit (8bit×3).

Fh:15.*kHz(Clock:13.5MHz)

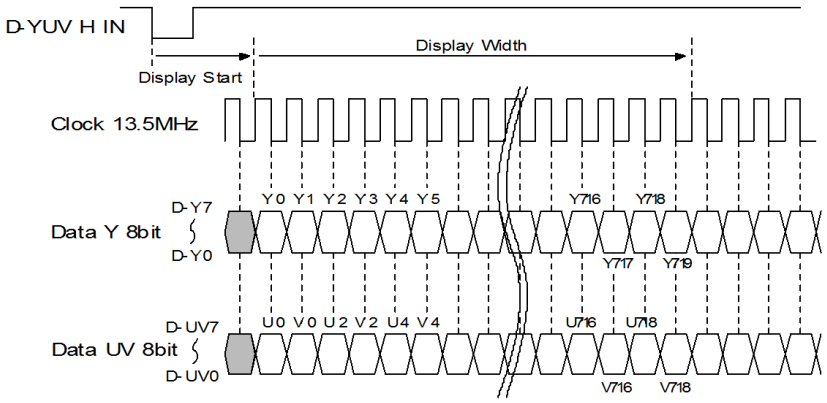


Figure 8-5 Input timing for Digital YUV ITU-R BT.601(525i/625i)

Fh:31.*kHz(Clock:27MHz)

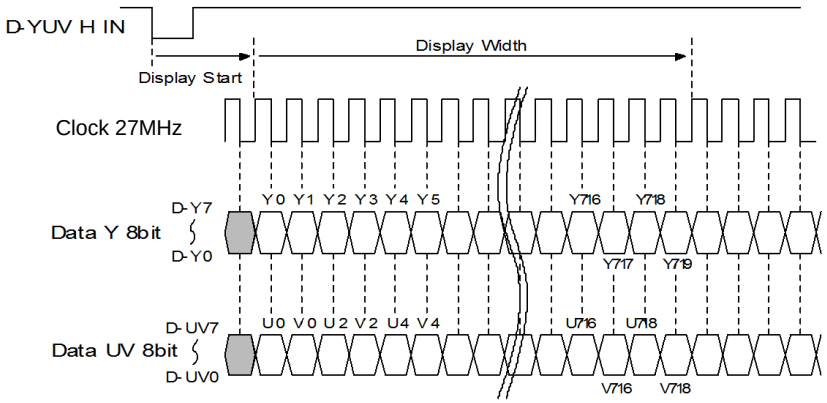


Figure 8-6 Input timing for Digital YUV ITU-R BT.601(525p/625p)

ITU-R BT.656

Digital YUV input interface for ITU-R BT.656. It adopts 525i / 625i signal format.
Input signal is data of 8bit and clock of 27MHz.

Fh:15.*kHz(Clock:27MHz)

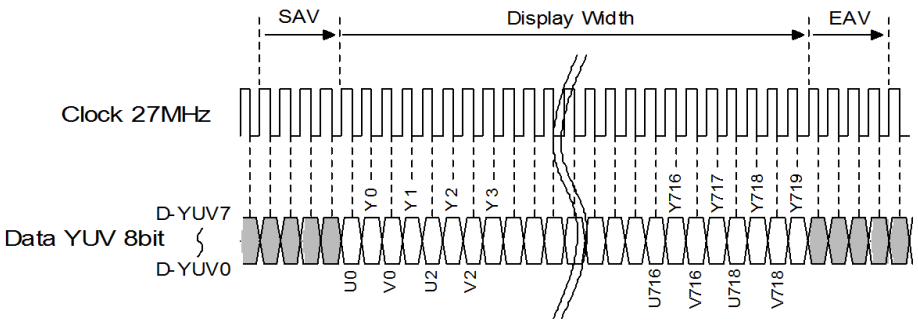


Figure 8-7 Input timing for Digital YUV ITU-R BT.656

Digital YUV Input sync signal

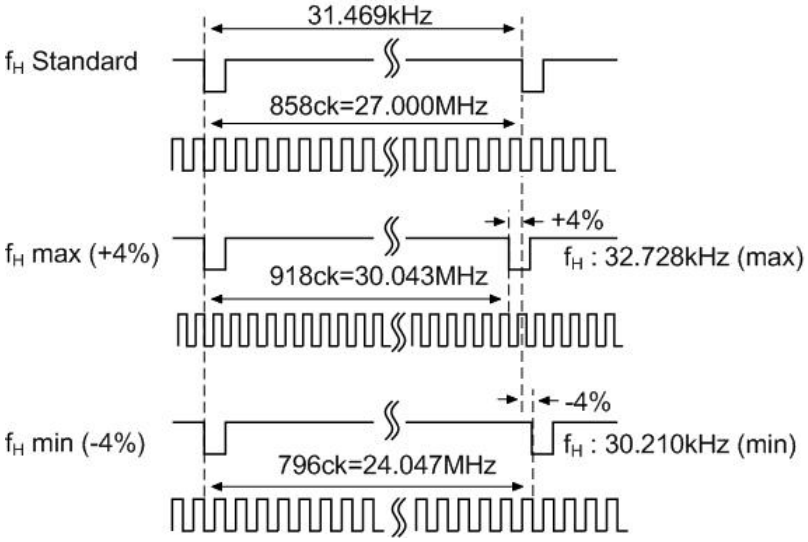


Figure 8-8 Input horizontal frequency and clock specific for Digital YUV ITU-R BT.601(525p/625p), ITU-R BT.656(525i/625i)

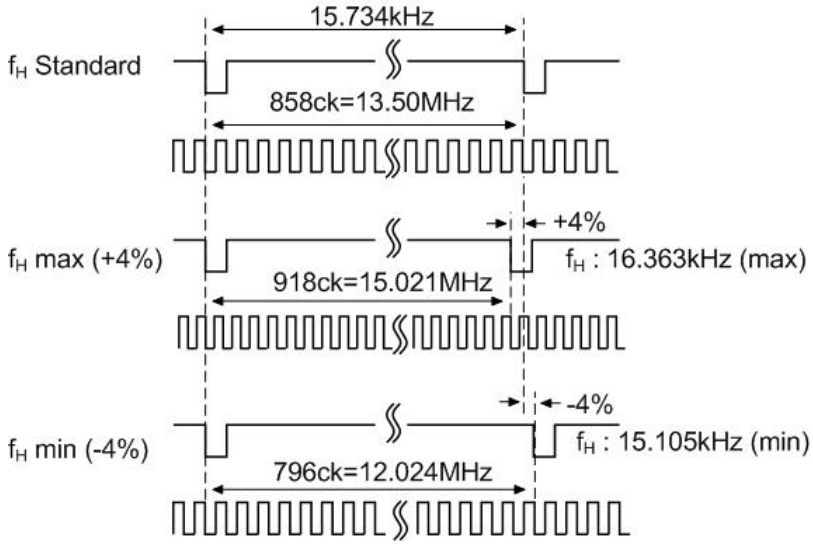
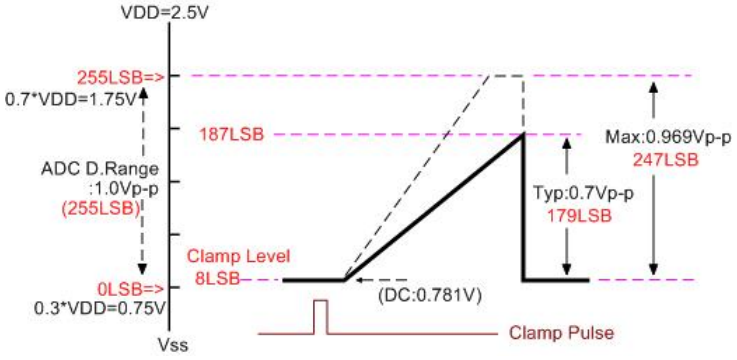


Figure 8-9 Input horizontal frequency and clock specific for Digital YUV ITU-R BT.601(525i/625i)

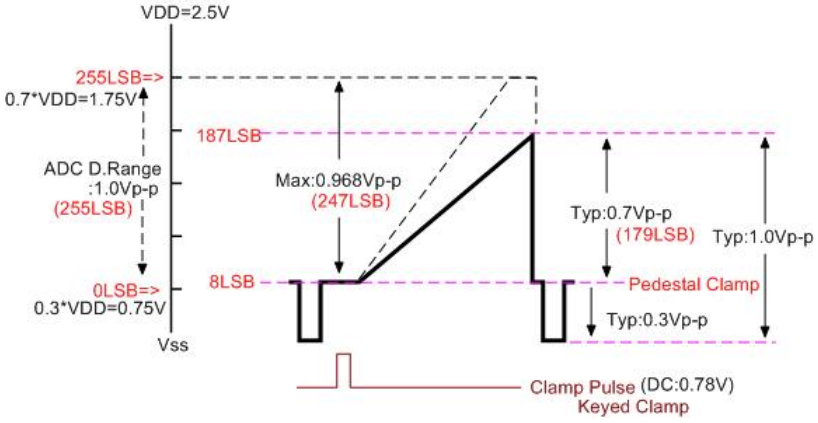
8.1.5 Analog component video signal (RGB, YCbCr)

3ch ADC input interface adopts RGB and YCbCr (525i, 525p, 625i, 625p) and also has 2ch interface (IN1 and IN2). The dynamic range of ADC is 1.0 Vp-p (V_{DD}×0.4). The reference value of amplitude of analog input signal is as below. When it uses 2.5 V standard voltage, the dynamic range of ADC is 1.0 V_{P-P}. Please refer to Figure 8-10.

- R, G, B, Y input (External H-Sync and V-Sync)



- R, G, B, Y input (Sync on G or Sync on Y)



- Cb, Cr input

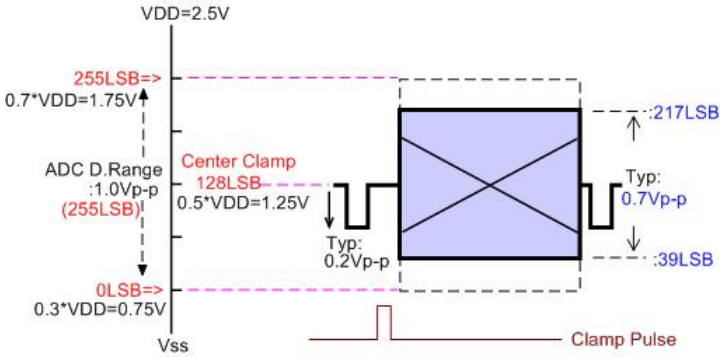


Figure 8-10 Recommended input amplitude of Component video

Camera input mode

TC90197XBG has extra video decoder for car camera application.

In this mode, analog component input is not available due to use 1ch ADC for Camera input mode. Input pin for Camera is Analog G/Y pin (L-16pin or J-15pin).

It requires standard NTSC or PAL composite video signal. The amplitude of it at input stage of ADC is shown as below.

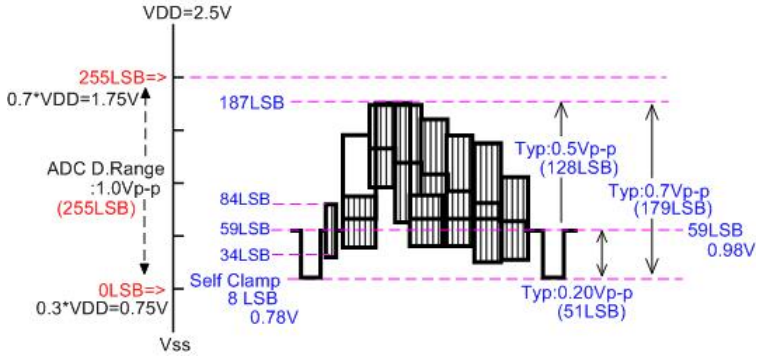


Figure 8-11 Recommended input amplitude of Camera input

Sync signal input

It is selectable 2 type of sync (*) signal for Analog component signal input 1.

(*)**:** C-Sync (Composite Sync) , H-Sync / V-Sync (Horizontal Sync and Vertical Sync)

It is C-Sync mode only for component signal input 2.

Table 8-3 Sync signal for Analog component

Sync signal for component video		R-15 pin	T-16 pin
Input 1ch	C-Sync	○	—
	H-Sync / V-Sync	○ (H-Sync)	○ (V-Sync)
Input 2ch	C-Sync	—	○
	H-Sync / V-Sync	×	×

Note 1**:** H-sync pulse width is 78ck typically. (min**:** 64ck, max**:** 90ck)

Note 2**:** V-sync pulse width is 3 line typically. (min**:** 2 line, max**:** 7 line)

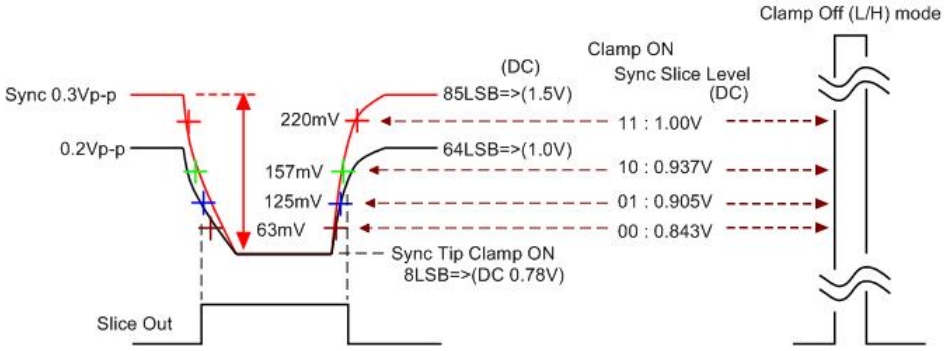
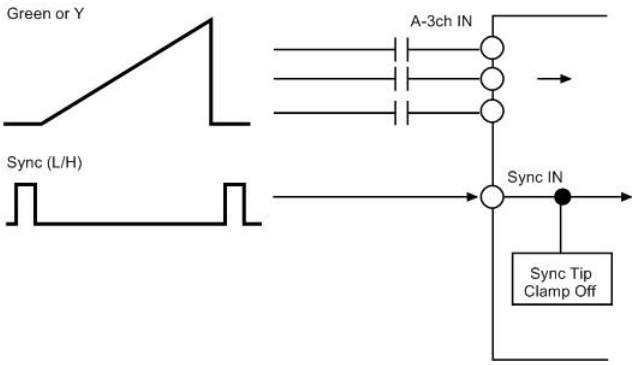


Figure 8-12 Synchronous input level for component video signal



The case of input signal with composite sync

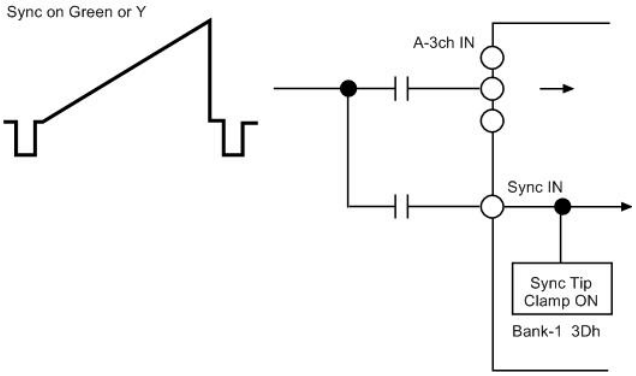


Figure 8-13 Method for component sync signal input

Sync input method for camera signal is same as component signal. Input terminal is R-15 pin or T-16 pin.

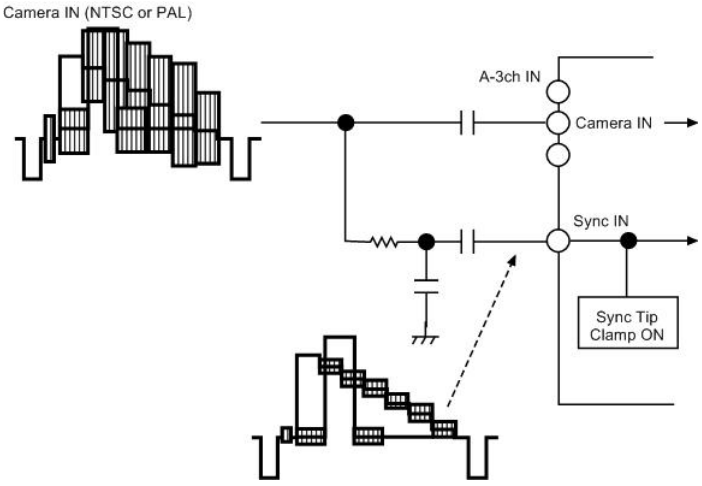


Figure 8-14 Method for camera sync signal input

8.1.6 Composite video signal

Composite signal adopts multi-color system (NTSC, PAL, SECAM, PAL-M, PAL-N, PAL60, 443NTSC).

In this interface there are 3ch selectors (C.Video1, C.Video2, C.Video3) at input stage of 8bit ADC.

When it is used 2.5V standard voltage, the dynamic range of ADC is designed as 1 Vp-p (V_{DD} × 0.4). In addition the recommendation value of it is 0.7 Vp-p.

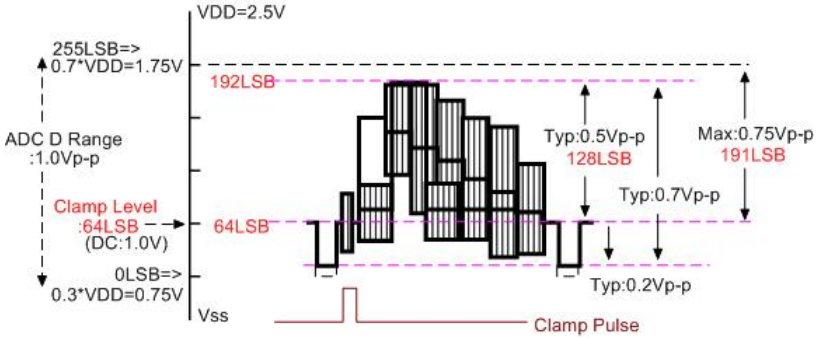


Figure 8-15 Recommended input amplitude of Composite video

Forced Composite video display mode

Regarding CVBS IN3 input (N15 pin), its display can be controlled by R-1pin forcibly. In this mode, it is not available to use overlay function.

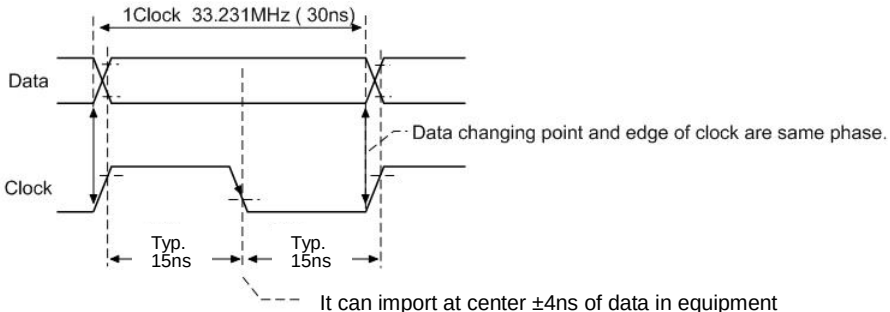
R1 pin	Function
Low	Normal mode (I^2C-Bus control)
High	Forced CVBS IN3 display mode.

8.2 Output signal

8.2.1 Output signal format

The phase relation between output data and clock is shown as below. The output data has maximum 4 ns delay against clock. It can import at center ±4ns of data in equipment which receives this signal.

Basic output signal



Output signal with delay time

There is time difference for ±4ns for output signal.

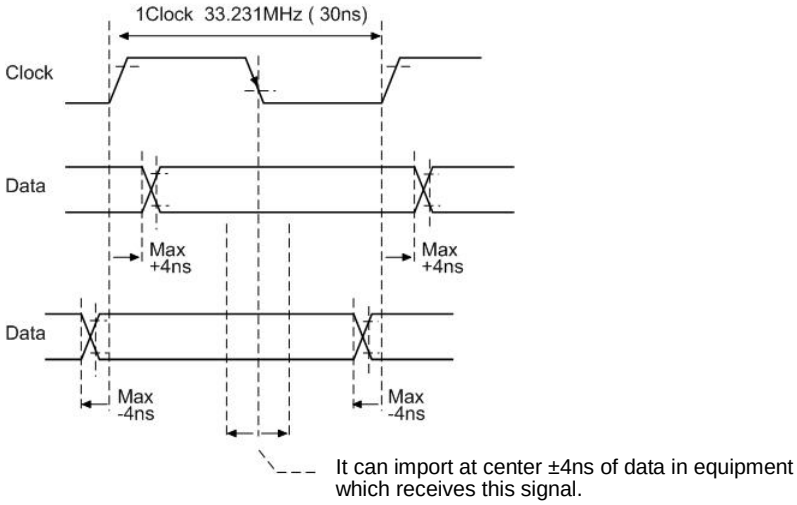


Figure 8-16 Relative delay for output signal

8.2.2 PWM output

PWM signal, it can be outputted from DIMMER (C14 pin).

The duty of it is set via I^2C-Bus from 0.024% to 100%.

It can be provided offset value by using the data of APL or dark area level of Dynamic-γ or blight area level of Dynamic-γ.

8.3 Explanation of LCD panel connection

TC90197XBG has Timing control function (T-Con) for LCD. There are some kinds of LCD witch needs different timing control signal.

Then it needs to start to provide power supply for LCD panel before TC90197 to avoid over current on it.

8.3.1 Timing control signal

The timing control signals those are set active or non-active individually via I2C-Bus. Regarding horizontal start pulse, it has 2 modes to adopt different types of LCD. (Built in T-Con or non T-Con)

(1) STH mode
1 dot and 1 clock horizontal start pulse. It is for non T-Con LCD panel.

(2) HD mode (for built in T-Con LCD panel)
It outputs horizontal start pulse which has same phase with the reference signal (H.LCD.REF).
It is for T-Con LCD panel.

The name of timing control signal are different. It is called different types of LCD panel.
Please refer to table 8-4 by way of example.

Table 8-4 Timing control signal

Pin No.	Function	Pin name of TC90197		The name of signal in LCD panel			Note
		Non T-Con LCD pane	Built in T-Con LCD panel	Example1	Example2	Example3	
B16	Horizontal writing Start Pulse	STH	HD	SPR or SPL	HSY	HS	(*1)
C16	Horizontal writing Enable Pulse	Load	—	LS	—	—	
A16	Horizontal Clock	CPH	Clock	DCLK	CLK	DCLK	
E15	Horizontal latch	Hcom	—	—	—	—	
F16	Vertical writing Start Pulse 1	STV1	VD	SPS	VSY	VS	(*2)
D15	Vertical writing Start Pulse 2	STV2	—	—	—	—	(*2)
G14	Vertical writing Enable Pulse	V-Load	—	—	—	—	
E16	Vertical Clock	CPV	—	CLS	—	—	
C15	The Period of active picture	—	Enable	—	ENAB	EN	
G15	Common Electrode output 1	Vcom1	—	VCOM	—	—	(*3)
F14	Common Electrode output 2	Vcom2	—	VCOM	—	—	(*3)
D16	Panel Reset output	GOE	—	MODE1, 2	—	—	
F15	Bus Port Control output	U/D	—	U/L	—	—	

(*1)**:** Some of LCD panels have 2 input pins for horizontal start pulse. But this IC has 1 output pin (B16 pin).

(*2)**:** There are 2 output pins as Vertical start pulse (STV1 (F16 pin) and STV2 (D15 pin)). But non selected pin is not active.

(*3)**:** Vcom2 (F14 pin) can be set to shift the phase against Vcom1 (G15 pin) via I^2C-Bus.

9. Absolute Maximum Rating

The parameters listed in the following absolute maximum rating table are limit values for this product.
Exceeding even one of these limit values even momentarily may cause damage to the product.
Be sure to use it within the started ratings.

Table 9-1 Absolute Maximum Rating

(Vss = 0 V, Ta = 25°C)

Parameter	Symbol	Rating	Unit
Power supply 1 (1.5V block)	$V_{DD}1$	-0.3 to V_{SS} + 2.0	V
Power supply 2 (2.5V block)	$V_{DD}2$	-0.3 to V_{SS} + 3.5	V
Power supply 3 (3.3V block)	$V_{DD}3$	-0.3 to V_{SS} + 3.9	V
Input voltage 1 (1.5V block)	$V_{IN}1$	-0.3 to V_{DD} + 0.3	V
Input voltage 2 (2.5V block)	$V_{IN}2$	-0.3 to V_{DD} + 0.3	V
Input voltage 3 (3.3V block)	$V_{IN}3$	-0.3 to V_{DD} + 0.3	V
Input voltage 4 (3.3V block, Up to 5V)	$V_{IN}4$	-0.3 to V_{SS} + 5.5	V
Potential difference between supply pins (1.5V block supply voltage pins)	$V_{DG}1$ (*)	0.3	V
Potential difference between supply pins (2.5V block supply voltage pins)	$V_{DG}2$ (*)	0.3	V
Potential difference between supply pins (3.3V block supply voltage pins)	$V_{DG}3$ (*)	0.3	V
Potential difference between supply pins (1.5V block > 2.5V block)	$V_{DG}4$ (*)	0.3	V
Potential difference between supply pins (2.5V block > 3.3V block)	$V_{DG}5$ (*)	0.3	V
Power consumption	P_D	4184	mW
Operating temperature	T_{opr}	−40 to 85	°C
Storage temperature	T_{stg}	−55 to 125	°C

(*)**:** For each of 1.5 V and 2.5 V and 3.3 V, system power supply terminal is made into the same voltage.
The maximum potential difference should not exceed rating for all power supply terminals then.
In addition, potential difference between all V_{SS} terminal must be under 0.01 V in this status.

9.1 Allowable power dissipation

If using a temperature higher than Ta = 25°C, reduce by 41.84 mW per 1°C increase.
When Ta = 85°C, maximum power dissipation is 1674 mW.

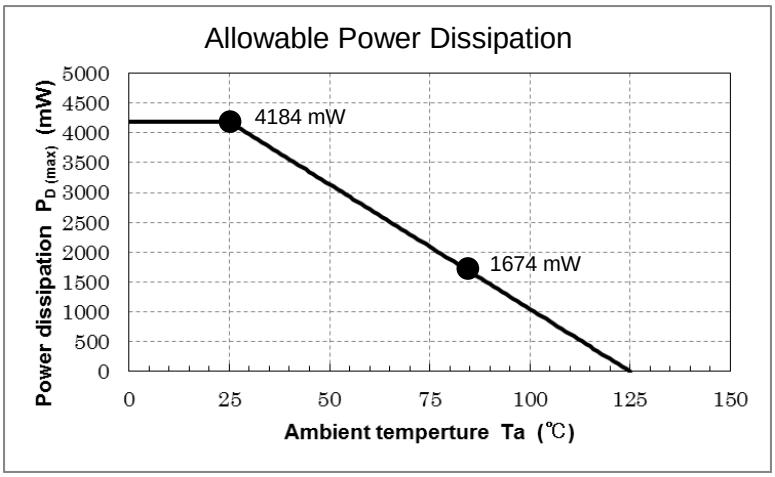


Figure 9-1 Allowable power dissipation

10. Operating Ranges

The product may not operate normally if its rated supply voltage range is exceeded.

Once a rated supply voltage range is exceeded, the product may remain in a condition different from the previous condition even if it gets back to the rated range.

If a rated range is exceed for DRAM, it is necessary to turn the product power off and on again.

Table 10-1 Operating Ranges

Parameter	Symbol	Min	Typ.	Max	Unit
Digital block supply voltage	V_{DD}-D	1.4	1.5	1.6	V
DRAM block supply voltage	V_{DD}-1.5DRAM	1.4	1.5	1.6	V
	V_{DD}-2.5DRAM	2.3	2.5	2.7	V
Analog block supply voltage	V_{DD}-MADC	2.3	2.5	2.7	V
	V_{DD}-SADC				
	V_{DD}-ADC Logic				
	V_{DD}-DSEP				
	V_{DD}-DAC				
XO block supply voltage	V_{DD}-XTAL	2.3	2.5	2.7	V
PLL block supply voltage	V_{DD}-PLL	2.3	2.5	2.7	V
I/O block supply voltage	V_{DD}-IO	3.0	3.3	3.6	V
Operating temperature	T_{opr}	-40	25	85	°C

Caution

When using the product at 85°C, be sure to keep the total power consumption for the power supply within 1674 mW.

Be careful especially for I/O block output pins. Their current varies depending on the state the load.

The current of the 3.3 V block power supply stand in “11. Electrical Characteristic” is applicable to a specific load and presented for reference purposes.

11. Electrical characteristics

Table 11-1 Electrical characteristics

($V_{DD}1$ = 1.5 V, $V_{DD}2$ = 2.5 V, $V_{DD}3$ = 3.3 V, Ta = 25 °C)

Parameter	Corresponding pin number	Symbol	Min	Typ.	Max	Unit	Remarks
Power supply current	VDD-D, VDD-1.5DRAM	$I_{DD}1$	127	152	177	mA	Total current of 1.5 V block supply voltage pin.
	VDD-2.5DRAM	$I_{DD}2$	2	4	6		Total current of 2.5 V DRAM block supply voltage pin.
	VDD-MADC, VDD-SADC, VDD-ADC Logic, VDD-DSEP, VDD-DAC, VDD-XTAL, VDD-PLL	$I_{DD}3$	75	95	115		Total current of 2.5 V Analog block supply voltage pin.
	VDD-IO	$I_{DD}4$	45	55	65		Total current of 3.3 V block supply voltage pin. (*)
Input voltage	A1, A2 A3, B1, B2, B3, C1, C2, C4, D1, D2, D4, E1, E2, E4, F1, F2, F13, G1, G2, G11, G12, G13, H1, H2, H11, H12, J1, J2, K1, K2, M3, N1, N2, N3, P2, R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, T1, T2, T3, T4, T5, T6, T7, T8, T9, T10, T11	V_{IH}	$V_{DD}3$ ×0.8	—	$V_{DD}3$	V	3.3 V block I/O input pin.
	L1, L2, M1, M2, P1						5 V withstand voltage I/O input pin.
Input voltage	A1, A2 A3, B1, B2, B3, C1, C2, C4, D1, D2, D4, E1, E2, E4, F1, F2, F13, G1, G2, G11, G12, G13, H1, H2, H11, H12, J1, J2, K1, K2, M3, N1, N2, N3, P2, R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, T1, T2, T3, T4, T5, T6, T7, T8, T9, T10, T11	V_{IL}	V_{SS}	—	$V_{DD}3$ ×0.2		3.3 V block I/O input pin.
	L1, L2, M1, M2, P1						5 V withstand voltage I/O input pin.
Input current	A1, A2 A3, B1, B2, B3, C1, C2, C4, D1, D2, D4, E1, E2, E4, F1, F2, F13, G1, G2, G11, G12, G13, H1, H2, H11, H12, J1, J2, K1, K2, M3, N1, N2, N3, P2, R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, T1, T2, T3, T4, T5, T6, T7, T8, T9, T10, T11	I_{IH}	-10	—	10	µA	3.3 V block I/O input pin.
	L1, L2, M1, M2, P1						5 V withstand voltage I/O input pin.
Input current	A1, A2 A3, B1, B2, B3, C1, C2, C4, D1, D2, D4, E1, E2, E4, F1, F2, F13, G1, G2, G11, G12, G13, H1, H2, H11, H12, J1, J2, K1, K2, M3, N1, N2, N3, P2, R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, T1, T2, T3, T4, T5, T6, T7, T8, T9, T10, T11	I_{IL}	-10	—	10		3.3 V block I/O input pin.
	L1, L2, M1, M2, P1						5 V withstand voltage I/O input pin.
Output voltage	A4, A5, A6, A7, A8, A9, A10, A11, A12, A13, A14, A15, A16, B4, B5, B6, B7, B8, B9, B10, B11, B12, B13, B14, B15, B16, C14, C15, C16, D14, D15, D16, E15, E16, F14, F15, F16, G14, G15, G16	V_{OH}	$V_{DD}3$ -0.6	—	$V_{DD}3$	V	3.3V block I/O output pin, with 4mA source load. (For A16pin (CPH Out), with 8mA source load.)
Output voltage	A4, A5, A6, A7, A8, A9, A10, A11, A12, A13, A14, A15, A16, B4, B5, B6, B7, B8, B9, B10, B11, B12, B13, B14, B15, B16, C14, C15, C16, D14, D15, D16, E15, E16, F14, F15, F16, G14, G15, G16	V_{OL}	V_{SS}	—	0.4		3.3 V block I/O output pin, with 4 mA sink load. (For A16 pin (CPH Out), with 8 mA sink load.)
	L1, M2						5 V withstand voltage I/O input pin, with 4 mA sink load.

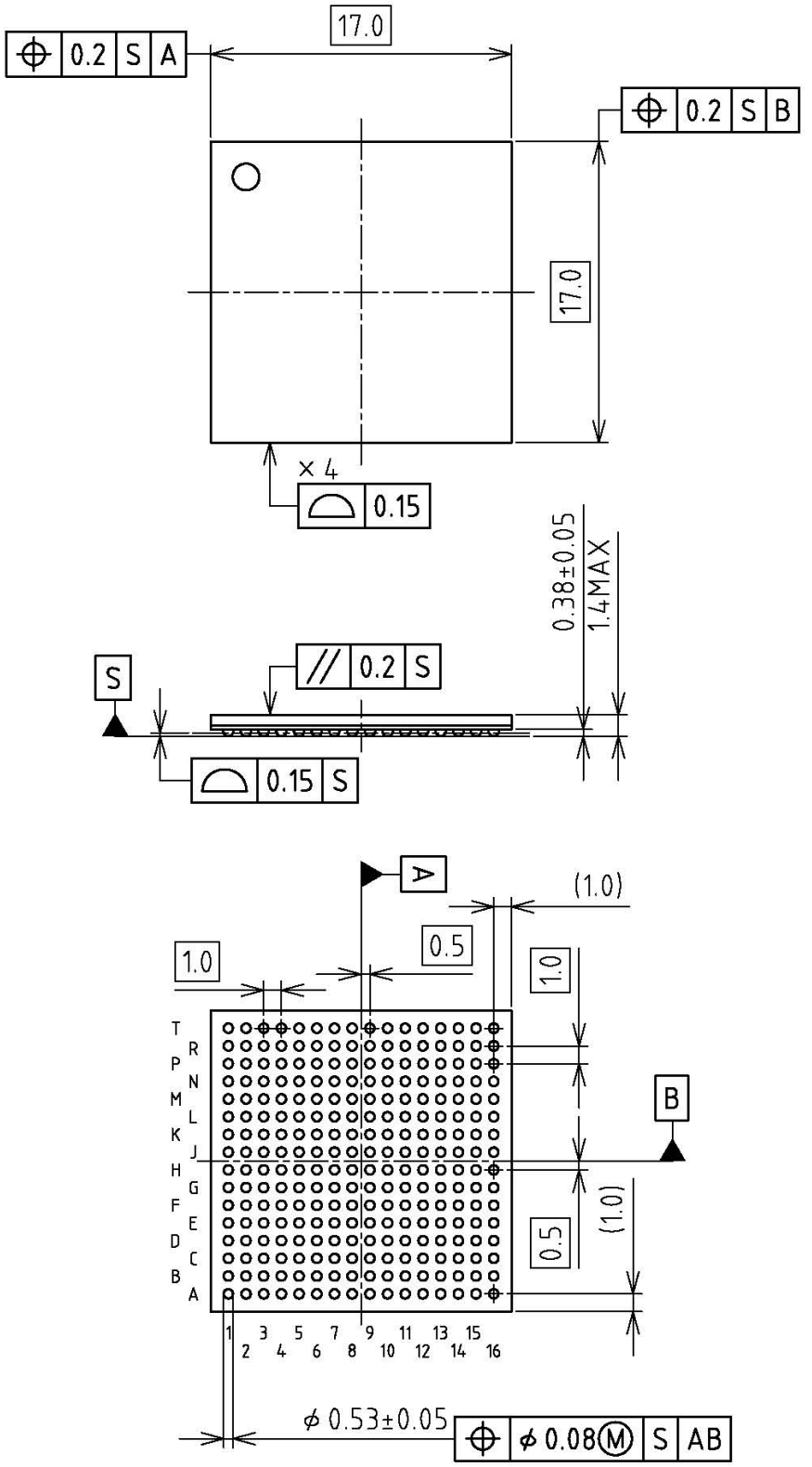
Caution**:** If the total power supply power consumption exceeds 1674 mW, the product cannot satisfy the thermal tolerance for 85°C.

(*)**:** The current required by the 3.3 V block varies depending on the connected display images and load.

12. Package

12.1 Dimensions

P-LBGA256-1717-1.00-001 Unit: mm



Weight: 0.63 g (typ.)

13. Revision History

Date	Revision	Contents
2016/01/21	1.00	First edition

RESTRICTIONS ON PRODUCT USE

- Toshiba Corporation, and its subsidiaries and affiliates (collectively "TOSHIBA"), reserve the right to make changes to the information in this document, and related hardware, software and systems (collectively "Product") without notice.
- This document and any information herein may not be reproduced without prior written permission from TOSHIBA. Even with TOSHIBA's written permission, reproduction is permissible only if reproduction is without alteration/omission.
- Though TOSHIBA works continually to improve Product's quality and reliability, Product can malfunction or fail. Customers are responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of Product could cause loss of human life, bodily injury or damage to property, including data loss or corruption. Before customers use the Product, create designs including the Product, or incorporate the Product into their own applications, customers must also refer to and comply with (a) the latest versions of all relevant TOSHIBA information, including without limitation, this document, the specifications, the data sheets and application notes for Product and the precautions and conditions set forth in the "TOSHIBA Semiconductor Reliability Handbook" and (b) the instructions for the application with which the Product will be used with or for. Customers are solely responsible for all aspects of their own product design or applications, including but not limited to (a) determining the appropriateness of the use of this Product in such design or applications; (b) evaluating and determining the applicability of any information contained in this document, or in charts, diagrams, programs, algorithms, sample application circuits, or any other referenced documents; and (c) validating all operating parameters for such designs and applications. **TOSHIBA ASSUMES NO LIABILITY FOR CUSTOMERS' PRODUCT DESIGN OR APPLICATIONS.**
- **PRODUCT IS NEITHER INTENDED NOR WARRANTED FOR USE IN EQUIPMENTS OR SYSTEMS THAT REQUIRE EXTRAORDINARILY HIGH LEVELS OF QUALITY AND/OR RELIABILITY, AND/OR A MALFUNCTION OR FAILURE OF WHICH MAY CAUSE LOSS OF HUMAN LIFE, BODILY INJURY, SERIOUS PROPERTY DAMAGE AND/OR SERIOUS PUBLIC IMPACT ("UNINTENDED USE"). ** Except for specific applications as expressly stated in this document, Unintended Use includes, without limitation, equipment used in nuclear facilities, equipment used in the aerospace industry, medical equipment, equipment used for automobiles, trains, ships and other transportation, traffic signaling equipment, equipment used to control combustions or explosions, safety devices, elevators and escalators, devices related to electric power, and equipment used in finance-related fields. **IF YOU USE PRODUCT FOR UNINTENDED USE, TOSHIBA ASSUMES NO LIABILITY FOR PRODUCT.** For details, please contact your TOSHIBA sales representative.
- Do not disassemble, analyze, reverse-engineer, alter, modify, translate or copy Product, whether in whole or in part.
- Product shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable laws or regulations.
- The information contained herein is presented only as guidance for Product use. No responsibility is assumed by TOSHIBA for any infringement of patents or any other intellectual property rights of third parties that may result from the use of Product. No license to any intellectual property right is granted by this document, whether express or implied, by estoppel or otherwise.
- **ABSENT A WRITTEN SIGNED AGREEMENT, EXCEPT AS PROVIDED IN THE RELEVANT TERMS AND CONDITIONS OF SALE FOR PRODUCT, AND TO THE MAXIMUM EXTENT ALLOWABLE BY LAW, TOSHIBA (1) ASSUMES NO LIABILITY WHATSOEVER, INCLUDING WITHOUT LIMITATION, INDIRECT, CONSEQUENTIAL, SPECIAL, OR INCIDENTAL DAMAGES OR LOSS, INCLUDING WITHOUT LIMITATION, LOSS OF PROFITS, LOSS OF OPPORTUNITIES, BUSINESS INTERRUPTION AND LOSS OF DATA, AND (2) DISCLAIMS ANY AND ALL EXPRESS OR IMPLIED WARRANTIES AND CONDITIONS RELATED TO SALE, USE OF PRODUCT, OR INFORMATION, INCLUDING WARRANTIES OR CONDITIONS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ACCURACY OF INFORMATION, OR NONINFRINGEMENT.**
- Do not use or otherwise make available Product or related software or technology for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). Product and related software and technology may be controlled under the applicable export laws and regulations including, without limitation, the Japanese Foreign Exchange and Foreign Trade Law and the U.S. Export Administration Regulations. Export and re-export of Product or related software or technology are strictly prohibited except in compliance with all applicable export laws and regulations.
- Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product. Please use Product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. **TOSHIBA ASSUMES NO LIABILITY FOR DAMAGES OR LOSSES OCCURRING AS A RESULT OF NONCOMPLIANCE WITH APPLICABLE LAWS AND REGULATIONS.**