TC78B016FTG
Usage considerations

Rev.2.0

Summary

The TC78B016FTG is a three-phase sine-wave PWM driver for brushless motors. It controls motor rotation speed by changing the PWM duty ratio, based on the speed control input. Hall signal is supported to three sensors.

This is a reference.
Please do not determine the final equipment design by this material.

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1. Power Supply Voltage

The absolute maximum rating of the power supply voltage (VM) is 40 V that must not be exceeded even for a moment. Do not exceed any of these ratings.
Please use the IC within the operation range of the power supply voltage at VM terminal. When the voltage of VM is less than 6 V, the output voltage of VREG sinks and then the IC may malfunction.
Please use the IC within the VM voltage range of 6 V to 30 V.

Table 1 Absolute maximum ratings of power supply voltage (Ta = 25°C)

Characteristic	Symbol	Rating	Unit
Power supply voltage	VM	40	V

Table 2 Power supply voltage usage range

Characteristic	Symbol	Min	Max	Unit
Power supply voltage	VM_{opr}	6	30	V

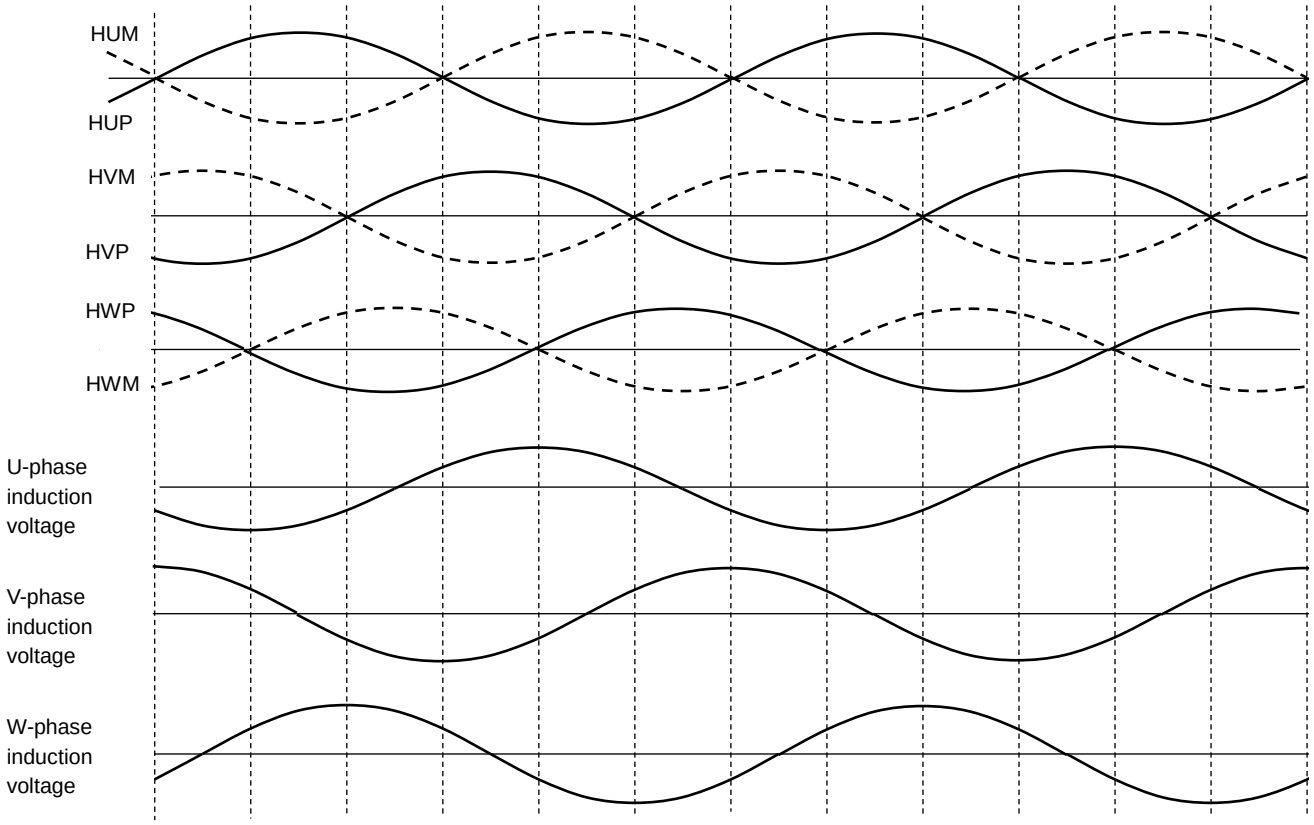
2. Output Current

The absolute maximum rating is 3 A that must not be exceeded, even for a moment. Design an actual application system with the IC so as not to make the inrush current and the lockout current exceed the absolute maximum ratings, especially when a motor starts up and gets stuck in the lockout.
Available average output current changes depending on the usage conditions (ambient temperature, mounting board method, and so on). Design an actual application system with a sufficient margin in order that T_j does not exceed 150°C.

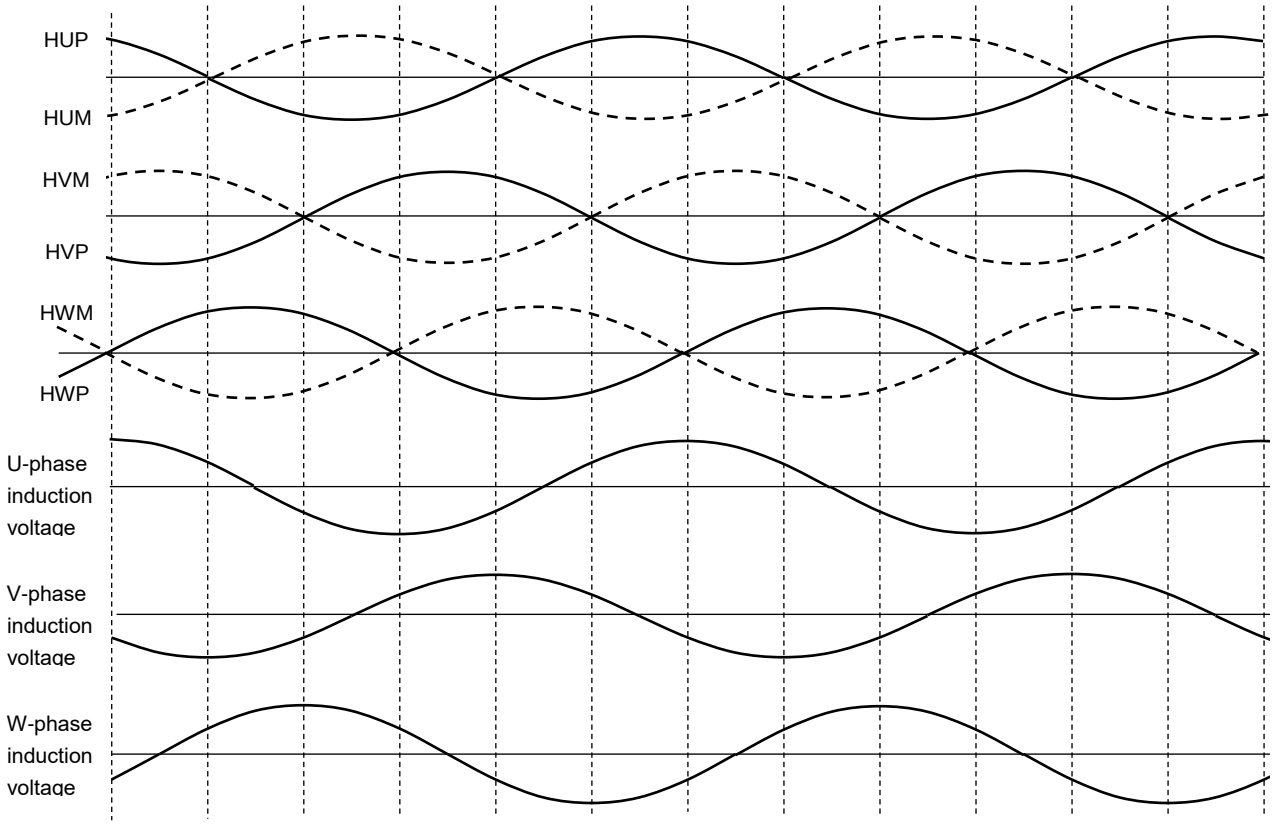
3. Notes in using the motor

Please use the motor whose phase relation between a hall sensor and induction voltage corresponds to the following timing chart.

CW/CCW=L



CW/CCW=H



4. Auto lead angle

Lead angle is controlled by SEL_LA terminal.
When SEL_LA ="2", lead angle is controlled by phase-control system (auto lead angle).
The phase-control system (auto lead angle) makes the phase of the motor current match that of the induction voltage based on the hall signal automatically. This function is able to improve the efficiency of a motor automatically even when the conditions such as the motor rotation speed and the motor current change. Adjust the off-set appropriately, in case the motor efficiency needs being optimized, for example, when there is any misalignment of the hall elements or hall ICs.
Adjust the off-set by the voltage applied to LA terminal in order to minimalize the current as monitoring either the average current of the motor output or the current of the power supply under the same conditions of the rotation speed and the load.

- Default setting: LA=0 (off-set: 0 degree)
- Lead angle adjustment: LA=0 to 3.125 V (off-set: -30 to +30 degree)

5. Application circuit example

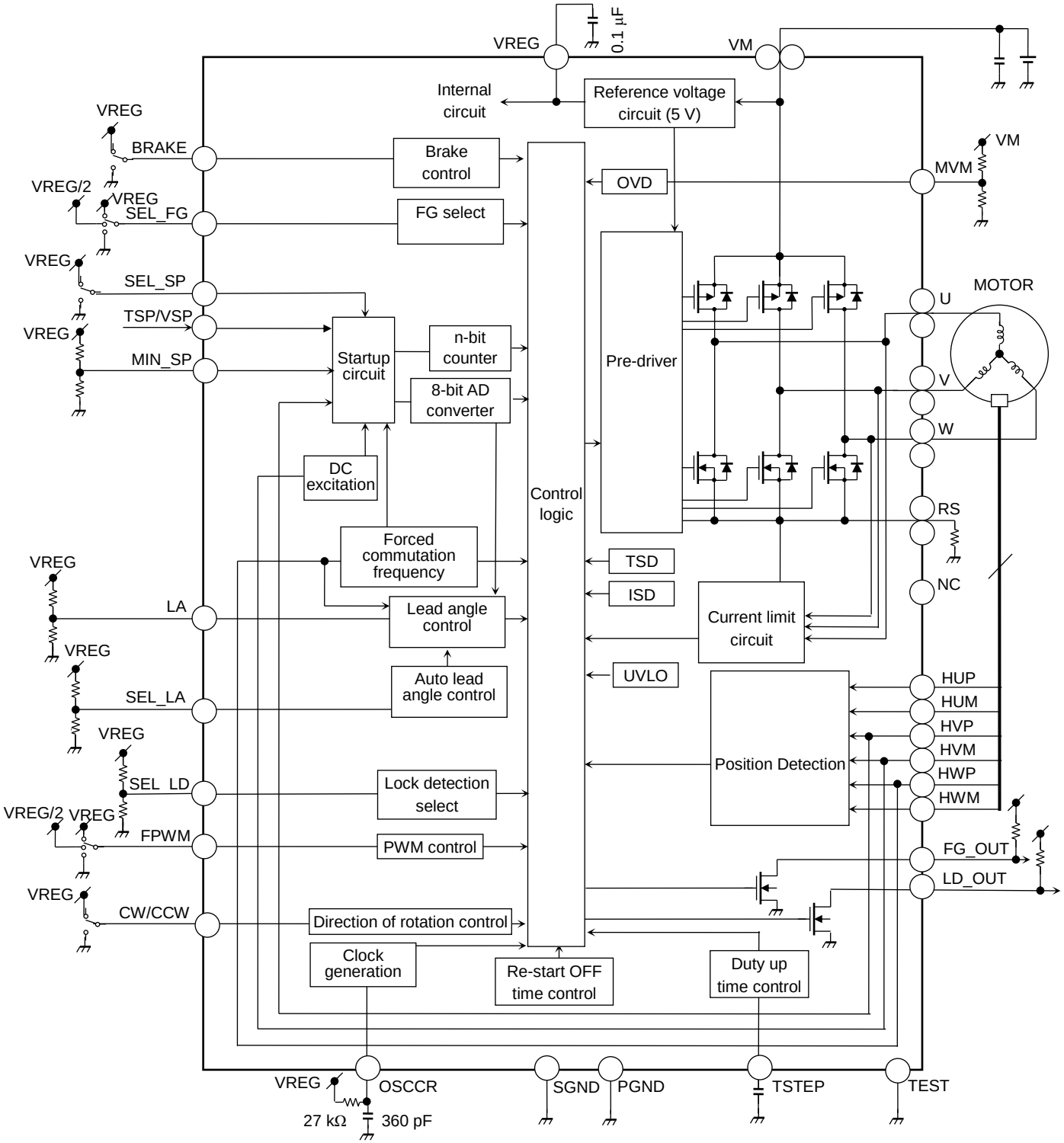


Figure 1 Application circuit example of the TC78B016FTG

(1) Capacitor for VM terminal

Take the VM wiring pattern on a print circuit board widely because large current flows from the power supply to the motor through VM terminal.
Connect an appropriate capacitor between VM terminal and PGND to stabilize the supply voltage and reduce the noise.

Moreover, place the capacitor as close to the IC as possible. In particular, the power supply variation and the noise, which generate at high frequency, can be effectively reduced by connecting ceramic capacitors (0.01 to 1 μF) in parallel near the IC.

Table 3 Capacitor of VM terminal

Item	Parts	Typ.	Recommended range
Between VM and PGND	Ceramic/electrolytic capacitor	10 μF	2.2 to 47 μF

Notes: It is possible using capacitors other than a recommendation value which exclude each part depending on the motor load conditions and the board pattern, etc.

(2) Capacitor for VREG terminal

Please connect the capacitor of 0.1 μF between VREG and SGND as close to the IC as possible in order to reduce the noise and the fluctuation of the voltage at VREG terminal.

Table 4 Capacitor of VREG terminal

Item	Parts	Typ.
Between VREG and SGND	Ceramic capacitor	0.1 μF

(3) Setting OSCCR terminal

OSCCR terminal sets reference oscillating frequency.
Please connect the capacitor of 360 pF between OSCCR terminal and SGND as close to the IC as possible not to be influenced by noise and wiring impedance. Moreover, please connect the resistor of 27 kΩ between OSCCR terminal and VREG as close to the IC as possible. 27 kΩ (typ.) and 360 pF (typ.) should be adopted as an external capacitor and resistor respectively. Please select the resistor and capacitor high-precision as much as possible. When their accuracy is low, the setting time and the frequency might be different from the typical values greatly. Recommended accuracy of the capacitor × resistor is ±30 % or less including the temperature characteristics. (When the accuracy of the capacitor is ±20 %, please apply the resistor whose accuracy is ±5 % or less.)

In addition, internal oscillating frequency can be indirectly checked by measuring the frequency of OSCCR terminal. Internal oscillating frequency and frequency of OSCCR terminal can be gained from the following formula. When internal oscillating frequency is 13 MHz, the frequency of OSCCR terminal is 406.25 kHz.

Internal oscillating frequency [MHz] = Frequency of OSCCR terminal [kHz] × 32 × 1000

(4) Setting RS terminal

Please configure the limit current of the motor output by connecting the detecting resistor between RS terminal and PGND.

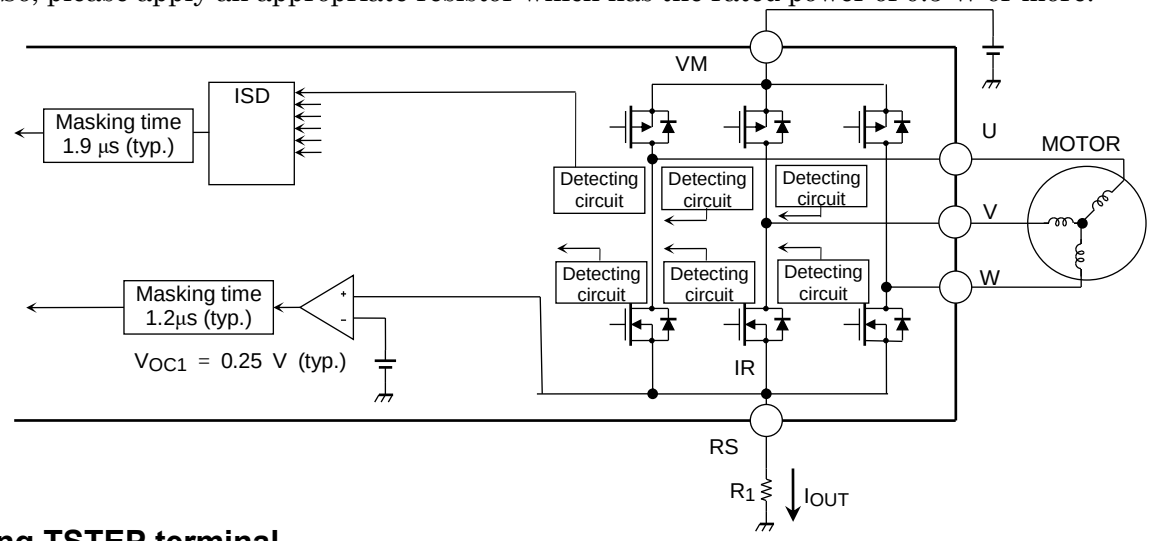
The relation of output current (I_{OUT}) and detecting resistor (R1) is calculated from following formula.

$I_{OUT} = V_{RS} / R_1$

Detecting voltage for over current (V_{RS}): 0.225 V (min), 0.25 V (typ.), and 0.275 V (max)

e.g.) When resistor of R_1 is configured 0.3 Ω, I_{OUT} (typ.) = 0.25 V (typ.)/0.3 Ω ≃ 0.83 A

Please select the external parts with enough margins because high current flows in the detecting resistor (R1). In motor operation, the power on the detecting resistor (P) is calculated as follows; P (max) =0.275 V × 0.275 V/ R_1. For example, when R_1 is 0.3 Ω, then P becomes 0.252 W. So, please apply an appropriate resistor which has the rated power of 0.5 W or more.



(5) Setting TSTEP terminal

Set the time until the duty of input control signal to TSP/VSP terminal is reflected to the output duty during the increase or decrease of the duty of input control signal by connecting the capacitor at TSP/VSP terminal. It controls rapid change of the motor rotation speed.

Please connect the capacitor between TSTEP terminal and SGND to configure the time until the duty of input control signal of TSP/VSP is reflected to the output duty.

When the value of duty command, which is configured by input signal of TSP/VSP terminal, changes, time until the difference of 2.5 % is reflected to the output duty is calculated from following formula.

Reflecting time = $32 \times 0.313 \times C \times 10^6$ [s]

When the external capacitor is 0.01 μF, the reflecting time is about 0.100 s.

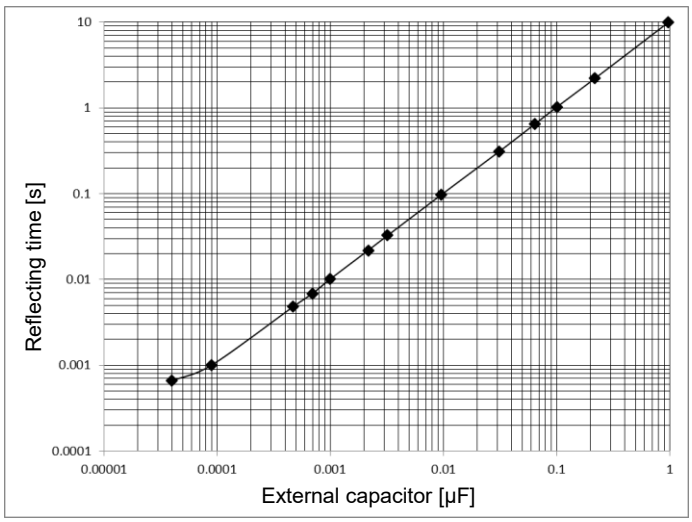


Figure 2 Relation between external capacitor and reflecting time to output duty

(6) Setting FG_OUT and LD_OUT terminals

It is an open-drain output. So, the voltage should be pulled-up by either the external power supply or a pull-up resistor to VREG terminal to output high level.
When pulling up to the VREG terminal, it is recommended to connect the resistor of 1 kΩ to 100 kΩ. When pulling up to the external power supply, do not exceed absolute maximum rating.

(7) Setting TSP/VSP terminal

Please input signal of output PWM duty command. In controlling the analog voltage by setting SEL_SP terminal "2", connect the pull-down resistor between TSP/VSP terminal and SGND externally. It is recommended to connect the pull-down resistor of 10 kΩ to 100 kΩ.

(8) Setting TEST terminal

It is a terminal for shipping test of the IC. Be sure to set to a low level. It is recommended to connect TEST terminal to SGND. It incorporates the pull-down resistor of 100 kΩ. However, in setting it open, it is concerned that the terminal voltage rises rapidly influenced by board wirings. In setting it open unavoidably, please confirm that IC terminal voltage is 0.8 V or less.

(9) Setting CW/CCW terminal

Connect this terminal to VREG terminal and SGND, or input the external control signal. In connecting to VREG terminal, the voltage becomes H level. In connecting to SGND, the voltage becomes L level. Please confirm the voltage of the IC terminal is 0.8 V or less in setting it open unavoidably, though pull-down resistor of 50 kΩ is incorporated.

(10) Setting BRAKE terminal

Connect this terminal to SGND, or input the external control signal. In connecting to SGND, the voltage becomes L level. Please confirm the voltage of the IC terminal is 0.8 V or less in setting it open unavoidably, though pull-down resistor of 50 kΩ is incorporated.

(11) Setting FST, SEL_SP, and SEL_LA terminals

Configure the voltage by resistive dividing voltage between VREG terminal and SGND, or connect these terminals to VREG terminal or GND terminal. In setting them open, the function becomes middle level. So, please evaluate the IC on the actual board enough before setting them open. It is recommended to connect the resistor of 10 kΩ to 100 kΩ between VREG terminal and SGND.

(12) Setting SEL_FG, MIN_SP, LA, FPWM, and SEL_LD terminals

Configure the voltage by resistive dividing voltage between VREG terminal and SGND, or connect it to VREG terminal or GND terminal. It is recommended to connect the resistor of 10 kΩ to 100 kΩ between VREG terminal and SGND.

(13) Setting MVM terminal

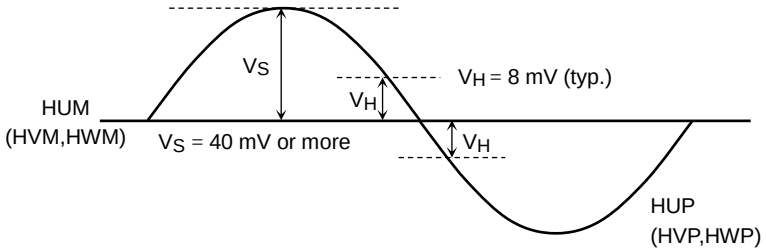
Configure the voltage by resistive dividing voltage between VM terminal and SGND. When this function is not used, please connect it SGND terminal. It is recommended to connect the resistor of about 100 kΩ between VM terminal and SGND.

(14) HUP, HUM, HVP, HVM, HWP, and HWM terminals

Input hall signals to HUP, HUM, HVP, HVM, HWP, and HWM terminals. Select hall elements or hall ICs to provide hall signals. Connect output terminals of U, V, and W, and the hall signal terminals of HUP, HUM, HVP, HVM, HWP, and HWM, to the motor to have the relation shown in the timing chart of "3. Notes in using the motor".

<Notes in using the hall device>

- When 5 V-power supply of VREG supplies power to the hall element, add the limiting resistor to the power supply terminal of the hall element in order to be within the maximum input current of the hall element.
- To recognize switching of the hall signal correctly, the amplitude of the hall device should be 40 mV or more and the input voltage range should be 0.5 V to 3.5 V.
- Hall amplifier has a hysteresis. When the amplitude of it is small, the phase gap of the switching timing becomes large. So, please make the amplitude of it as large as possible.
- When the capacitor for reducing the noise of the hall signal is attached, please arrange it close to HUP and HUM terminals, HVP and HVM terminals, and HWP and HWM terminals. The recommended capacitor is 0.001 µF to 0.1 µF.

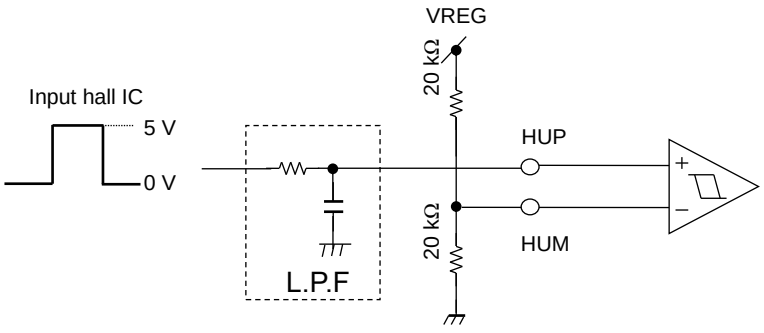


< Notes in using the hall IC>

Please configure HUP, HVP, HWP, HUM, HVM, and HWM as follows;

(1) HUP, HVP, and HWP: Input voltage: H level = VREG, L level = SGND
HUM, HVM, and HWM: Input voltage: VREG/2 * Configure it with resistive dividing voltage between VREG terminal and SGND.

(2) HUP, HVP, and HWP: Input voltage: VREG/2 * Configure it with resistive dividing voltage between VREG terminal and SGND.
HUM, HVM, and HWM: Input voltage: H level = VREG, L level = SGND



*) In case of V phase and W phase are also the same.

(15) Connecting U, V, and W terminals

Connect output terminals of U, V, and W, and the hall signal terminals of HUP, HUM, HVP, HVM, HWP, and HWM, to the motor to have the relation shown in the timing chart of "3. Notes in using the motor".

6. Notes in designing circuit board

In designing board patterns of VM, SGND, and PGND, please pay attention to following notes.

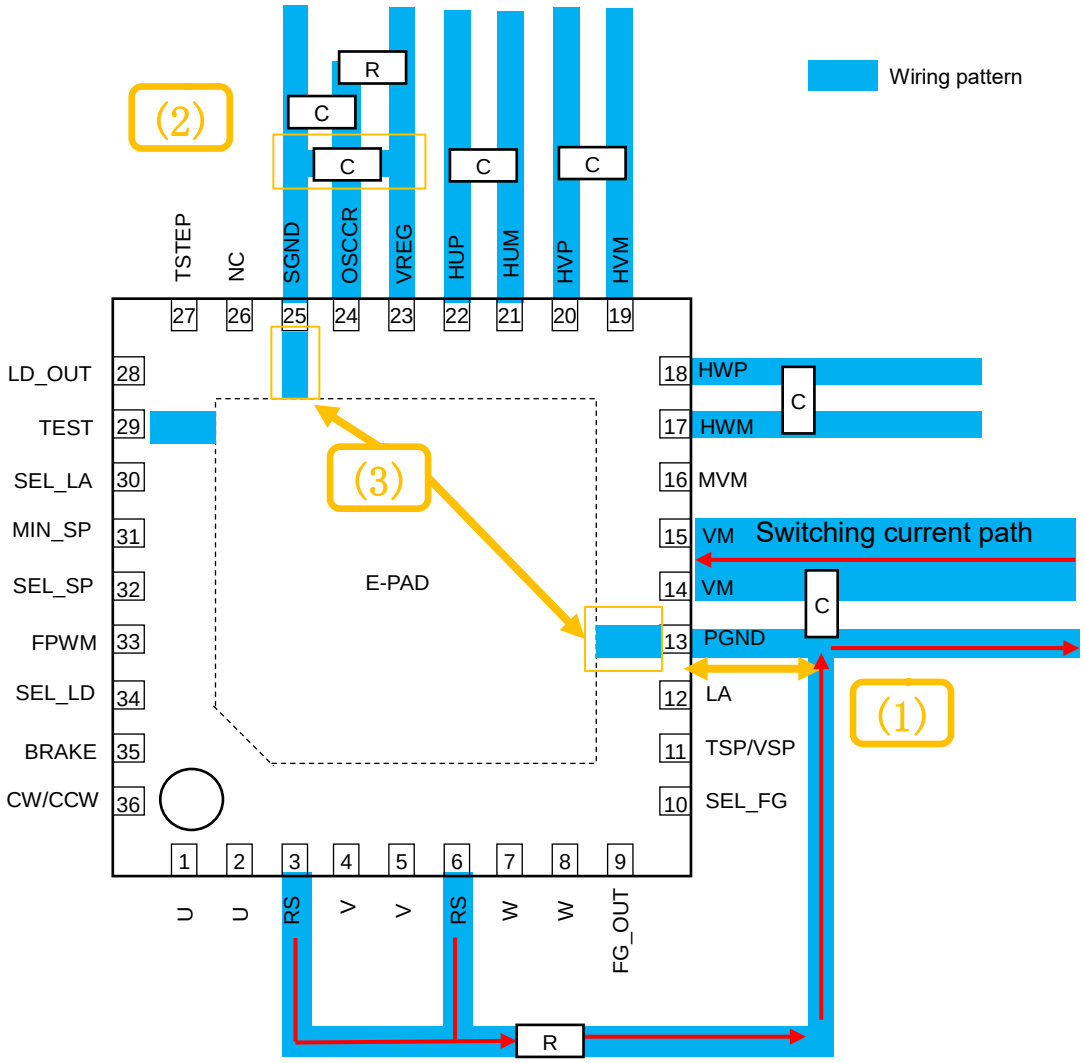
(1) Place the capacitor between VM and PGND close to the IC as possible.
Shorten the wiring length between the capacitor (between VM and PGND) and the IC terminal as much as possible to make wiring impedance low.

(2) Place the capacitor between VREG and SGND close to the IC as possible.
In order to stabilize the VREG voltage, shorten the wiring length between the capacitor (between VREG and SGND) and the IC terminal as much as possible to make wiring impedance low. Especially, shorten the wiring length between the capacitor and SGND terminal to reduce the path for flowing the switching current.

(3)Short-circuit each terminal of PGND and SGND near the IC.
Please refer the example of the following board layout.

<Board layout example >

Layout examples of VM, PGND, SGND, VREG, OSCCR, RS, HUP, HUM, HVP, HVM, HWP, and HWM terminals are shown to simplify the description.



<How to improve IC heat dissipation and reduce generation of heat >

・ Increase the number of thermal Via.
Especially, the heat dissipation improves by arranging the thermal Via on the back of E-PAD of the IC and by increasing the number of thermal via.

・ Enlarge the ratio of wiring cover of the board.
When the ratio of wiring cover of the board is enlarged, the temperature gradient of the board surface is equalized and the heat dissipation improves.

・ Decrease the output current of VREG terminal
When the resistor configured by resistive dividing voltage between VREG and SGND is enlarged and the hall bias power supply is changed from VREG terminal to another power supply, the output current of VREG is decreased and the consumption current of the IC is suppressed. So, generation of heat is reduced.

7. Power consumption

Power of the IC is consumed mainly by the logic block, the internal regulator, and output stages.

P(total) = P(logic) + P(reg) + P(out) ・・・・・・ (Formula 1)

P (total) : Power consumption of IC

P (logic) : Power consumption of logic block

P (reg) : Power consumption of internal regulator

P (out) : Power consumption of output stages

Power consumption of logic block
It can be calculated as follows;
P(logic) = VM × IM ・・・・・・ (Formula 2)

When IM (Typ) =6 mA, IM (Max) =8.5 mA, and VM=12 V, from (Formula 2),
P (logic) Typ=12 V × 6 mA = 0.072 W, and P (logic) Max=12 V × 8.5 mA = 0.102 W

Power consumption of internal regulator
When using Vreg power supply as a power supply of external parts, such as a hall device, the power consumption of an internal regulator can be calculated as follows.

$P(reg) = (VM - VREG) \times I_{VREG}$ ・・・・・・ (Formula 3)

When VM=12 V, I_{VREG}=15 mA (typ.), from (Formula 3), P (reg) = (12 V-5 V) × 15 mA = 0.105 W

Power consumption of the output stages
It is calculated as follows;
$P(out) = Iout(RMS)2 \times R_{ON}(H+L) \times 1.5$ ・・・・・・ (Formula 4)

R_{ON} (H+L) Typ=0.25 Ω, and R_{ON} (H+L) Max=0.33 Ω,
When RMS value (Iout (RMS)) of the phase current of the motor is 1 A,
P (out) Typ = 1 A^2 × 0.25 Ω × 1.5 = 0.375 W, and
P (out) Max = 1 A^2 × 0.33 Ω × 1.5 = 0.495 W
Power consumption of the output stages depends on the conditions, such as the output peak current, output duty, and so on. Above formulas are examples of calculations.

IC power consumption
When I_{VREG}=15 mA (typ.) and Iout (RMS) =1 A, the IC power consumption is gained from (Formula 1), (Formula 2), (Formula 3), and (Formula 4) as follows;
P (total) Typ = P (logic) + P (reg) + P (out) = 0.072 W+0.105 W+0.375 W=0.552 W
P (total) Max = P (logic) + P (reg) + P (out) = 0.102 W+0.105 W+0.495 W=0.702 W

8. Power dissipation

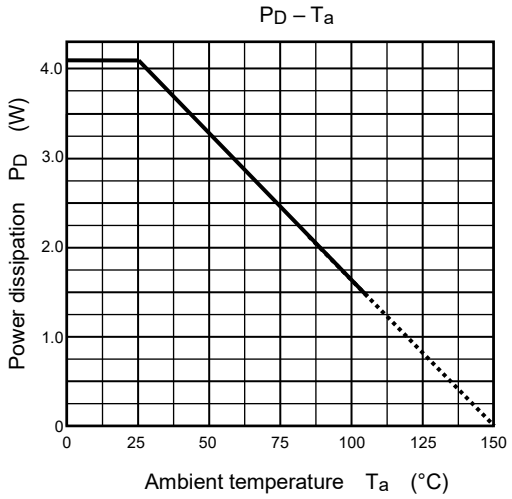
The relation of the ambient temperature (T_a), the junction temperature (T_j), and the heat resistance ($R_{th\ (j\text{-}a)}$) between the ambient temperature and the junction is as follows.

$T_j = T_a + P_{(total)} \times R_{th\ (j\text{-}a)}$

For example, Ta=40[°C], and P (total) =0.702[W],
When $R_{th\ (j\text{-}a)}$ = 30.5[°C/W] (board conditions: 4-layer FR4, 76.2 mm × 114.3 mm × 1.6 mm),
Tj = 40[°C] +0.702 W × 30.5°C/W = 61.411[°C]

The absolute maximum rating of junction temperature (T_j) is 150℃. Permissible power consumption ($P_{(total)}$) depends on T_a and $R_{th\ (j\text{-}a)}$. When ambient temperature is high, permissible power consumption becomes small accordingly. When heat resistance is high, permissible power consumption becomes small accordingly.

(Reference) Relation of power dissipation and ambient temperature
In mounting on board (4-layer FR4 board, 76.2 mm × 114.3 mm × 1.6 mm) $R_{th\ (j\text{-}a)}$ = 30.5°C/W



9. Land pattern dimensions (for reference only)

P-WQFN36-0505-050-001

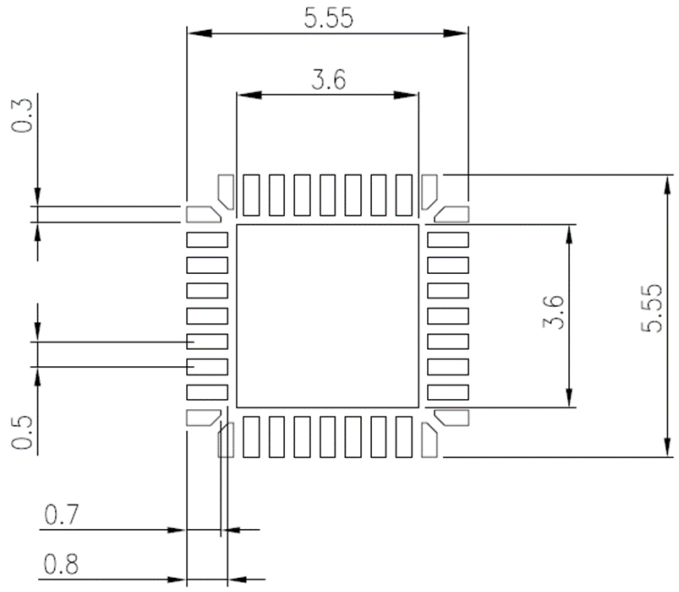


Figure 3 Land pattern dimensions (for reference only): P-WQFN36-0505-050-001

On the actual designing of the PCB, please consider below conditions enough and decide the optimum pattern.
- Solder bridge
- Solder joint strength
- Pattern accuracy when board is produced
- Heat radiation from lead consideration
- Installing accuracy of the machine equipped with IC

IC Usage Considerations

Notes on handling of ICs

(1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings. Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.

(2) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

- Points to remember on handling of ICs
  - (1) Over current Protection Circuit

    Over current protection circuits (referred to as current limiter circuits) do not necessarily protect ICs under all circumstances. If the over current protection circuits operate against the over current, clear the over current status immediately.

    Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the over current protection circuit to not operate properly or IC breakdown before operation. In addition, depending on the method of use and usage conditions, if over current continues to flow for a long time after operation, the IC may generate heat resulting in breakdown.

  - (2) Thermal Shutdown Circuit

    Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over temperature, clear the heat generation status immediately.

    Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the thermal shutdown circuit to not operate properly or IC breakdown before operation.

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