TB67S158
Usage considerations

Summary

The TB67S158 is a two-phase unipolar stepping motor driver of a PWM chopping type. Fabricated with the BiCD process, rating is 80V/1.5A.

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1. Power supply voltage

1.1. Power supply voltage and usage range

In using the TB67S158, the voltage should be applied to the terminals of VM, and VREF.
The maximum rating of VM supply voltage is 80 V. Operating range of the power supply voltage is 10 to 60 V.

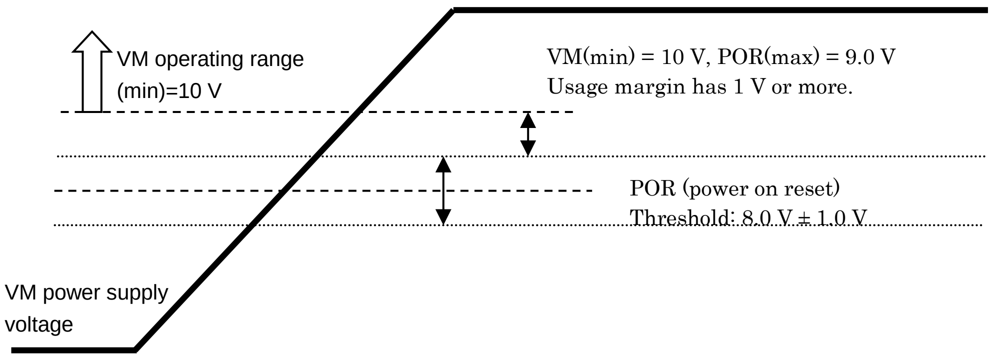


Figure 1.1 Power supply voltage and usage range

1.2. Power supply sequence

There are no special procedures of inputting a power supply and shutdown because the TB67S158 incorporates the power on reset (POR). However, under the unstable state of inputting the power supply (VM) and shutdown, it is recommended to turn off the motor operation. Please operate the motor by switching the input signal after the power supply becomes in the stable state.

2. Output current

Motor usage current should be 1.5 A or less. The maximum current of the actual usage is limited depending on the usage conditions (the ambient temperature, the wiring pattern of the board, the radiation path, and the exciting design). Configure the most appropriate current value after calculating the heat and evaluating the board under the operating environment.

3. Control input

When the logic input signal is inputted under the condition that the voltage of VM is not supplied, the electromotive force by inputting signal is not generated. However, configure the input signal low level before the power supply is applied by referring to the description of the "1.2 Power supply voltage."

4. Function explanation

MODE pin function

MODE	Function	
L	Mode1	Full parallel control I/F (Similar operation of transistor array)
H	Mode2	Serial/parallel conversion control I/F

4.1. Pin function of Full pararell control I/F (Mode1)

IN_X pin can control each transistor directly like transistor array.

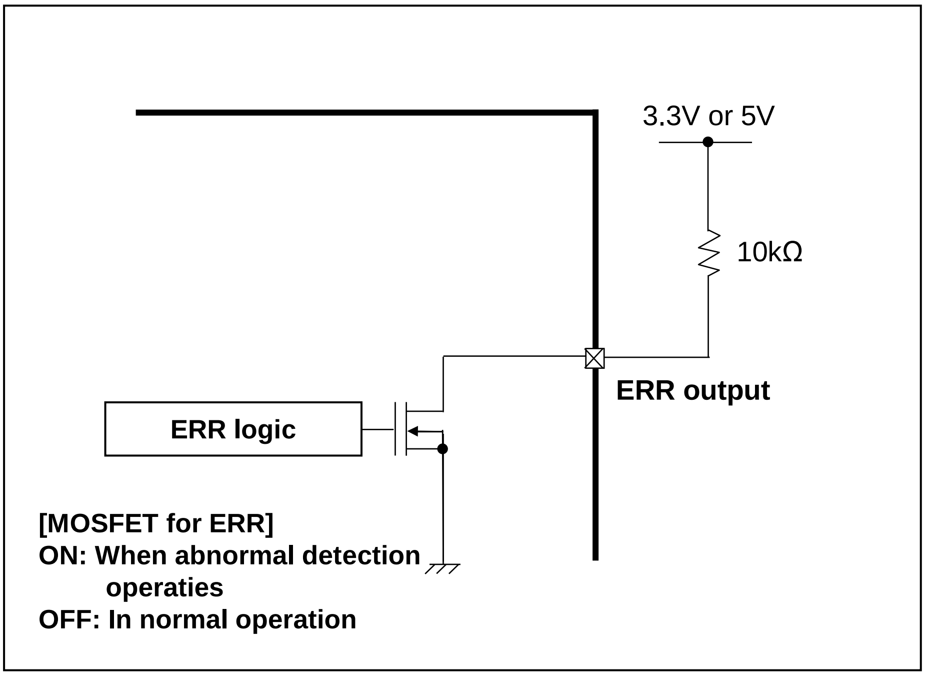
IN_A1	IN_A2	IN_B1	IN_B2	Function
L	-	-	-	OUT_A+=OFF
H	-	-	-	OUT_A+=ON
-	L	-	-	OUT_A-=OFF
-	H	-	-	OUT_A-=ON
-	-	L	-	OUT_B+=OFF
-	-	H	-	OUT_B+=ON
-	-	-	L	OUT_B-=OFF
-	-	-	H	OUT_B-=ON

IN_C1	IN_C2	IN_D1	IN_D2	Function
L	-	-	-	OUT_C+=OFF
H	-	-	-	OUT_C+=ON
-	L	-	-	OUT_C-=OFF
-	H	-	-	OUT_C-=ON
-	-	L	-	OUT_D+=OFF
-	-	H	-	OUT_D+=ON
-	-	-	L	OUT_D-=OFF
-	-	-	H	OUT_D-=ON

4.1.1. ERR function (output function of abnormal detection)

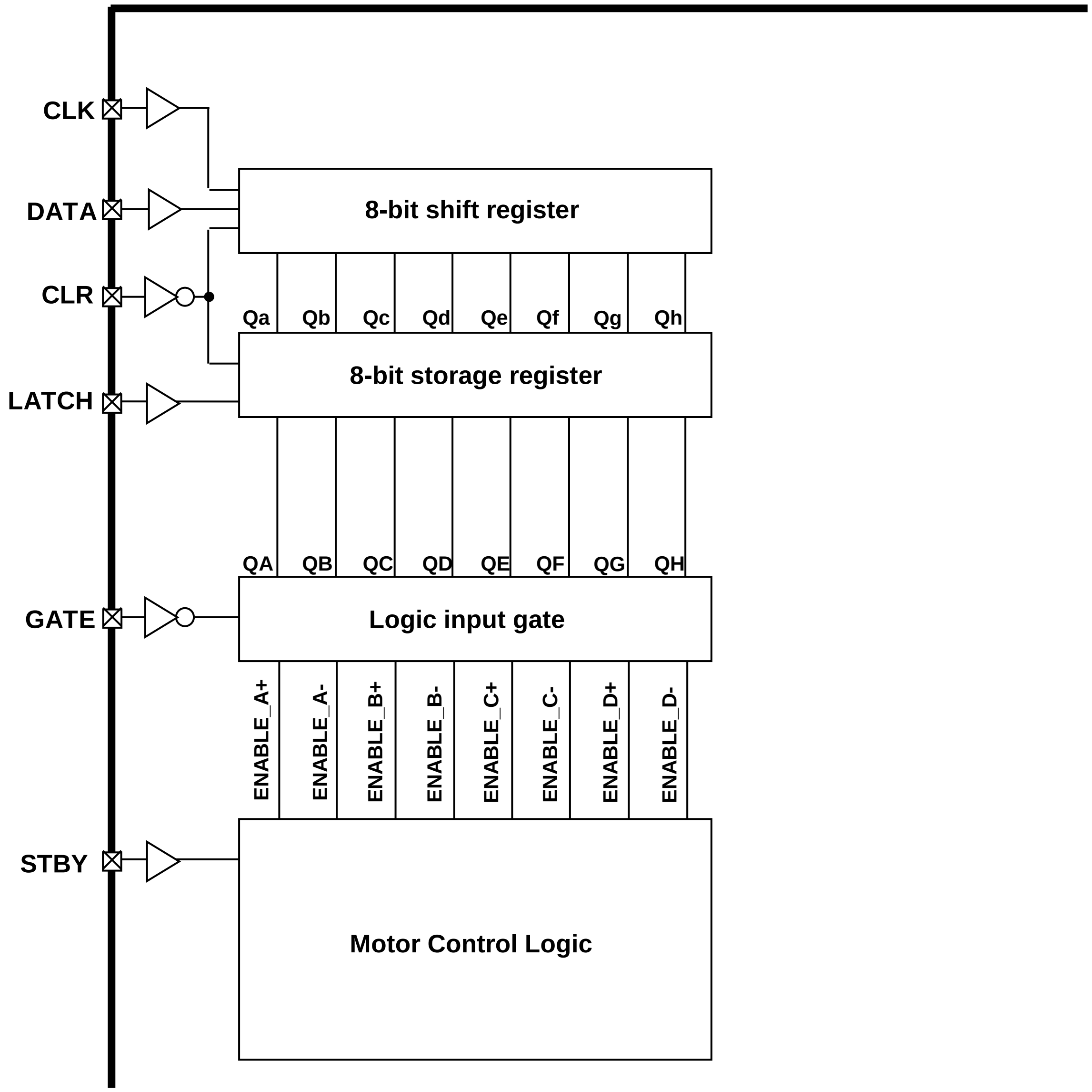
ERR output	Function
H	Normal operation
L	Abnormal detection (TSD or ISD)

ERR pin is a logic output pin of open drain type. It outputs high level (pull-up voltage level) in the normal operation. It outputs low (GND level) when TSD or ISD operates. When TSD or ISD detection is cleared, high level is outputted.



4.2. Pin function of serial/parallel conversion control I/F (Mode2)

4.2.1. Input interface (8-bit shift register + 8-bit storage register)

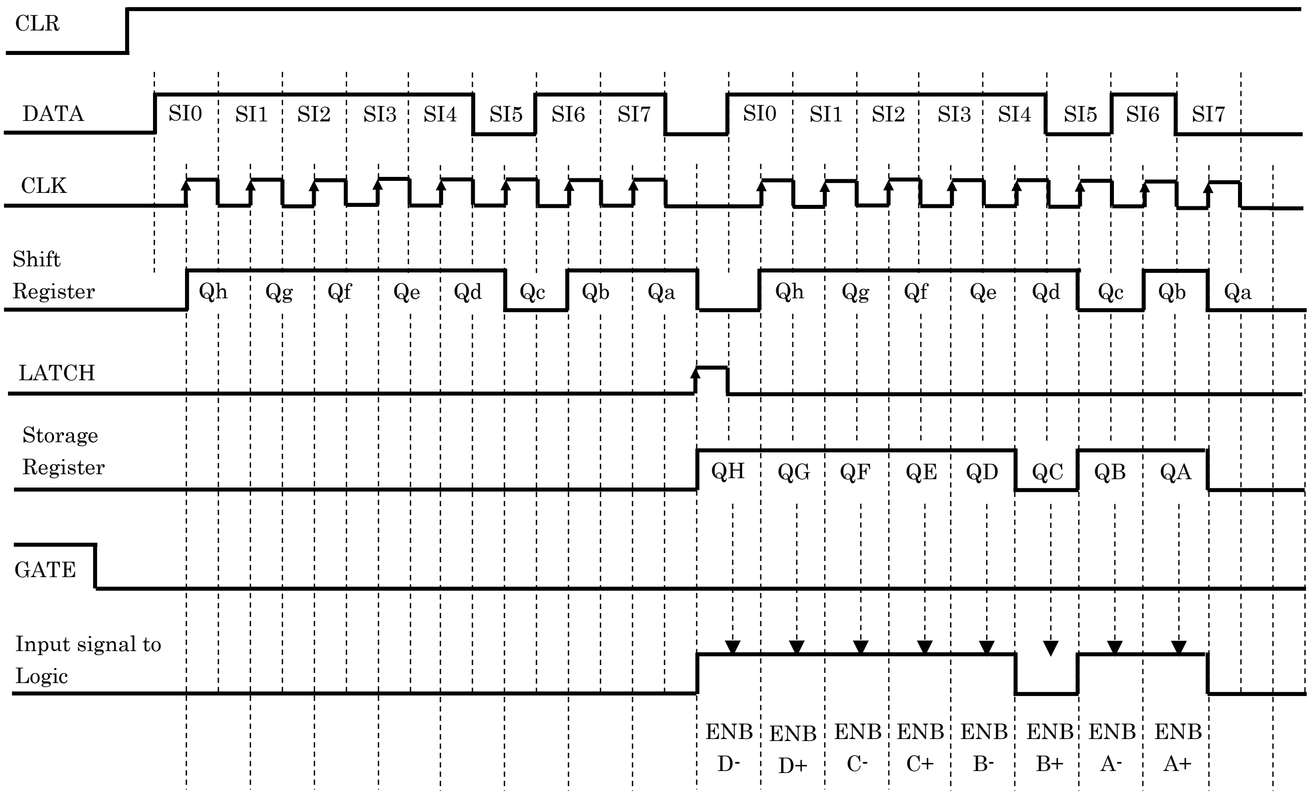


*** Initial value for each logic pin when signal is not inputted**

Pin name	Initial value
CLK	Low
DATA	Low
CLR	Low
LATCH	Low
GATE	High
STBY	Low

Initial state for each logic pin when signal is not inputted is as follows.
LATCH: Low=sift register/storage register: initial state
GATE: High=ENABLE_X+ENABLE_X-=Disable * "X" of ENABLE_X stands for A, B, C, and D.
STBY=Low: standby state

Timing chart of input signal (normal input)



- **Truth value table**

Input					Function
CLK	DATA	CLR	LATCH	GATE	
X	X	X	X	L	Data of ENABLE_X+ and ENABLE_X-: Not applicable
X	X	X	X	H	Data of ENABLE_X+ and ENABLE_X-: Applicable
X	X	L	X	X	Data stored in the storage register is cleared
L	↑	H	X	X	The first step of the shift register: 'L', Others: data of each prior step is stored.
H	↑	H	X	X	The first step of the shift register: 'H', Others: data of each prior step is stored.
X	↓	H	X	X	Shift register keeps prior state.
X	X	H	↑	X	Data of shift register is stored in the storage register.
X	X	H	↓	X	Storage register keeps prior state.

Truth value table: X=Don't care
* "X" of ENABLE_X stands for A, B, C, and D.

* Note: To operate logic output normally, SCK must be configured low in data transfer and complete.

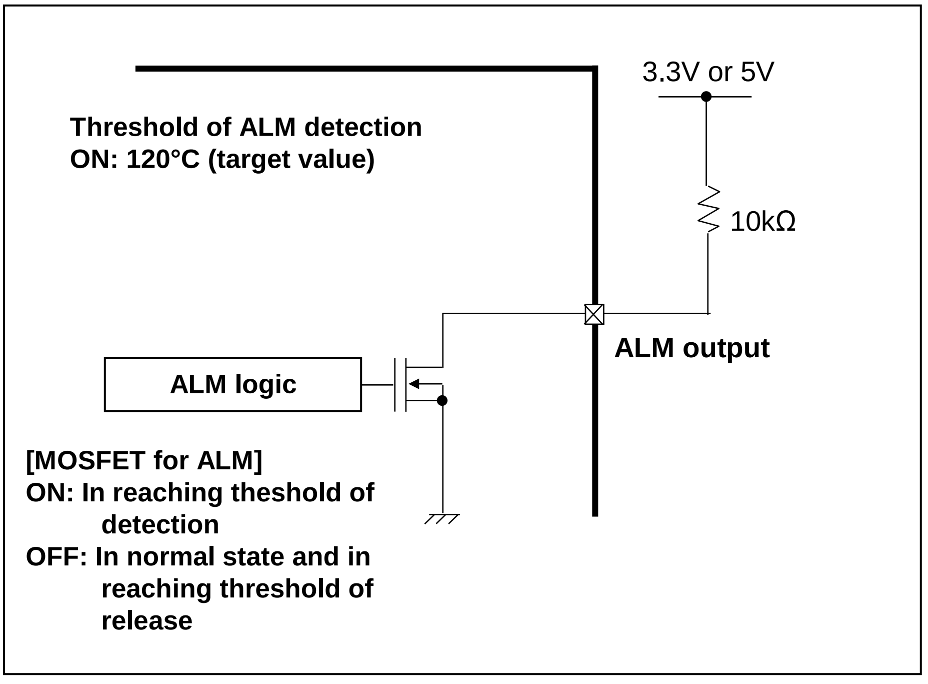
- **Description of logic signal**

Signal name	H	L	Notes
ENABLE_X	Output ON	Output OFF	When ENABLE_x is set low, output of corresponded channel is turned off (Hi-z).
STBY	Motor operation: enable	Turn off all functions of the IC	When STBY is set L, motor output is turned off. (Motor cannot operate).

4.2.2. Function of ALM (output function of thermal shutdown alarm) (Enable in serial/parallel conversion control I/F)

ALM output	Function
H	Normal operation
L	Thermal shutdown alarm function (Thermal_Alarm)

ALM pin is a logic output pin of open drain type. It outputs high (pull-up voltage level) in normal state.
When the temperature of the IC reaches specified threshold (Thermal_Alarm), low level (GND level) is outputted.
Function of ALM is cleared automatically when the temperature of the IC falls 30°C (target value) lower than the threshold of Thermal Alarm.



The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

5. Dead band time of error detection circuits

Dead band time of over current detection circuit

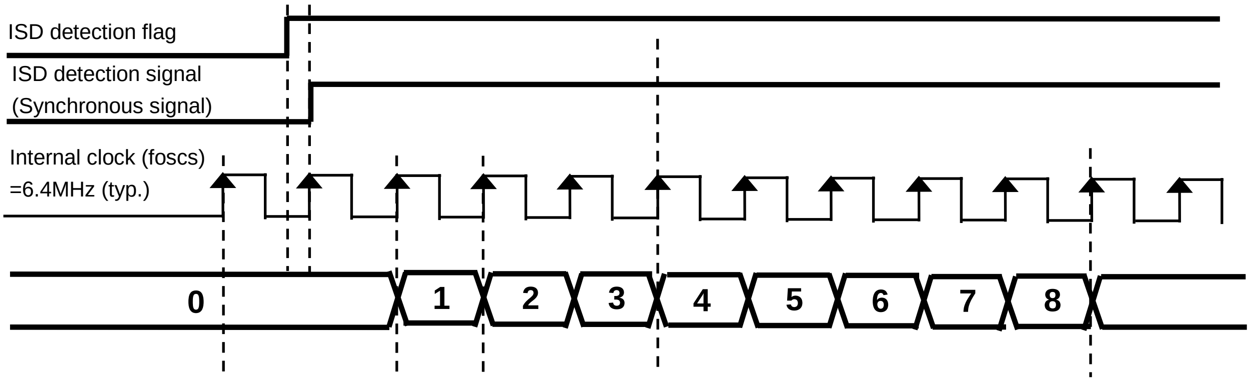


Figure 5.1 Dead band time of over current detection circuit

Timing charts may be omitted for explanatory purpose.

The over current detection circuit has a built-in dead band time to avoid miss-detecting the over current detection due to switching noise or current spikes. The counter for this dead band time is controlled by the internal system clock (foscs=6.4 MHz (typ.)).

* foscs=6.4 MHz (typ.) internal clock
  1/foscs×8 to 9clk worth (1.25μs to 1.4μs)

Note that this detection sequence is an example of an ideal situation when the current flows through the motor continuously, meaning it does not assure the safety of the device at all times. Therefore, to avoid secondary damage of the device, we recommend using a fuse to the VM power line. The proper value of the fuse depends on the operation status, therefore please select the fuse that best fits the operation status.

Dead band time of over thermal detection

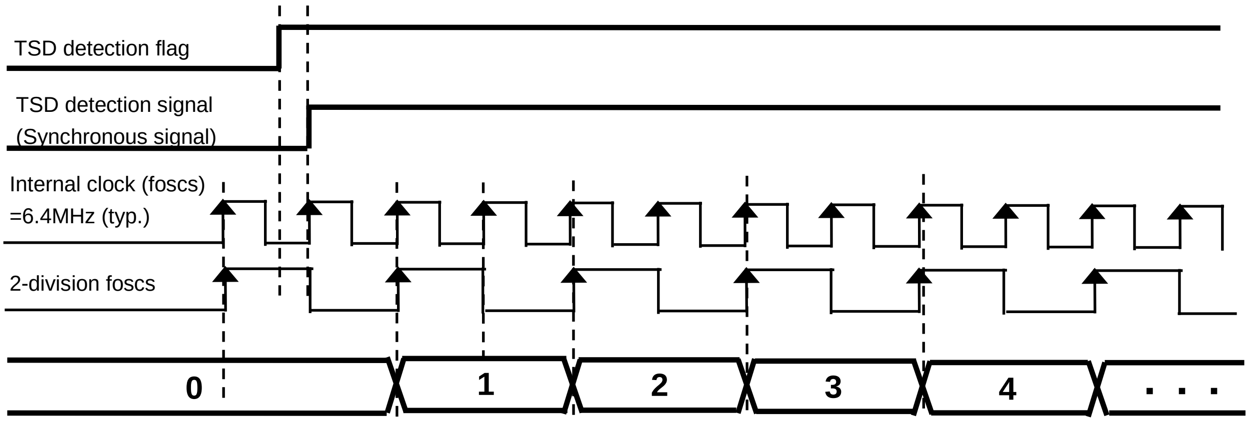


Figure 5.2 Dead band time of over thermal detection

The thermal shutdown circuit has a dead band time to avoid miss detection. The dead band time is to avoid miss detection of the TSD circuit. This dead band time is set by the internal counter (using the system clock).

* foscs=6.4MHz (typ.) internal clock
  1/foscs×32 to 33clk worth (5.0μs to 5.15μs)

6. Power consumption

The power consumption of this device is mainly consumed by the output stage MOSFET and the logic block.

P(total) = P(out) + P(bias)

- Power consumption of the output stage MOSFET
  The power consumption of the output stage is mainly consumed by MOSFET and SBD.

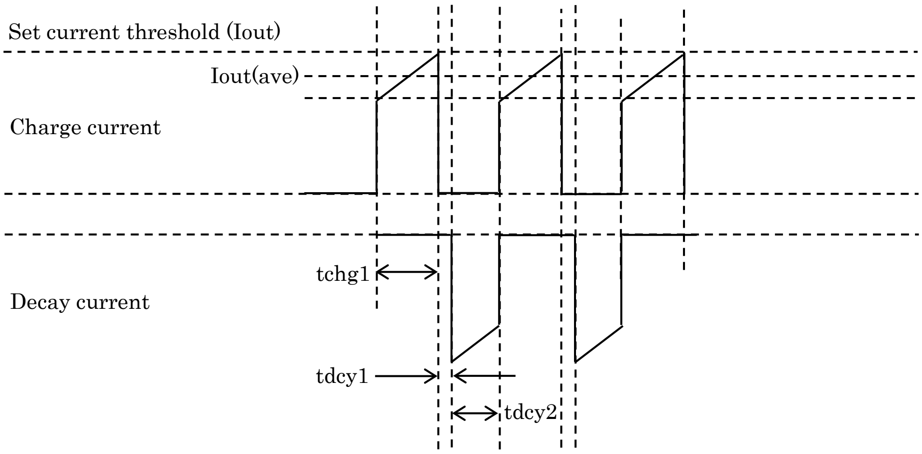


Figure 6.1 Constant current PWM waveform timing chart example

tchg1: Charge sequence (The current will flow from the power source to the motor.)
tdcy1: Mutual induction sequence (From Charge -> Decay)
tdcy2: Decay sequence (The current will flow back from the motor to the power source.)

Calculation variable:

- Motor current(Iout(ave)) = Current setting(Iout) × 0.85 (taking current ripple into consideration)
- Flow through current of the internal common diode(IZD) = 10% of Iout(ave)=Iout(ave) × 0.1
- Output voltage during decay sequence(VOUT)=VM(Motor power supply) + VZD(Zener voltage)
- Setting each sequence duty to tchg1:tdcy1:tdcy2=50%:3%:47% for reference.

From the calculation shown above; Ex: VM=24V, VZD=36V, Iout=1.5A, Full step resolution,

Pout = Pchg1+Pdcy1+Pdcy2
Pchg1 = Iout (ave) ×Iout (ave) ×Ron×H-bridge channel×Duty,
=1.5×0.85×1.5×0.85×0.25×2×0.5=0.406 [W]
Pdcy1=Vout× (IZD) ×H-bridge channel×Duty
= (VM+VZD) × (Iout (ave) ×10%) ×2×0.03
=60×1.5×0.85×0.1×2×0.03=0.459 [W]
Pdcy2=VF×IF×H-bridge channel×Duty,
=1.4×1.5×0.85×2×0.47=1.678 [W]
∴Pout=0.406+0.459+1.678=2.543 [W] → The power consumption of the output stage.

* Note that the average running current will drop to around 71%(1/$\sqrt{2}$, compared to full-step operation) of the set value when using the micro-stepping function.

- Power consumption of the logic block and low power analog block
  (IM2) = 3.0 mA (typ.)

The output block is connected to VM (24V) (the sum total of the consumed current which is consumed by connecting to VM and consumed by switching output channels.)

The power consumption can be calculated as below;

Pbias = 24 (V) × 0.003 (A)= 0.072 (W)

- Total power consumption of the device;
  The total power consumption (Ptotal) of the device can be calculated by adding Pout and Pbias.

Ptotal = Pout + Pbias = 2.543 + 0.072 = 2.615 (W)

Note that the actual power consumption can be different, depending on the current step, slew rate, constant current PWM current ripple, etc.
Therefore, used the calculated value only as a reference, and evaluate the device enough so that the thermal designing can be set with enough margins.

7. Power dissipation

The power dissipation can be calculated by using the ambient temperature (Ta), junction temperature (Tj), and junction-to-case thermal resistance (Rth (j-a)).

Tj = Ta + P × Rth (j-a)

(For example) When mounted to a 4-layer PCB (an assumed Rth (j-a) = 25°C/W), Ta = 25°C, Ptotal = 2.615 W (Iout = 1.5 A, full step resolution)
Tj = 25 (°C) + 25 (°C/W) × 2.615 (W) = 90.38°C

(For reference) Relationship between power dissipation and ambient temperature

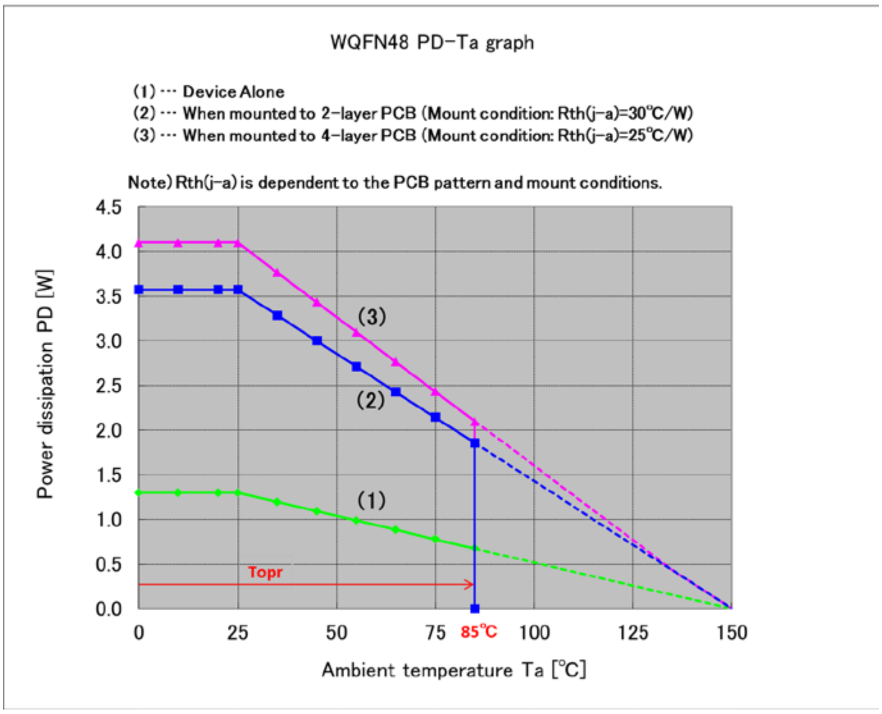


図 8.1 Power dissipation

* Pay attention that Ta, Rth (j-a), and P (total) depend on the usage environment. When ambient temperature is high, the allowable power consumption decreases.

For reference only: QFN48 T (j-c) =3.5°C/W

(1) Capacitor for the VM power supply

To stabilize the voltage of the power supply, and also to reject any incoming noise, we recommend connecting the proper value capacitor to the VM power line (near the device). Especially the ceramic capacitor should be placed near the device as close as possible, to reject high frequency incoming noise.

Table 7.1 Recommended capacitor values for power supply

Item	Parts	Symbol	Typ.	Recommended range
VM-GND	Electrolytic capacitor	CVM1	100 µF	47 to 100 µF
	Ceramic capacitor	CVM2	0.1 µF	0.01 to 1 µF
VCC-GND	Ceramic capacitor	CVCC	0.1 µF	0.01 to 1 µF
VREF-GND	Ceramic capacitor	CVRF	0.1 µF	0.01 to 1 µF

* VREF-GND: The voltage for VREF can be set using a resistance divider from VCC. If you wish to use a voltage divider for VREF, please set the resistance (between VCC and GND) in a range of 10kΩ to 30kΩ.
* The values shown in the table is for reference only, therefore components outside the recommended range can also be used, depending on the motor load condition and the design pattern of the PCB.

(2) Zener diode

This device requires a zener diode between the VM-VCOM pins for the constant current PWM control. The zener diode should also be placed near the device.

Table 7.2 Recommended zener diode values

Item	Parts	Symbol	VM Typ.	Recommended range
VM-VCOM	Zener diode	VZD	10 to 18V	24V
			19 to 27V	36V
			28 to 40V	43V

* The values shown in the table above are for reference only, therefore please decides the proper value with evaluation.

(3) Resistance for Logic output pins

This device has two open-drain type logic output pins (ERR, ALM). When the internal CMOS is OFF, the pin voltage level becomes 'high impedance'. Therefore, in order to use these functions properly, please pull-up the pin to 3.3V or 5.0V power line with a pull-up resistance.

Table 7.3 Recommended pull-up resistance values for logic output pins

Item	Parts	Symbol	Typ.	Recommended range
ERR pull-up resistance	Chip or lead type resistance	RERR	10 kΩ	10 to 100 kΩ
ALM pull-up resistance		RALM		

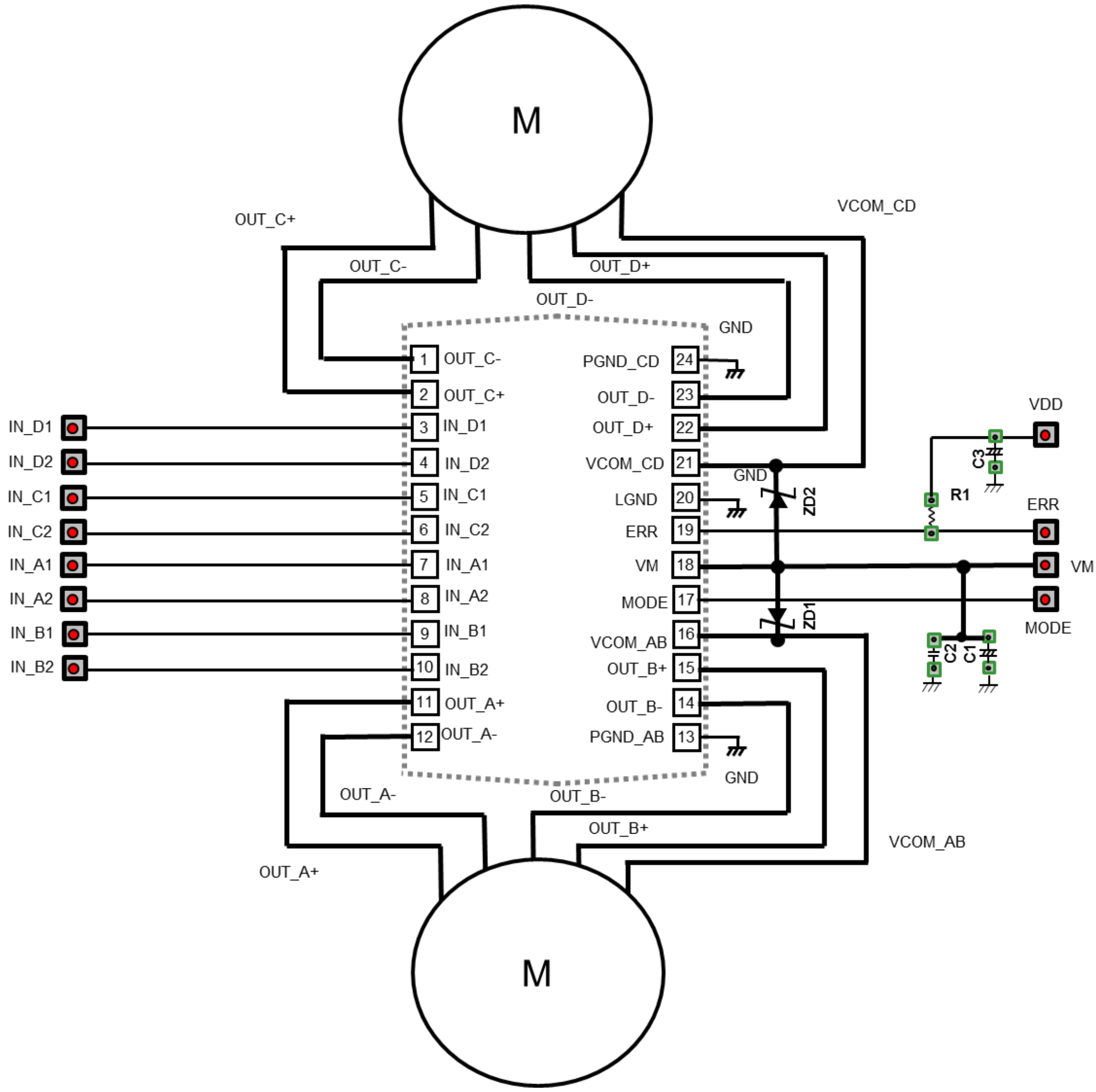
(4) Wiring pattern for power supply and GND

Since large current may flow in VM, OUT, RSGND, and GND pattern especially, design the appropriate wiring pattern to avoid the influence of wiring impedance. It is very important for surface mounting package to radiate the heat from the heat sink of the back side of the IC to the GND. So, design the pattern by considering the heat design.

(5) Fuse

Use an appropriate power supply fuse for the power supply line to ensure that a large current does not continuously flow in the case of over-current and/or IC failure.
The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead to smoke or ignition. To minimize the effects of the flow of a large current in the case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.
This IC incorporates over current detection circuit (ISD) that turns off the output of the IC when over current is detected in the IC. However, it does not necessarily protect ICs under all circumstances. If the Over current detection circuits operate against the over current, clear the over current status immediately. Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the over current protection circuit to not operate properly or IC breakdown before operation. In addition, depending on the method of use and usage conditions, if over current continues to flow for a long time after operation, the IC may generate heat resulting in breakdown.
To avoid above IC destruction and malfunctions caused by noise, the over current detection circuit has a dead band time. So, it is concerned that the over current detection circuit may not operate depending on the output load conditions because of the dead band time. Therefore, in order to avoid continuing this abnormal state, use the fuse for the power supply line.

8. Example of application circuit



The application circuit example is for reference only, and does not guarantee the mass production design of the device.

Figure 8.1 Example of application circuit

9. Example of reference foot pattern

(1) WQFN48 foot pattern

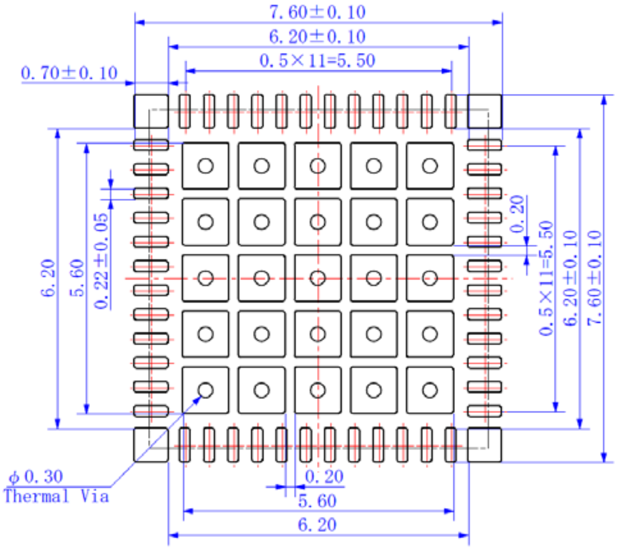


Figure 10.1 WQFN48 foot pattern

Toshiba does not guarantee the data for mass production. Please use the data as reference data for customer's application.
Note: In determining the size of mounting board, design the most appropriate pattern by considering the solder bridge, the solder connecting strength, the pattern accuracy in making board, the heat sink of leads, and the mounting accuracy of the IC board.

Notes on Contents

1. Block diagram
   Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. Equivalent Circuits
   The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

3. Timing Charts
   Timing charts may be simplified for explanatory purposes.

4. Application Circuit
   The application circuits shown in this document are provided for reference purposes only.
   Thorough evaluation is required, especially at the mass production design stage.
   Toshiba does not grant any license to any industrial property rights by providing these examples of application circuits.

IC Usage Considerations

Notes on handling of ICs

(1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings. Exceeding the rating(s) may cause device breakdown, damage or deterioration, and may result in injury by explosion or combustion.

(2) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in the case of overcurrent and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead to smoke or ignition. To minimize the effects of the flow of a large current in the case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

(3) If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition. Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

(4) Do not insert devices in the wrong orientation or incorrectly.
Make sure that the positive and negative terminals of power supplies are connected properly. Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.

(5) Carefully select external components (such as inputs and negative feedback capacitors) and load components (such as speakers), for example, power amp and regulator.
If there is a large amount of leakage current such as input or negative feedback condenser, the IC output DC voltage will increase. If this output voltage is connected to a speaker with low input withstand voltage, overcurrent or IC failure can cause smoke or ignition. (The over current can cause smoke or ignition from the IC itself.) In particular, please pay attention when using a Bridge Tied Load (BTL) connection type IC that inputs output DC voltage to a speaker directly.

Points to remember on handling of ICs

(1) Over current Protection Circuit
Over current protection circuits (referred to as current limiter circuits) do not necessarily protect ICs under all circumstances. If the over current protection circuits operate against the over current, clear the over current status immediately.
Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the over current protection circuit to not operate properly or IC breakdown before operation. In addition, depending on the method of use and usage conditions, if over current continues to flow for a long time after operation, the IC may generate heat resulting in breakdown.

(2) Thermal Shutdown Circuit
Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over temperature, clear the heat generation status immediately.
Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the thermal shutdown circuit to not operate properly or IC breakdown before operation.

(3) Heat Radiation Design
In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (Tj) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into considerate the effect of IC heat radiation with peripheral components.

(4) Back-EMF
When a motor reverses the rotation direction, stops or slows down abruptly, a current flow back to the motor's power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond absolute maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

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