

TB67B001

Usage considerations

Summary

The TB67B001 is a three-phase PWM chopper driver for sensorless brushless motors. It controls motor rotation speed by changing the PWM duty cycle, based on the speed control input.

Packages of WQFN24 and SSOP24 can be chosen. And four patterns of functions is selectable. The TB67B008 is the similar product which miniaturized the TB67B001 and reduced functions.

Table 1 Differences between TB67B001 and TB67B008

	TB67B001	TB67B008
Input terminal for speed command	Selectable of input control by SEL_SP terminal: Analog voltage of TSP/VSP terminal or PWM duty	Input of PWM duty is controlled by TSP terminal.
Output terminal for lock detecting signal Output terminal for rotation speed detecting signal	Capable of outputting both signals by FG_OUT terminal and LD_OUT terminal	Only one signal is outputted depending on the product.
Selecting rotation direction (Forward/Reverse)	Rotation direction is selectable by CW/CCW terminal	No function
Output commutation drive type	6 types of drives (120-degree commutation with and without soft switching, 135-degree commutation with and without soft switching, and 150-degree commutation with and without soft switching) can be selected by SLOP and LAP terminals.	150-degree commutation with soft switching
Input vs. Output Adjusting PWM duty	Three duty adjustments are possible by ADJ0, ADJ1, ADJ2, and ADJ3 terminals.	Two duty adjustments are possible by ADJ0, ADJ1, and ADJ2 terminals.
Selecting lead angle control	18 types are selectable by ROT and LA terminals.	9 types are selectable by LA terminal.
Package	VQFN36	WQFN24 SSOP24

Table 2 Product pattern of the TB67B001

	TB67B001FTG	TB67B001AFTG
Lock detecting signal (LD_OUT)	Normal state: High Abnormal state: Low	Normal state: Low Abnormal state: High

Table 3 Product pattern of the TB67B008

Differences in function	Package (Corresponding terminal number of differences in function)	
	WQFN24 (8PIN)	SSOP24 (23PIN)
Rotation speed detecting signal (FG_OUT) 1ppr(1 pulse/1 electrical angle)	TB67B008FTG	TB67B008FNG
Lock detecting signal (LD_OUT) Normal state: High, Abnormal state: Low	TB67B008AFTG	TB67B008AFNG
Rotation speed detecting signal(FG_OUT) 3ppr (3 pulses/1 electrical angle)	TB67B008BFTG	TB67B008BFNG
Lock detecting signal (LD_OUT) Normal state: Low, Abnormal state: High	TB67B008CFTG	TB67B008CFNG

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1. Power supply

Operating range of the power supply voltage is 4V to 22V. The absolute maximum rating of the power supply voltage is 25V that must not be exceeded, even for a moment. Do not exceed any of these ratings. Please use the IC within the range of the power dissipation.

Please pay attention in using the IC when the voltage of VM is 5.5V or less because the characteristics of the output on resistance and the output voltage of VREG change in this condition.

2. Output current

The absolute maximum rating is 3A. The absolute maximum rating is a set of a rating that must not be exceeded, even for a moment. Do not exceed any of these absolute maximum ratings for the rush current in motor startup and the current in the lock mode.

The average output current shall be increased or decreased depending on usage conditions such as ambient temperature and IC mounting method.

Take enough margins in designing so that the junction temperature of 150°C (Tj) is not exceeded.

3. Rotation speed

Upper limit of the rotation speed (FMAX) is determined by FST terminal. Over this specified value is recognized as an abnormal value.

When FST = High, FMAX = 1.5kHz/1 electrical angle frequency

When FST = Middle, FMAX = 1.5kHz/1 electrical angle frequency

When FST = Low, FMAX = 750Hz /1 electrical angle frequency

In considering the tolerance of the IC, take the margin of about 20% for the upper limit (FMAX).

Reference example:

Upper limit of the rotation speed when FST = High and Middle is as follows;

4-polar motor: 36k [rpm]

8-polar motor: 18k [rpm]

Upper limit of the rotation speed when FST = Low is as follows;

4-polar motor: 18k [rpm]

8-polar motor: 9k [rpm]

Use the IC within this range of the rotation speed.

4. Application circuit example

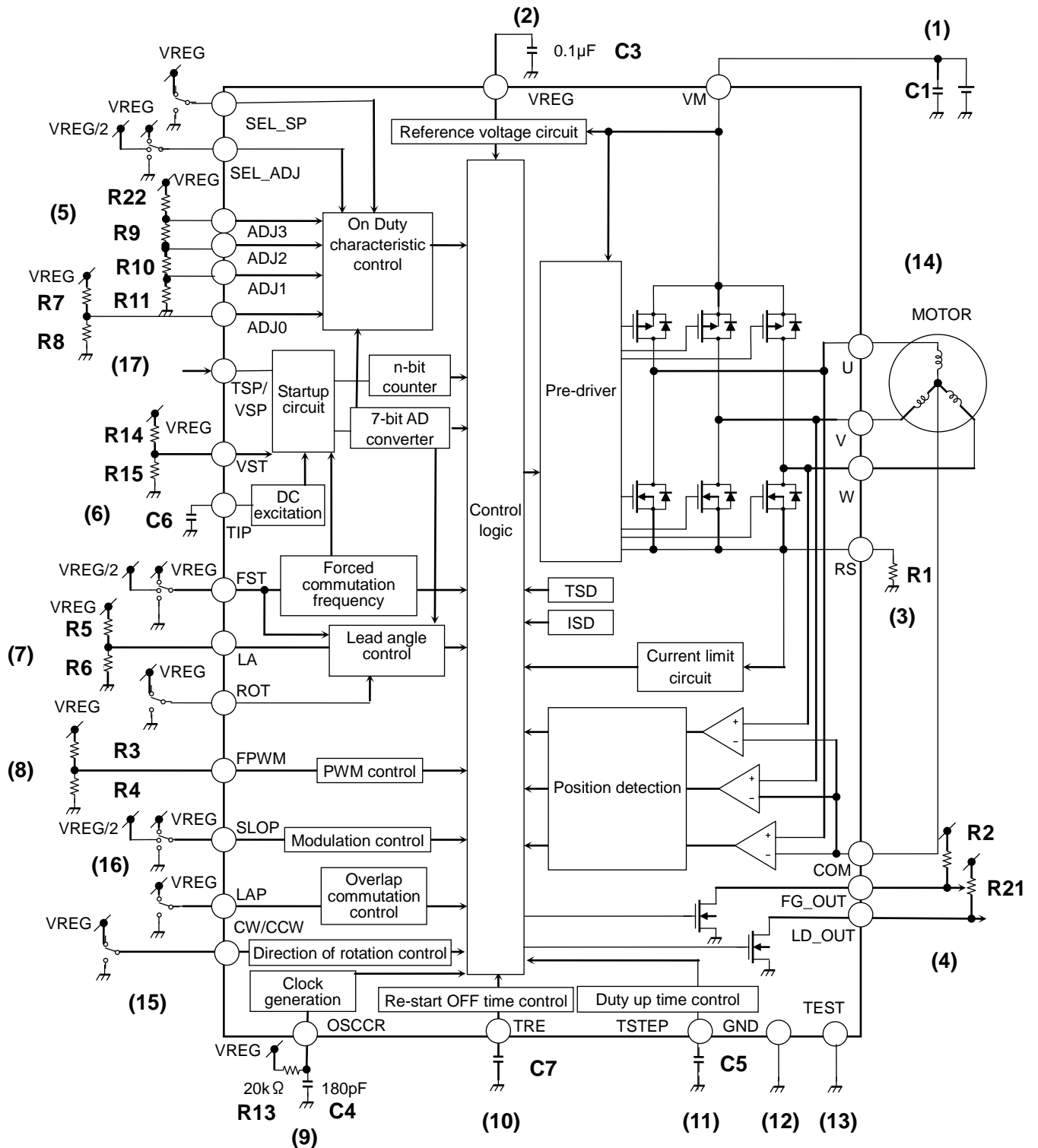


Figure 1 Application circuit example

(1) Capacitor for VM terminal

Take the GND pattern of the print board widely because large current flows from the power supply to the motor through VM terminal.

Connect the capacitor between VM and GND as close to the IC as possible in order to reduce the noise and vibration of VM terminal.

1 μ F to 47 μ F: Electrolytic capacitor
0.001 μ F to 10 μ F: Ceramic capacitor

When the power of the motor is small, applying the ceramic capacitor is enough.
However, the vibration of the power supply can be reduced more efficiently by connecting the large capacity of the electrolytic capacitor for reduction of low-frequency noise and the ceramic capacitor for reduction of high-frequency noise in parallel.

(2) Capacitor for VREG terminal

Connect the capacitor of 0.1 μ F between VREG and GND as close to the IC as possible to reduce the noise and the vibration of VREG terminal.

(3) Setting RS terminal

Take the GND pattern of the print board widely because large current flows to the motor.

Resistance (R1) is for limit of output current. It is recommended to set the resistance of 0.1 Ω or more and the accuracy of 1% or less.

Connect the resistance that permits the power applying to the output current and the VRS voltage (0.25 V) to the resistance (R1).

$$I_{out} [A] = VRS [V]/R1 [\Omega]$$

When the resistance (R1) is configured 0.3 Ω ,
 $I_{out} (typ.) = 0.25 V (typ.)/0.3 \Omega \approx 0.83 A$

(4) Setting FG_OUT and LD_OUT terminals

It is an open-drain output. So, the voltage should be pull-up by the resistance to output high level.

It is recommended to connect the resistance of 10k Ω to 100k Ω .

(5) Setting ADJ0, ADJ1, ADJ2, ADJ3, and SEL_ADJ terminals

Output PWM duty can be adjusted by setting the input PWM duty signal of TSP/VSP terminal with ADJ0, ADJ1, ADJ2, ADJ3, and SEL_ADJ terminals.

Input and output PWM duty of TSP/VSP terminal should operate linearity. In case the output PWM duty is not adjusted, all ADJ0, ADJ1, ADJ2, ADJ3, and SEL_ADJ terminals should be configured to GND.

As for ADJ0 terminal, the accuracy of the resistance should be 1% or less.

And as for ADJ1, ADJ2, and ADJ3 terminals, the accuracy of the resistance should be also 1% or less.

When SEL_ADJ terminal is configured high level, it should short-circuit to VREG terminal. When it is configured middle level, it should be open. And when it is configured low level, it should be connected to GND.

(6) Setting TIP, VST, and FST terminals

Startup sequence starts after receiving the input signal of TSP/VSP terminal. And the operation moves as follows; DC resolution mode → Forced commutation mode → Sensorless mode

When the induced voltage of the motor cannot be position detected regularly by the forced commutation frequency in startup, the operation cannot move to the sensorless drive. In this case, adjustment to synchronize the forced commutation frequency to the motor rotation is necessary.

When initial rotor position is irregular, startup may not succeed because they do not synchronize in the forced commutation mode. In this case, the initial rotor position is fixed in the DC resolution to synchronize them in the forced commutation mode.

So, adjust the DC resolution term (capacitor configuration of TIP terminal) to stop the rotor in any rotor position.

From this rotor stopping position, adjust the forced commutation frequency (configuration of FST terminal) and the output duty (input voltage of VST terminal) in forced commutation mode to move the operation to the Sensorless drive.

By changing the VST terminal, not only the output duty of the forced commutation frequency but also the output duty in the DC resolution term change. And so, readjust the DC resolution term to stop the rotor at the input voltage of VST terminal, which is configured by the forced commutation frequency.

Table 4 Configuration in startup

	DC Resolution term	Forced commutation frequency	Sensorless drive
Set terminal of output Duty	VST	VST	TSP/VSP (ADJ0, ADJ, ADJ2, ADJ3, and SEL_ADJ)
Set terminal of time (frequency)	TIP	FST	—

Configuration of TIP terminal in the DC resolution term can be calculated as follows;

$$\text{DC resolution term: } T = 0.313 \times 31.5 \text{ times} \times C6 \times 10^6$$

$$\text{When } C6 = 0.01 \mu\text{F}, T = 0.0986 \text{ s}$$

As for input voltage of VST terminal, the accuracy of the resistance should be 1% or less.

When FST terminal is configured high level, it should short-circuit to VREG terminal. When it is configured middle level, it should be open. When it is configured low level, it should be connected to GND.

FST = High : Forced commutation frequency $f_{ST} \approx 6.4 \text{ Hz}$

FST = Middle, Open : Forced commutation frequency $f_{ST} \approx 3.2 \text{ Hz}$

FST = Low : Forced commutation frequency $f_{ST} \approx 1.6 \text{ Hz}$

*Forced commutation frequency: Initial value. It changes after operation.

(7) Setting LA terminal

Lead angle can be configured by the input voltage of LA terminal.
When most appropriate lead angle is set, the efficiency is improved and the noise is reduced.
The accuracy of the resistance should be 1% or less.

Table 5 LA setting

ROT	Reference configuration			Number of steps of LA set	Voltage of LA terminal [V]	Rotation speed (electrical angle)					
						FST terminal=L: upper step (0 to 750Hz)/FST terminal=H/M: lower step (0 to 1.5kHz)					
	R5	R6	Set voltage			0 to 100Hz	100 to 200Hz	200 to 300Hz	300 to 400Hz	400 to 500Hz	500Hz to 750Hz
H	-	-	VREG	8	2.5	30°					
	18kΩ	16kΩ	2.35	7	2.1875	26.25°					
	12kΩ	8.2kΩ	2.03	6	1.875	22.5°					
	13kΩ	6.8kΩ	1.72	5	1.5625	18.75°					
	12kΩ	4.7kΩ	1.41	4	1.25	15°					
	20kΩ	5.6kΩ	1.09	3	0.9375	11.25°					
	13kΩ	2.4kΩ	0.78	2	0.625	7.5°					
	15kΩ	1.6kΩ	0.48	1	0.3125	3.75°					
	-	-	GND	0	0	0°					
L	-	-	VREG	8	2.5	3.75°	11.25°	18.75°	26.25°	30°	30°
	18kΩ	16kΩ	2.35	7	2.1875	11.25°	15°	18.75°	22.5°	26.25°	30°
	12kΩ	8.2kΩ	2.03	6	1.875	7.5°	11.25°	15°	18.75°	22.5°	26.25°
	13kΩ	6.8kΩ	1.72	5	1.5625	3.75°	7.5°	11.25°	15°	18.75°	22.5°
	12kΩ	4.7kΩ	1.41	4	1.25	0°	3.75°	7.5°	11.25°	15°	18.75°
	20kΩ	5.6kΩ	1.09	3	0.9375	0°	15°	15°	15°	18.75°	22.5°
	13kΩ	2.4kΩ	0.78	2	0.625	7.5°	7.5°	15°	15°	18.75°	22.5°
	15kΩ	1.6kΩ	0.48	1	0.3125	0°	7.5°	15°	15°	18.75°	22.5°
	-	-	GND	0	0	7.5°	15°	15°	15°	18.75°	22.5°

(8) Setting FPWM terminal

PWM frequency of the output can be configured by the input voltage of FPWM terminal.

Since the position is detected at the timing of the output PWM, when the rotation speed increases, the PWM frequency should be set higher. However, when the output PWM frequency is set higher, it becomes harder to detect the position in startup and in low rotation speed mode. So, please configure them by referring to the following calculation.

$$\text{Rotation frequency [Hz]} = \text{PWM frequency [Hz]} / 100$$

(Example)

When PWM frequency = 23.8 kHz,

Rotation frequency = about 238Hz or less (in case of 4-polar motor: about 7140[rpm])

The accuracy of the resistance should be 1% or less.

Table 6 FPWM setting

Example			Number of set steps of FPWM terminal	Voltage of FPWM terminal[V]	Rotation speed (electrical angle)					
R3	R4	Set voltage			0 to 200Hz	200 to 400Hz	400 to 600Hz	600 to 800Hz	800Hz to 1kHz	1kHz to 1.5kHz
-	-	VREG	8	2.5	23.8kHz	47.7kHz	95.3kHz	95.3kHz	190.6kHz	190.6kHz
18kΩ	16kΩ	2.35V	7	2.1875	23.8kHz	23.8kHz	47.7kHz	47.7kHz	95.3kHz	95.3kHz
12kΩ	8.2kΩ	2.03V	6	1.875	23.8kHz	47.7kHz	95.3kHz	95.3kHz	95.3kHz	95.3kHz
13kΩ	6.8kΩ	1.72V	5	1.5625	47.7kHz	47.7kHz	95.3kHz	95.3kHz	95.3kHz	190.6kHz
12kΩ	4.7kΩ	1.41V	4	1.25	47.7kHz	95.3kHz	95.3kHz	95.3kHz	95.3kHz	190.6kHz
20kΩ	5.6kΩ	1.09V	3	0.9375	190.6kHz					
13kΩ	2.4kΩ	0.78V	2	0.625	95.3kHz					
15kΩ	1.6kΩ	0.48V	1	0.3125	47.7kHz					
-	-	GND	0	0	23.8kHz					

(9) Setting OSCCR terminal

OSCCR terminal configures OSC frequency which corresponds to the reference oscillation frequency.

When the capacitor of 180pF (C4) and the resistance of 20kΩ (R13) are connected to OSCCR terminal, the frequency of OSCCR terminal is 762.5 kHz, and that of OSC terminal is 12.2MHz. The frequency of OSC terminal corresponds to '16 × (frequency of OSCCR terminal)'.

The frequency of OSC terminal is gained from following formula.

$$\text{OSC frequency} = 43.92 / (C4 \times R13) \text{ [Hz]}$$

However, the capacitor (C4) is adopted 180pF and the resistance of R13 is adopted 20kΩ. So, if the constant numbers are changed, some differences may be occurred in comparing to the above formula.

In order not to be influenced by noise and wiring impedance, the capacitor (180pF, accuracy: 1% or less) should be connected between OSCCR terminal and GND as close to the IC as possible.

And the resistance (20kΩ, accuracy: 1% or less) should be connected between OSCCR terminal and VREG terminal as close to the IC as possible.

(10) Setting TRE terminal

When abnormality is detected, the output is turned off (high impedance: Hi-Z) in the restart term configured by the capacitor of TRE terminal.

Abnormality detection is configured as follows;

1. When forced commutation frequency corresponds to 4-electrical angle
2. In ISD operating
3. In TSD operating
4. When rotation speed is under the forced commutation frequency during sensorless drive
5. In reaching the maximum commutation frequency (FMAX)

When FST = High	FMAX = 1.5kHz/1electrical angle frequency
When FST = Middle	FMAX = 1.5kHz/1electrical angle frequency
When FST = Low	FMAX = 750Hz /1electrical angle frequency

Restart term can be set by the capacitor of TRE terminal.

Restart term: $T = 0.313 \times 31.5 \text{ times} \times C \times 10^6$

When $C = 1 \mu\text{F}$, $T = 9.86 \text{ s}$

(11) Setting TSTEP terminal

TSTEP terminal can configure the time that the increasing duty of input control signal of TSP/VSP terminal reflects on the output duty. It can accelerate the motor rotation speed gradually in startup.

Acceleration time: $T = 0.313 \times 31.5 \text{ times} \times C \times 10^6$

When $C = 0.01 \mu\text{F}$, $T = 0.0986 \text{ s}$

(12) Setting GND terminal

Take the GND wiring pattern widely with solid wiring as possible.

(13) Setting TEST terminal

Connect to GND because of test terminal.

(14) Setting U, V, and W terminals

Take the wiring pattern widely because large current flows in the motor.

(15) Setting CW/CCW terminal

The rotation direction of the motor can be switched by CW/CCW terminal.

In switching the rotation direction, please stop the motor to turn off the output by the TSP/VSP terminal. Then, switch the rotation direction by changing the configuration of CW/CCW terminal.

(16) Setting SLOP and LAP terminals

In forced commutation mode in startup, the motor operates under the condition as follows; lead angle = 0°, 120° commutation, and without soft switching. And the operation changes automatically to the configured mode by LA, LAP, and SLOP terminals when the operation switches to the sensorless mode.

The ability of noise reduction and power consumption changes by changing the configuration of soft switching and conduction angle of the motor. So, please determine the optimum configuration after evaluate the applied motor enough.

Soft switching switches the conduction shift gradually. Soft switching of pattern A switches the commutation more gently than that of pattern B. The ability of noise reduction and power consumption depends on the characteristics of the motor. So, please determine the optimum configuration after evaluate the applied motor enough.

Table 3 Setting SLOP and LAP terminals

SLOP terminal	LAP terminal	Soft switching	Commutation angle
H	H	Without	120° commutation
	M	Without	135° commutation
	L	Without	150° commutation
L	H	With B pattern	150° commutation
	M	With	135° commutation
	L	With A pattern	150° commutation

(17) Setting TSP/VSP and SEL_SP terminals

Input signal of TSP/VSP terminal starts up and stops the motor operation, and controls the output PWM duty to control the rotation speed of the motor.

Moreover, input signal of TSP/VSP terminal can select pulse duty control or analog voltage control by SEL_SP terminal.

Output PWM duty in the DC excitation mode and the forced commutation mode is according to the voltage of VST.

As other functions, input signal of TSP/VSP terminal can adjust the output PWM duty by the configuration of ADJ0, ADJ1, ADJ2, and ADJ3 terminals.

Input of SEL_SP terminal	Input control of TSP/VSP terminal
High	Analog voltage control
Low	Pulse duty control

5. Circuit dimensions (for reference only)

The idling detector is built in and a motor can start rotating from the idling state of a forward direction in starting. However, when the motor is vibrating by the external factor etc. also in the state where the motor stops, change of the delicate electric signal by the vibration may be incorrect-detected as idling of a motor. And the motor may not start operating normally.

In such a case, the motor can start operating normally by adding the external resistances of R16, R17, R18, and R19 to provide the offset voltage in the position detection comparator inside IC, as shown in the following figure.

However, if offset voltage is increased too much under the condition that the motor rotates at low speed, idling detection does not work. And the motor starts operation in recognizing the state as a stop.

Rough calculation of offset voltage: $V_M \times R_{19} / \{R_{19} + R_{20} + (R_{16}R_{17}R_{18}) / (R_{16}R_{17} + R_{17}R_{18} + R_{16}R_{18})\}$

Example: When $V_M=12V$, $R_{16}=100k\Omega$, $R_{17}=100k\Omega$, $R_{18}=100k\Omega$, $R_{19}=1k\Omega$, and $R_{20}=100k\Omega$,

Offset voltage = $12V \times 1k / (100k + 1k + 33.3k) \approx 90mV$

In case that the rotation speed is maximum when V_M is 12V, the offset voltage is 7.5% of V_M ($90mV/12V=7.5\%$). So, when the rotation speed is about 7.5% or less of the maximum rotation speed, idling cannot be detected.

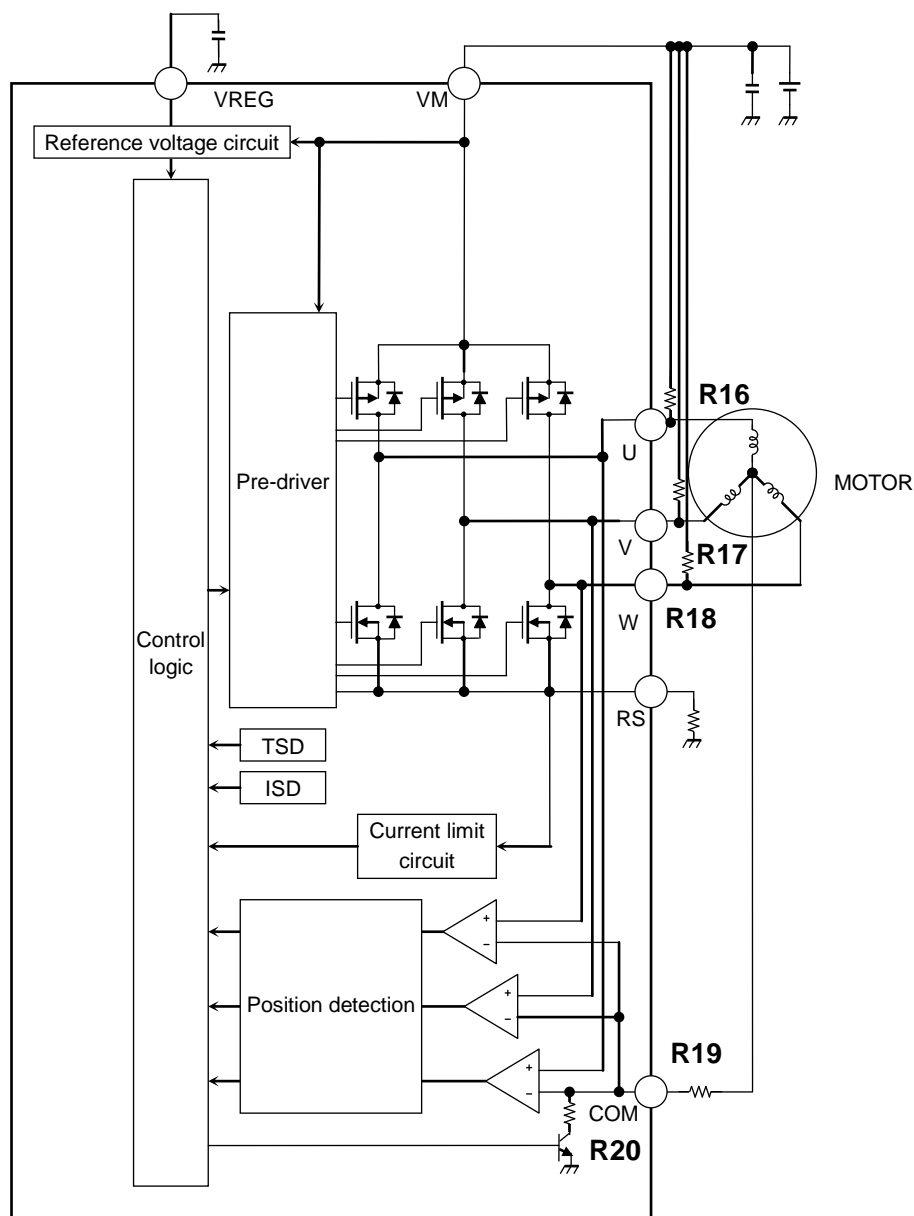


Figure 2 Circuit dimensions (for reference only)

6. Power consumption

The power consumption is calculated from below formulas.

Power consumption $P [W] = V_M \times I_M + I (RMS)^2 \times R_{on}$

Example: When $V_M=12V$ and $I_{OUT} (peak) = 1.1A$,

(As for circuit current (I_M) and output ON resistance (R_{ON}), please refer to 'Electrical characteristics' in the technical data sheet.)

$P(IC) Typ = 12V \times 6mA + (0.707 \times 1.1A)^2 \times 0.6\Omega = 0.432W$

$P(IC)Max = 12V \times 8.5mA + (0.707 \times 1.1A)^2 \times 1.2\Omega = 0.827W$

Junction temperature (T_j) of the IC is calculated from the ambient temperature (T_a) and the power consumption shown below.

$T_j = P \times \theta_{ja} + T_a$

θ_{ja} : Heat resistance between junction temperature and ambient temperature

T_a : Ambient temperature (Surrounding constant temperature which avoids influence of heat)

Example: When mounted to the package, θ_{ja} is calculated $44.64^\circ C/W$ from the power dissipation provided in below figure.

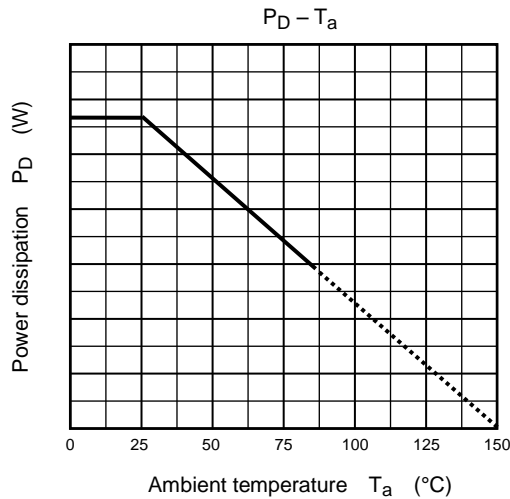
When $T_a = 85^\circ C$, Power consumption (P_{MAX}) = $0.827 W$,

$T_j = 0.827 W \times 44.64^\circ C/W + 85^\circ C = 122^\circ C$

Pay attention that θ_{ja} depends on the usage conditions such as mounting method.

When ambient temperature is high, the power dissipation decreases.

Please use the IC with enough margin after evaluating the board by setting the junction temperature $150^\circ C$ or less because above formulas are rough calculations.



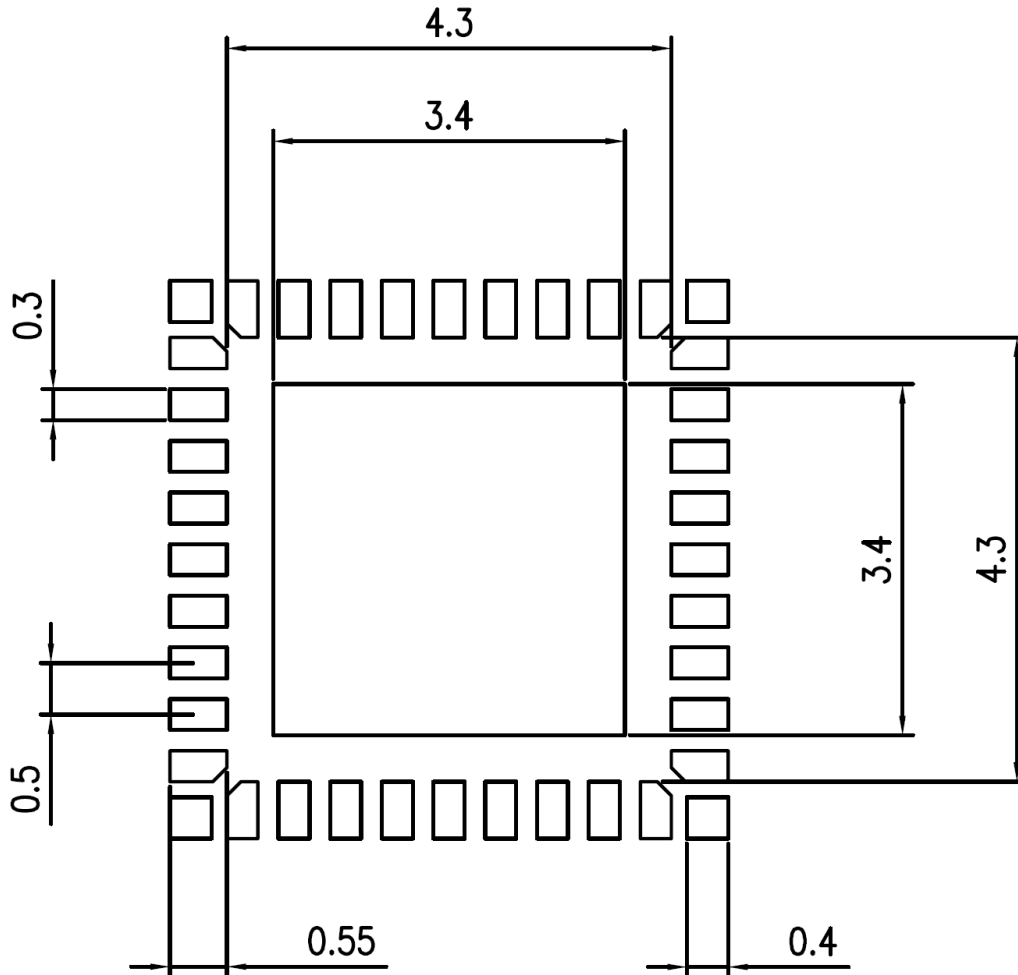
When mounted to the board
(4-layer FR4 board: 76.2mm x 114.3mm x 1.6mm)

Figure 3 Power dissipation

7. Land pattern dimensions (for reference only)

P-VQFN36-0505-0.50-001

Unit: mm



Notes

- All linear dimensions are given in millimeters unless otherwise specified.
- This drawing is based on JEITA ET-7501 Level3 and should be treated as a reference only. TOSHIBA is not responsible for any incorrect or incomplete drawings and information.
- You are solely responsible for all aspects of your own land pattern, including but not limited to soldering processes.
- The drawing shown may not accurately represent the actual shape or dimensions.
- Before creating and producing designs and using, customers must also refer to and comply with the latest versions of all relevant TOSHIBA information and the instructions for the application that Product will be used with or for.

Figure 4 Land pattern dimensions (for reference only) (P-VQFN36-0505-0.50-001)

**IC Usage Considerations
Notes on handling of ICs**

- [1] The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings. Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
- [2] Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

Points to remember on handling of ICs**(1) Over current Protection Circuit**

Over current protection circuits (referred to as current limiter circuits) do not necessarily protect ICs under all circumstances. If the over current protection circuits operate against the over current, clear the over current status immediately.

Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the over current protection circuit to not operate properly or IC breakdown before operation. In addition, depending on the method of use and usage conditions, if over current continues to flow for a long time after operation, the IC may generate heat resulting in breakdown.

(2) Thermal Shutdown Circuit

Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over temperature, clear the heat generation status immediately.

Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the thermal shutdown circuit to not operate properly or IC breakdown before operation.

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