TC78B006 Series
Usage Considerations

Rev. 1.0

Description

The TC78B006 series are single phase full-wave drivers for fan motors.
The TC78B006 series drive external Pch+Nch FET by PWM control.

Contents

Description 1
Contents 2
Figure Contents 3
Table contents 3
1. Main difference between TC78B006 series 4
2. Power Supply Voltage 4
3. PWM duty resolution 6
4. Control signal 8
4.1. VSOFT 8
4.2. SS 9
4.3. VMI 10
4.4. CT 10
5. Output of pre-driver 11
5.1. High side pre-driver output 11
5.2. Low side pre-driver output 12
6. Protection functions 13
6.1. Lock protection 13
6.2. Current limit 13
6.3. Thermal shutdown (TSD) 14
6.4. Under voltage lockout (UVLO) 14
7. Power consumption of the IC 15
8. Notes in designing PCB 17
Notes on Contents 18
IC Usage Considerations 18
Points to remember on handling of ICs 19
RESTRICTIONS ON PRODUCT USE 20

Figure Contents

Figure 2.1 VM voltage rise by motor regeneration current during phase switching 5
Figure 2.2 VM voltage rise by motor regeneration current during IC protection 5
Figure 2.3 Protection against VM voltage rise 5
Figure 3.1 Relation between VSP voltage and output PWM Duty 6
Figure 3.2 Relation between TSP frequency and Resolution (fosc=10MHz) 7
Figure 4.1 Operation waveform example (No soft switching) 8
Figure 4.2 Operation waveform example (soft switching=31.9°) 8
Figure 4.3 Operation waveform example (soft switching=61°) 8
Figure 4.4 Operation waveform example (soft switching=90°) 8
Figure 4.5 Operation waveform example (no soft stat time) 9
Figure 4.6 Operation waveform example (soft start time=1.3s) 9
Figure 4.7 Operation waveform example (soft start time=2.7s) 9
Figure 4.8 Operation waveform example (soft start time=5.1s) 9
Figure 5.1 Application circuit example of drive external FETs (12V/24V power supply) 11
Figure 5.2 Application circuit of drive external FETs (48V power supply) 12
Figure 6.1 Setting of current limit 13

Table contents

Table 1.1 Product comparison 4
Table 2.1 Operating range of power supply voltage 4
Table 4.1 Relation between VSOFT voltage and soft switching term 8
Table 4.2 Relation between VMI voltage and minimum duty / startup threshold 10
Table 4.3 Function of CT pin 10

1. Main difference between TC78B006 series

Main differences are shown in table below

Table 1.1 Product comparison

Item	Output duty control signal	Output signal	Package
TC78B006FTG	PWM duty	Rotation speed (FG)	SSOP16
TC78B006FNG	PWM duty	Rotation speed (FG)	WQFN16
TC78B006AFTG	PWM duty	Lock Detection (RDO)	SSOP16
TC78B006AFNG	PWM duty	Lock Detection (RDO)	WQFN16
TC78B006BFTG	Analog voltage	Rotation speed (FG)	SSOP16
TC78B006BFNG	Analog voltage	Rotation speed (FG)	WQFN16
TC78B006BFTG	Analog voltage	Lock Detection (RDO)	SSOP16
TC78B006BFNG	Analog voltage	Lock Detection (RDO)	WQFN16

2. Power Supply Voltage

To use the TC78B006, power supply voltage should be applied to the VM pin.

The VM voltage should be within the operating range from 3.5V to 30V though the absolute maximum rating of the VM voltage is 40V.

Table 2.1 Operating range of power supply voltage

Characteristic	Symbol	Operating Voltage Range	Unit
VM power supply voltage (Normal)	VM_{opr1}	5.5 to 30	V
VM power supply voltage (low voltage operation)	VM_{opr2}	3.5 to 5.5	V

Note: The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Use the IC within the operating power supply voltage range.

The TC78B006 series use single power supply. There is no special procedure for power on or off.

If motor speed is controlled by external TSP/VSP signal, it is recommended to input TSP/VSP signal after VM supply voltage is stable, because the motor may not function normally when the power supply is unstable. There is no problem if motor speed is controlled by VSP voltage which is generated by resistor division from V_{REG}.

When power off, VM voltage may rise due to regenerative current. It is recommended stopping the motor before shutting off the power supply. If motor speed is controlled by VSP voltage which is generated by resistor division from V_{REG} or if the minimum output duty is set, make sure that the VM voltage does not exceed the absolute maximum rating when the power is shut off

V_{REG} is the power supply voltage for IC internal circuit. It is generated by IC's internal regulator. Do not apply a voltage from outside to VREG pin. A capacitor of 0.1μF is required between VREG pin and GND to make V_{REG} voltage stable. Place the capacitor as close as possible to the IC. Be careful with the layout so that there is no switching current path between the capacitor's GND and IC's GND pin. Please confirm V_{REG} voltage does not exceed 5.5V referring to IC's GND pin in the IC operation.

V_{REG} can also be used as the voltage of the hall element or the voltage for IC control pins by resistor division circuit. Please do not draw current more than the capacity of the internal regulator. The output current should not exceed the absolute maximum rating of 10mA.

・Notes in using the IC when VM is 12V or less

In low-voltage operation, the electrical characteristics, such as output resistance, change compared to the condition that VM is 12V. For more detail information, please refer to "Reference Data" of the electrical characteristics in the datasheet.

When VM is 12V or less, the voltage of the gate driver drops. Please check the gate threshold voltage characteristic of the external FET to make sure the gate drive voltage is enough. For more detail

information, please refer to “Chapter 5. Output of pre-driver”

When VM is 5.5V or less, the V_{REG} voltage drops along with VM voltage. The reference voltage of the A/D conversion circuit is V_{REG}. So, if the voltage of the IC control pin (VSP, VMI, VSOFT, CT, and SS) is generated by resistor division from V_{REG}, the A/D conversion result is nearly unchanged. However, if the voltage is input from outside directly, the A/D conversion result may change. Especially in the case that VSP voltage is input from outside, the output duty may increase when VM voltage is low.

・VM voltage rise due to motor regeneration current

VM voltage rises because of the motor regeneration current. Especially when reverse connection protection diode is used in the circuit, VM voltage rises since the current cannot regenerate back to the power supply. VM voltage must not exceed the absolute maximum rating including the voltage rise due to the regenerative current.

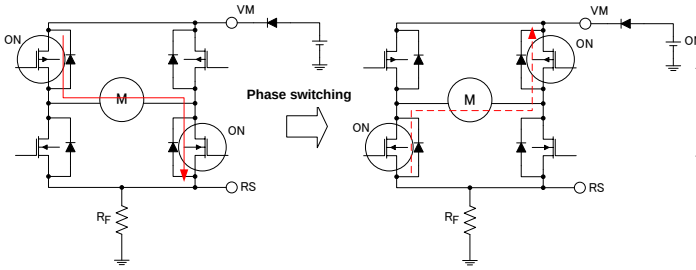


Figure 2.1 VM voltage rise by motor regeneration current during phase switching

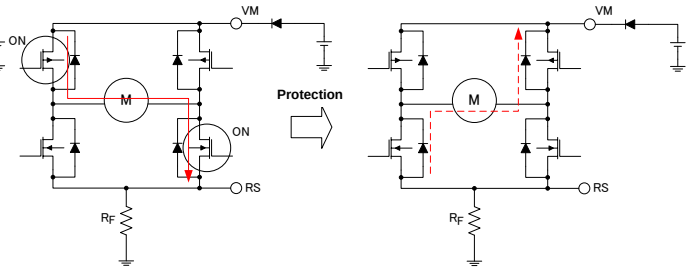


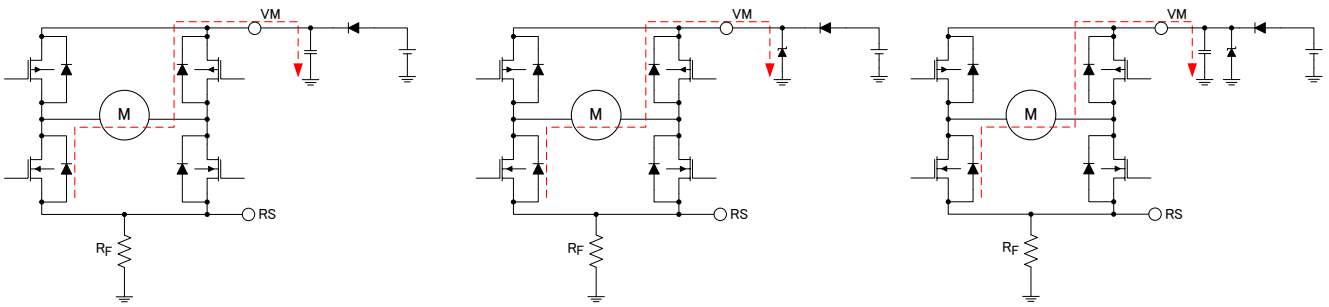
Figure 2.2 VM voltage rise by motor regeneration current during IC protection

The soft switching function of the TC78B006 can suppress the current flowing through the motor before phase switching. By reducing the regeneration current during phase switching close to zero, the VM voltage rise can be suppressed.

The period of PWM OFF is provided before all external FET are turned off in order to suppress the VM voltage rise caused by the regenerative current. During the PWM OFF period, one side of the lower FET keeps on state. The regenerative current is attenuated by low-side regeneration.

However, when an abnormality such as power shutdown occurs during motor rotation, IC cannot insert the PWM OFF period to attenuate regeneration current before all external FET turn off. To absorb the regenerative current to the power supply line, place (a) capacitor or (b) zener diode, or (c) both if necessary between VM and GND. The capacitor and the zener diode should be placed as close as possible to the IC. Please confirm that the VM voltage rise is limited under the absolute maximum rating with proper margin.

In addition to protect the IC against VM voltage rise due to motor regeneration current, zener diode can also protect the IC from the overvoltage of the external power supply. Choose the zener diode whose voltage is higher than the motor normal operating voltage so that current will not flow through the zener diode during the motor normal operation.



(a) Add Capacitor (b) Add Zener diode (c) Add both

Figure 2.3 Protection against VM voltage rise

3. PWM duty resolution

・Output PWM duty resolution

The output PWM frequency of the TC78B006 series is 40 kHz (typ.). The duty of output PWM is generated by comparing the internal modulation waveform and the internal 8-bit sawtooth wave. Therefore, the resolution of the output PWM duty is 8 bit (256 steps).

However, although based on the response characteristic of external FET, when “on” time of the PWM output is short, the actual output of FET may be “off”. If the “off” time of the IC’s PWM output is short, the actual output of the FET may be 100% “on”.

・Input control signal resolution

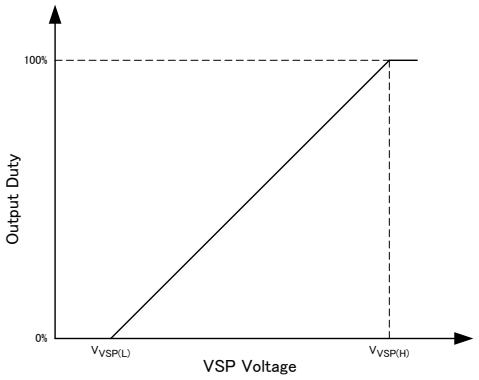
・In case of VSP input

The voltage of VSP pin is digitized by an internal 8-bit A/D converter. IC’s internal logic uses the digitized data to control the amplitude of the internal modulation waveform. The duty of output PWM is generated by comparing the internal modulation waveform and the internal 8-bit sawtooth wave.

Relation of VSP voltage and output PWM duty is as follows.

The effective resolution of VSP is 7bit (128 steps) ranging from 1.5V to 3.6V.

0	≤	VSP	≤	$V_{VSP\ (L)}$	→	Duty = 0% (A/D conversion result of VSP voltage: 0 to 89)
$V_{VSP\ (L)}$	<	VSP	≤	$V_{VSP\ (H)}$	→	Figure 3.1 (A/D conversion result of VSP voltage: 90 to 217)
$V_{VSP\ (H)}$	<	VSP	≤	V_{REG}	→	Duty = 100% (A/D conversion result of VSP voltage: 218 to 255)



Note: Output PWM duty varies in 128 steps from 0% to 100%, in response to the VSP voltage ranging from $V_{VSP\ (L)}$ to $V_{VSP\ (H)}$.

Figure 3.1 Relation between VSP voltage and output PWM Duty

$V_{VSP\ (L)}$ =1.5V (typ.) $V_{VSP\ (H)}$ =3.6V (typ.)

・In case of TSP input

Duty of the TSP signal is detected by internal clock. The resolution of TSP duty is related to the frequency of TSP signal as follows.

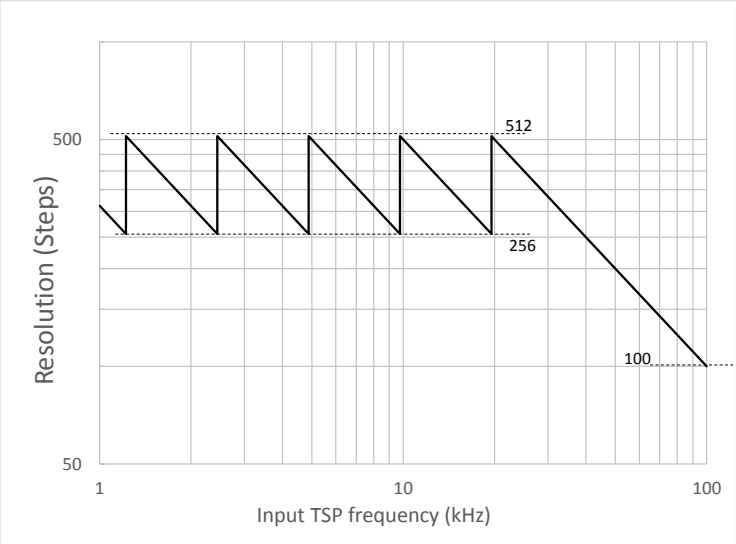


Figure 3.2 Relation between TSP frequency and Resolution (fosc=10MHz)

When f_{OSC} is10MHz, the resolution is 8-bit (256 steps) or more if TSP frequency is 39 kHz or less. The resolution decreases if TSP frequency exceeds 39 kHz. When TSP frequency is 100 kHz, the resolution becomes 100 steps.

When f_{OSC} is7MHz, the resolution is 8-bit (256 steps) or more if TSP frequency is 27 kHz or less. The resolution decreases if TSP frequency exceeds 27 kHz. When TSP frequency is 100 kHz, the resolution becomes 70 steps.

When f_{OSC} is13MHz, the resolution is 8-bit (256 steps) or more if TSP frequency is 50 kHz or less. The resolution decreases if TSP frequency exceeds 50 kHz. When TSP frequency is 100 kHz, the resolution becomes 130 steps.

4. Control signal

4.1. VSOFT

The voltage of VSOFT pin controls the soft switching function.

The soft switching function of the TC78B006 series inserts a certain period of time before and after conducting phase switching. Output PWM duty changes gradually in this period. The soft switching function is effective in reducing the motor vibration and suppressing the VM voltage rise, which occurs during conducting phase switching.

The voltage of VSOFT pin is digitized by the internal 8-bit A/D converter. IC's internal logic uses the digitized data to set the period of soft switching.

Table 4.1 Relation between VSOFT voltage and soft switching term

Step	VSOFT (V)	term (°)	Step	VSOFT (V)	term (°)	Step	VSOFT (V)	term (°)
1	0.00	0.0	12	1.46	31.9	23	2.92	63.9
2	0.13	2.9	13	1.59	34.8	24	3.05	66.8
3	0.27	5.8	14	1.73	37.7	25	3.19	69.7
4	0.40	8.7	15	1.86	40.6	26	3.32	72.6
5	0.53	11.6	16	1.99	43.5	27	3.45	75.5
6	0.66	14.5	17	2.13	46.5	28	3.59	78.4
7	0.80	17.4	18	2.26	49.4	29	3.72	81.3
8	0.93	20.3	19	2.39	52.3	30	3.85	84.2
9	1.06	23.2	20	2.52	55.2	31	3.98	87.1
10	1.20	26.1	21	2.66	58.1	32	4.12	90.0
11	1.33	29.0	22	2.79	61.0			

The table shows the threshold voltage of each step. For example, when the VSOFT voltage is 0.3V, the result is "step 3" since it is in the range of 0.27V to 0.4V.

In case of setting step 0, connect VSOFT pin to IC's GND directly. In case of setting step 32, VSOFT can be connected to VREG pin directly. In case of setting other steps, please generate the VSOFT voltage by resistor division from V_{REG}.

VSOFT=0V

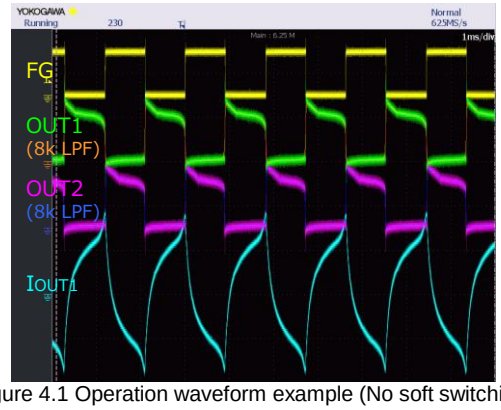


Figure 4.1 Operation waveform example (No soft switching)

VSOFT=1.55V

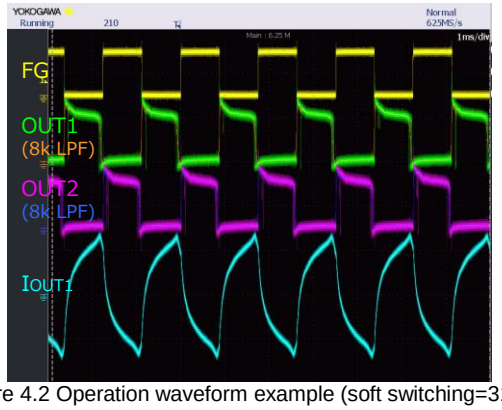


Figure 4.2 Operation waveform example (soft switching=31.9°)

VSOFT=2.85V

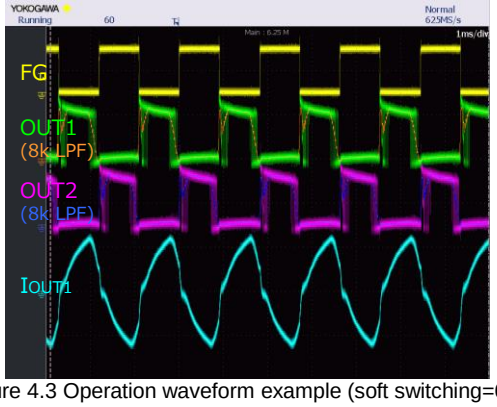


Figure 4.3 Operation waveform example (soft switching=61°)

VSOFT=4.5V

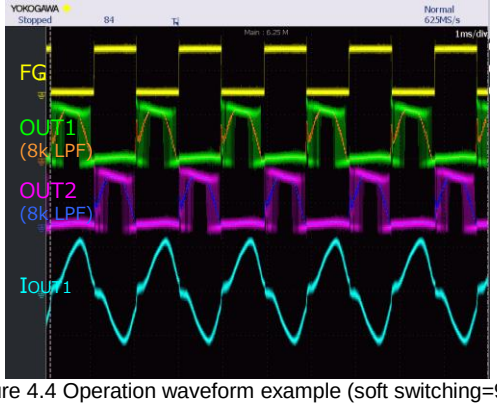


Figure 4.4 Operation waveform example (soft switching=90°)

4.2. SS

The voltage of SS pin controls the rate of acceleration or deceleration.

The voltage of SS pin is digitized by the internal 8-bit A/D converter. Voltage in the range from 0 to V_{ADC} (4.25V) is converted to the value between 0 and 255. Voltage which is V_{ADC} (4.25V) or more is converted to the value of 255. IC's internal logic uses the digitized data to control the rate of acceleration or deceleration. Please generate the SS voltage by resistor division from V_{REG}.

When the output PWM duty is changed, the accelerate or decelerate time from the previous output PWM duty to the new target output PWM duty can be calculated by the following formula.

・Previous output PWM duty = A (%)
・New target output PWM duty = B (%)
・Digitized SS voltage = N_{SS}
・Time = $|B - A| / 0.4 \times 4 \times N_{SS} \times (1 / f_{PWM})$

For example, when previous output PWM duty=50%, new target output PWM=70%, and digitized SS voltage=100,
the accelerate time = $(70-50) / 0.4 \times 100 \times (1 / 40kHz) = 0.5s$

The TC78B006 series have a soft start function. The soft start time is configured by the voltage of SS pin. When the motor starts up, output PWM duty changes gradually from 20% to the target output duty set by TSP. The soft start time can be calculated by the following formula.

・Start up PWM duty = 20(%)
・Target output PWM duty = B (%)
・Digitized SS voltage = N_{SS}
・Time = $|B - 20| / 0.4 \times 4 \times N_{SS} \times (1 / f_{PWM})$

For example, when target output PWM duty=100%, and digitized SS voltage=100,
the soft start time=$(100-20)/0.4 \times 100 \times (1 / 40kHz) = 2.0s$

The example waveform of soft start when the target output PWM duty corresponds to 100% is as follows.

SS=0V (N_{SS}=0)

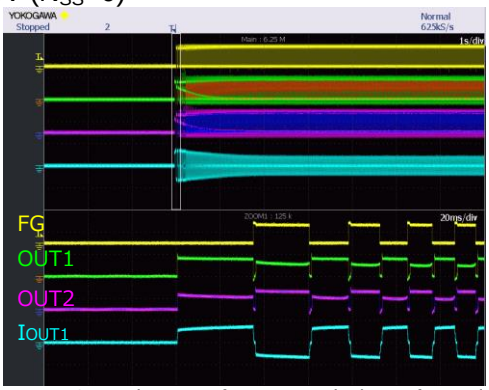


Figure 4.5 Operation waveform example (no soft stat time)

SS=1.1V (N_{SS}=66)

Figure 4.6 Operation waveform example (soft start time=1.3s)

SS=2.2V (N_{SS}=132)

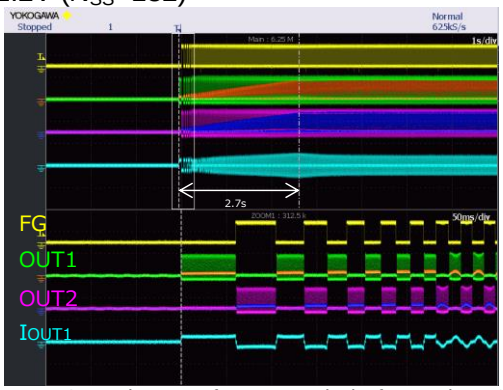


Figure 4.7 Operation waveform example (soft start time=2.7s)

SS=4.25V (N_{SS}=255)

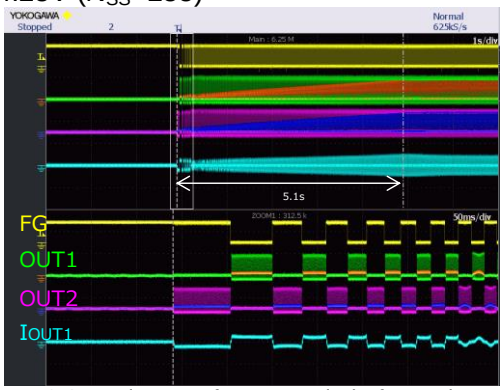


Figure 4.8 Operation waveform example (soft start time=5.1s)

4.3. VMI

The minimum of output PWM duty and the startup threshold duty (TSP input) / startup threshold voltage (VSP input) can be configured by the voltage of VMI pin.

Table 4.2 Relation between VMI voltage and minimum duty / startup threshold

Step	VMI [V]	Minimum Duty	Startup threshold Duty/Voltage	Step	VMI [V]	Minimum Duty	Startup threshold Duty/Voltage	Step	VMI [V]	Minimum Duty	Startup threshold Duty/Voltage
1	0.00	0%	0% / 1.5V	12	1.46	35%	0% / 0V	23	2.92	0%	5% / 1.61V
2	0.13	5%	0% / 0V	13	1.59	38%	0% / 0V	24	3.05	0%	10% / 1.71V
3	0.27	8%	0% / 0V	14	1.73	41%	0% / 0V	25	3.19	0%	15% / 1.83V
4	0.40	11%	0% / 0V	15	1.86	44%	0% / 0V	26	3.32	0%	20% / 1.93V
5	0.53	14%	0% / 0V	16	1.99	47%	0% / 0V	27	3.45	0%	25% / 2.03V
6	0.66	17%	0% / 0V	17	2.13	50%	0% / 0V	28	3.59	0%	30% / 2.14V
7	0.80	20%	0% / 0V	18	2.26	50%	0% / 0V	29	3.72	0%	35% / 2.24V
8	0.93	23%	0% / 0V	19	2.39	50%	0% / 0V	30	3.85	0%	40% / 2.36V
9	1.06	26%	0% / 0V	20	2.52	0%	0% / 1.5V	31	3.98	0%	45% / 2.46V
10	1.20	29%	0% / 0V	21	2.66	0%	0% / 1.5V	32	4.12	0%	50% / 2.56V
11	1.33	32%	0% / 0V	22	2.79	0%	0% / 1.5V				

(Minimum of output duty indicates the value of output peak because this circuit has a soft switching function.)

The table shows the threshold voltage of each step. For example, when the VMI voltage is 0.3V, the result is “step 3” since it is in the range of 0.27V to 0.4V.

In case of setting step 0, connect VMI pin to IC’s GND directly. In case of setting step 32, VMI can be connected to VREG pin directly. In case of setting other steps, please generate the VMI voltage by resistor division from V_{REG}.

4.4. CT

The voltage of CT pin sets the lock protection time (T_{ON}) and auto restart interval time (T_{OFF}). It can also select enable or disable of the standby mode.

Table 4.3 Function of CT pin

Setting of CT pin		T_{ON} term [s]	T_{OFF} term [s]	Standby mode
Voltage range (V_{REG}=5V)	Recommended setting			
3.73V to V_{REG}	Short to VREG	0.3	3.0	Invalid
3.20V to 3.72V	Pull-up to VREG with a resistor of 39kΩ	0.6	6.0	Invalid
2.67V to 3.18V	Pull-up to VREG with a resistor of 120kΩ	0.6	6.0	Valid
2.13V to 2.65V	Open	0.3	3.0	Valid
1.60V to 2.12V	Pull-down with a resistor of 75kΩ	0.3	6.0	Valid
0.55V to 1.58V	Pull-down with a resistor of 18kΩ	0.3	4.5	Valid
0V to 0.52V	Short to GND	Lock protection is invalid		Invalid

The lock protection time can be selected from 0.3s or 0.6s. Please confirm that the motor can start up within the lock protection term when soft start is valid. Choose the auto restart interval time not to let the motor overheat during lock state. When CT pin is short-circuited to GND, lock protection and standby mode will disable.

In setting CT pin voltage, please use recommended pull-up / pull-down resistor. Accuracy of the resistor should be ±5% or more. It is not recommended to apply voltage to CT pin directly.

5. Output of pre-driver

5.1. High side pre-driver output

The high-side pre-driver output of the TC78B006 series is a constant current open-drain type. An example of the application circuit is shown as figure 5.1.

The gate drive voltage of Pch FET (V_{GP}) is the voltage between the gate and the source of the external Pch FET. This voltage is generated by R1. Determine R1 to make V_{GP} exceed the threshold voltage of the Pch FET enough. However, V_{GP} must not exceed the absolute maximum rating of the Pch FET.

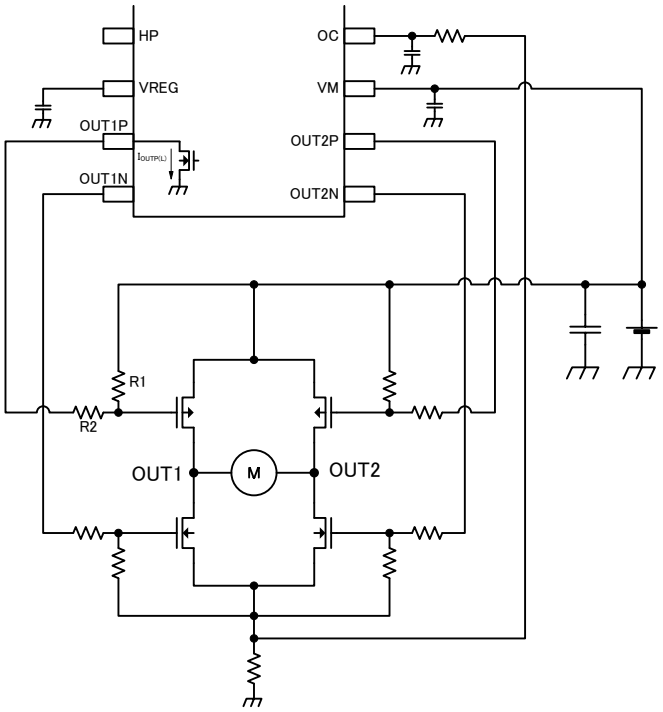


Figure 5.1 Application circuit example of drive external FETs (12V/24V power supply)

For example, when R1=1kΩ, V_{GP} can be calculated as follows,

V_{GP} = R1 × $I_{OUTP\ (L)}$
= 1kΩ × 11mA (typ.)
= 11V

Since V_{GP} is generated by the voltage drop from the power supply, V_{GP} does not exceed VM. When the power supply voltage is low, V_{GP} decreases. Make sure V_{GP} can exceed the threshold voltage of the Pch FET for low voltage application.

R2 is used to reduce the power consumption of the IC.

When the power supply is 24V, the power consumption of the high side pre-driver can be calculated as follows,

P_{OUTP}= (VM – (R1+R2) × $I_{OUTP\ (L)}$) × $I_{OUTP\ (L)}$
= 143mW (R1=1kΩ, R2=0Ω)
= 22mW (R1=1kΩ, R2=1kΩ)

Using appropriate R2 can reduce the power consumption of the IC.

For high voltage application, for example VM=48V, an example of application circuit is shown as figure 5.2. Please use a transistor (Q1) to ensure the voltage applied to high-side pre-driver output will not exceed the absolute maximum rating.

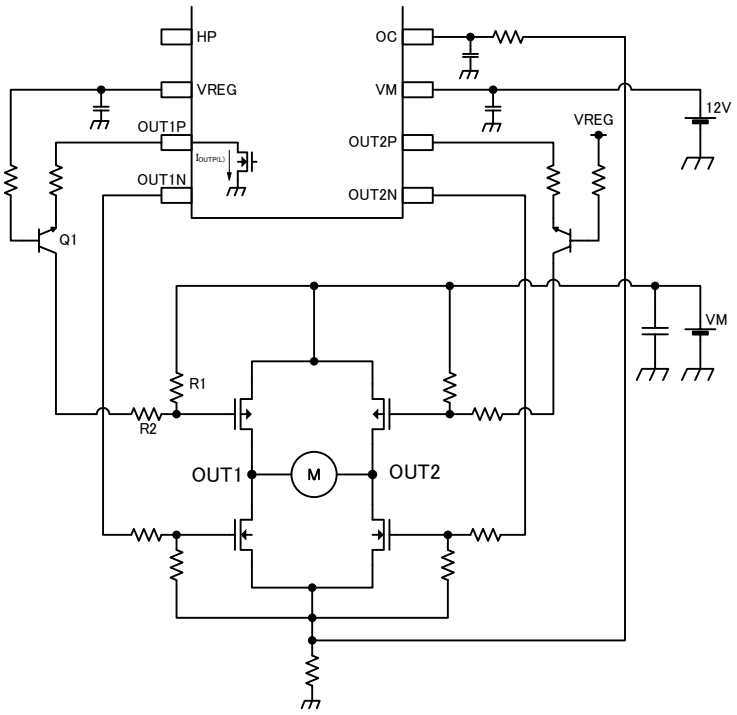


Figure 5.2 Application circuit of drive external FETs (48V power supply)

5.2. Low side pre-driver output

The low side pre-driver output of the TC78B006 series is a push-pull type. An internal voltage regulator is used to generate the gate drive voltage (V_{GN}), which is the voltage between the gate and the source of the external Nch FET. The output voltage ($V_{OUTN\ (H)}$) of the internal regulator drops from 10V when the power supply voltage is 12V or less. And the output capability of the internal regulator drops dramatically when VM is within the range of 3.5 to 5.5V. Make sure V_{GN} can exceed the threshold voltage of the Nch FET for low voltage application.

6. Protection functions

The TC78B006 series incorporate the following protection functions. The IC or external circuit is not protected by any cases.

6.1. Lock protection

Lock protection monitors motor rotation by the hall signal and operates when the zero cross of the hall signal cannot be detected for a certain term (T_{ON}) or more. When lock protection operates, the high side FET is turned off in the term of T_{ON}. Then, all FET are turned off. While the high side FET is turned off, the regenerative current is attenuated by low side regeneration.

The motor restarts after a certain term (T_{OFF}) from the lock protection operation. The output PWM duty starts from 20% if soft start is enabled.

Lock protection can be cleared when the voltage of TSP pin is set to low level for T_{stop} (100ms (typ.)) or more , or the voltage of VSP pin is set to $V_{VSP\ (L)}$ or less for T_{VSP} (10ms (typ.)) or more during lock protection term (T_{OFF}). After the lock protection is cleared, the motor operation restarts again without waiting for the end of the T_{OFF} term when TSP signal or VSP voltage is inputted.

Time of T_{ON} and T_{OFF} is set by CT pin. The lock protection can be set to disable when CT pin is connected to the ground directly.

6.2. Current limit

Current limit function turns off the high side external FET, when the current flowing through the motor is detected exceeding a certain threshold. The current limit threshold is determined by the shunt resistor (R_F) and the internal setting voltage.

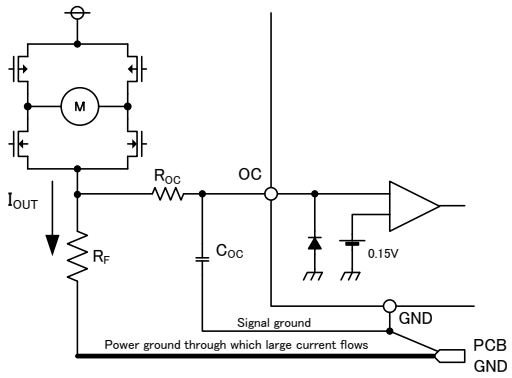


Figure 6.1 Setting of current limit

The internal setting voltage is 0.15V. When RF=0.1Ω, the current limit threshold is 1.5A

I_{OUT} = 0.15V / R_F
= 0.15V / 0.1Ω
= 1.5A

To disable the current limit function, short OC pin to GND.

Please note the power consumption of the shunt resistor.

P_R = 0.15V × 0.15V / R_F
= 0.15C × 0.15V / 0.1Ω
= 0.225W

Masking term of 1μs is provided for the measurement against the noise of R_F voltage signal. Even if R_F voltage exceeds 0.15V during masking term, the current limit circuit does not operate. A low-pass filter consisted of R_{OC} and C_{OC} can also be used to reduce the noise of R_F voltage signal. The ground of C_{OC} should be connected to the signal ground line, as same as the GND pin of the IC. The signal ground line should be separated from the power ground line through which large motor current flows. These two ground lines should be connected together on the GND pad of the PCB, where the power supply smoothing capacitor is placed.

6.3. Thermal shutdown (TSD)

The thermal shutdown circuit (TSD) operates when junction temperature (T_j) exceeds 165°C (typ.). Output is in PWM OFF state (both two high side external FETs are turned off, one low side FET is turned off while the other is kept on), until switching of the hall signal is detected for 3 times or its frequency is detected 5Hz or less. After that, all of external FETs are turned off. It has a hysteresis of 40°C (typ.). The operation resumes automatically when the temperature falls to 125°C (typ.) or less.

6.4. Under voltage lockout (UVLO)

The power supply voltage of VM is always monitored. When it falls to 2.9V (typ.) or less, it is recognized as low voltage and the circuit is turned off. The normal operation resumes when the voltage recovers to 3.2V (typ.) or more.

In normal operation, the voltage of VREG is also monitored. When it falls to 2.75V (typ.) or less, it is recognized as low voltage and the circuit is turned off. The normal operation resumes when the voltage recovers to 2.95V (typ.) or more.

7. Power consumption of the IC

The power consumption of the IC when it operates in standby mode can be estimated as follows,

$P_{(stby)} = VM \times I_{VM\_ST}$

When VM=12V, $P_{(stby)}$ =6mW. When VM=24V, $P_{(stby)}$ =12mW.

The power consumption of the IC when it operates in normal mode can be estimated as follows,

$P_{(norm)} = P_{(logic)} + P_{(reg)} + P_{(pre)}$

$P_{(norm)}$: Total power consumption of the IC when it operates in normal mode
$P_{(logic)}$: Power consumption of logic block
$P_{(reg)}$: Power consumption of internal regulator
$P_{(pre)}$: Power consumption of pre-driver output

- Power consumption of logic block
  It can be estimated as follows,

  $P_{(logic)} = VM \times I_{VM}$

  When VM=12V, $P_{(logic)}$ =54mW. When VM=24V, $P_{(logic)}$ =108mW

- Power consumption of internal regulator
  When using internal regulator output of V_{REG} as power supply of external parts, such as hall element, the power consumption can be estimated as follows,

  $P_{(reg)} = (VM - 5V) \times I_{VREG}$

  In case of assuming total output current I_{VREG} is 5mA,
  when VM=12V, $P_{(reg)}$=35mW. When VM=24V, $P_{(reg)}$ =95mW

- Power consumption of pre-driver output
  It can be estimated as follows,

  $P_{(pre)} = V_{OUTP\ (L)} \times I_{OUTP\ (L)} \times Duty$

  $V_{OUTP\ (L)}$: Remain voltage on high side pre-driver output when external Pch FET is turned on
  $I_{OUTP\ (L)}$: Sink current of high side pre-driver output
  Duty: Output PWM duty

  In case of assuming $V_{OUTP(L)}$ is 1V, and output PWM duty is 100% without soft switching,
  $P_{(pre)}$=11mW

  Soft switching function changes the output PWM duty gradually before and after the switching of the conduction phase. Therefore, when the peak of output PWM duty is the same, the power consumption of the pre-driver output with soft switching becomes less than that without soft switching.

- Total power consumption of the IC
  By accumulating the above results, the total power consumption of the IC is as follows,
  When VM=12V, $P_{(norm)}$ =100mW. When VM=24V, $P_{(norm)}$ =214mW.

  The junction temperature of the IC can be estimated as follows,

VM=12V $P_{(norm)}$ =100mW

Ta(°C) \ Tj(°C)	FNG $R_{th(j-a)}$=130°C/W	FTG $R_{th(j-a)}$=140°C/W
0	13	14
25	38	39
60	73	74
85	98	99

VM=24V $P_{(norm)}$=214mW

Ta(°C) \ Tj(°C)	FNG $R_{th(j-a)}$=130°C/W	FTG $R_{th(j-a)}$=140°C/W
0	28	30
25	53	55
60	88	90
85	113	115

Note: Ta: ambient temperature. Tj: junction temperature
Thermal resistance $R_{th\ (j-a)}$ is for reference. The value depends on PCB conditions.

When VM is high, reducing the power consumption of the internal regulator can help reducing the total power consumption. Using VM as the power supply of the hall element is useful to reduce the power consumption of the internal regulator.

Please design heat dissipation with enough margins after evaluating the thermal design for the board by referring to the above calculated values.

8. Notes in designing PCB

Please pay attention to the followings in designing PCB layout.

・Power and GND lines are made as wide as possible to reduce impedance.

・Output lines from the external FET are made as wide as possible.

・Smoothing capacitors are place as close as possible to the IC pins and FETs, respectively.

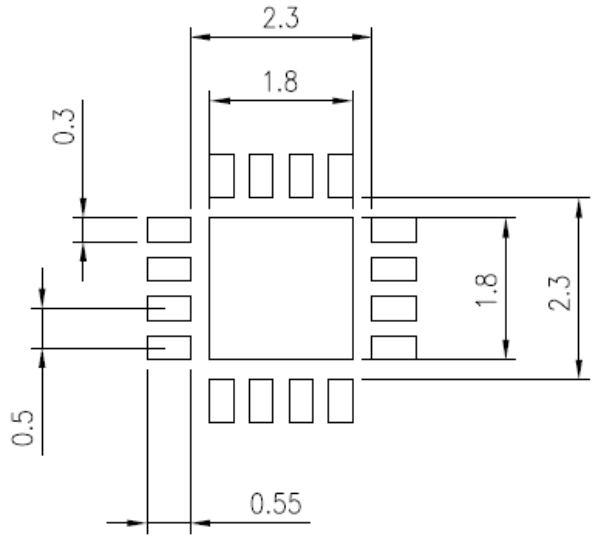
・The GND pin of the IC should be connected to the signal ground. The ground of FET should be connected to the power ground. These two grounds should be connected to a common grounding point not to have common impedance. Please place a smoothing capacitor to the common ground.

・For QFN package, heat generated in the IC can be dissipated efficiently by releasing it from the thermal pad on the bottom of the IC to the GND pattern of the board. Therefore, please secure GND pattern area near the IC as much as possible. In the case of a multilayer board, please place a thermal vias to reduce the thermal resistance between layers.

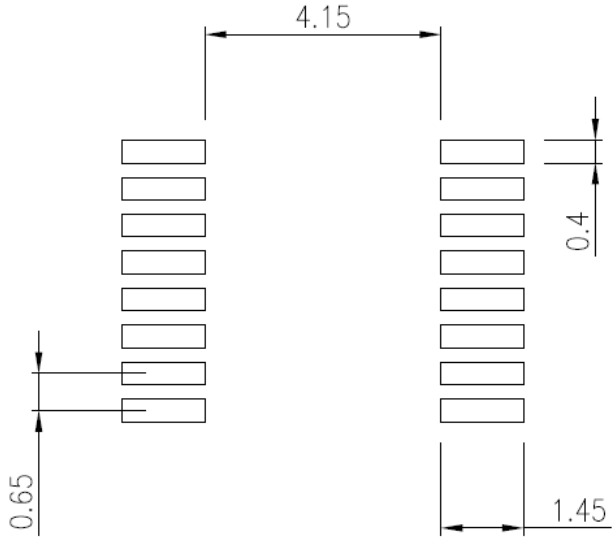
In designing board, the land pattern size for reference is shown below.

Unit: mm

P-WQFN16-0303-0.50-002



SSOP16-P-225-0.65B



Cautions

- As long as there is no indication in particular, the unit of the size is a millimeter.
- The figures are for reference according to JEITA ET-7501 Level 3.
  The accuracy of figures and information, and completeness are not guaranteed.
- Please evaluate various conditions (soldering conditions etc.) enough, and adjust them in a customer's responsibility.
- The figures of this document do not show actual form or size correctly. Please do not design estimating the size by measurement etc. with the value from figures.
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Notes on Contents

1. Block Diagrams
Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. Equivalent Circuits
The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

3. Timing Charts
Timing charts may be simplified for explanatory purposes.

4. Application Circuits
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5. Test Circuits
Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

IC Usage Considerations

Notes on handling of ICs

[1] The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.

[2] Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

[3] If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition.
Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

[4] Do not insert devices in the wrong orientation or incorrectly.
Make sure that the positive and negative terminals of power supplies are connected properly.
Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.

Points to remember on handling of ICs

(1) Over current Protection Circuit

Over current protection circuits (referred to as current limiter circuits) do not necessarily protect ICs under all circumstances. If the over current protection circuits operate against the over current, clear the over current status immediately.

Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the over current protection circuit to not operate properly or IC breakdown before operation. In addition, depending on the method of use and usage conditions, if over current continues to flow for a long time after operation, the IC may generate heat resulting in breakdown.

(2) Thermal Shutdown Circuit

Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over temperature, clear the heat generation status immediately.

Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the thermal shutdown circuit to not operate properly or IC breakdown before operation.

(3) Heat Radiation Design

In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (T_j) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into considerate the effect of IC heat radiation with peripheral components.

(4) Back-EMF

When a motor rotates in the reverse direction, stops or slows down abruptly, a current flow back to the motor's power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond absolute maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

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