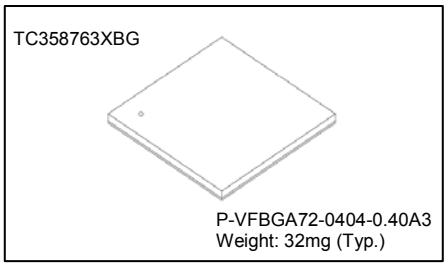
CMOS Digital Integrated Circuit Silicon Monolithic

TC358763XBG

Mobile Peripheral Devices



Overview

TC358763XBG provides data conversion between multiple input formats to a specified output format for mobile display systems. As the middle-range to high-end mobile phone sets are going to integrate higher-resolution, wider color depth, and larger size display in the clam-shell style body, connection between base body and display system is getting more difficult

TC358763XBG supports MIPI® DSI (Display Serial Interface) as a LCD interface. TC358763XBG also supports conventional LCD interface protocols; MIPI-DPI (Display Port Interface), MIPI-DBI (Display Bus Interface) as Host interface.

TC358763XBG can support 24-bit RGB Color format up to XGA size LCD module, when DPI is selected as Host interface. It also supports many different color format, and different LCD resolutions.

By using latest power saving technology, TC358763XBG can be controlled to minimize the power consumption in the target system.

Features

- LCD module interface
  - MIPI DSI-TX Data 3-lane, CLK 1-lane with data rates up to 500Mbps/lane
  - ✧ Support up to XGA size LCD panel. (When DPI is selected as host interface)
  - ✧ Output format: RGB888, RGB666 and RGB565.
  - ✧ Maximum LCD resolution setting size: 1024 × 1024
- Host interface
  - ✧ MIPI DPI 24-bit bus interface
  - ✧ MIPI DBI Type-B 16-bit bus interface
  - ✧ Serial input interface
    - 3 or 4-wire 8-bit SPI synchronous transfer
    - 3-wire 9-bit SSI synchronous transfer
- Peripheral control ports
  - ✧ SPI or SSI serial I/F ports
  - ✧ Single I^2C serial I/F port
  - ✧ Up to 13 General Purpose I/O ports
  - ✧ One PWM signals for LED intensity control
- PLL with 9.6MHz to 40MHz external reference clock to generate internal clock.
- Power supply
  - ✧ Core: 1.2 V ± 0.1 V
  - ✧ DSI I/O: 1.2 V ± 0.1 V
  - ✧ I/O: 1.8 V ± 0.1 V to 3.0 V ± 0.3 V
- Package
  - ✧ 4.5mm×4.5mm body, 72 ball, 0.4mm ball pitch, 1.0mm height (max)

Table of contents

List of Figures

List of Tables

- MIPI is registered trademarks of MIPI Alliance, Inc.

NOTICE OF DISCLAIMER

The material contained herein is not a license, either expressly or impliedly, to any IPR owned or controlled by any of the authors or developers of this material or MIPI. The material contained herein is provided on an “AS IS” basis and to the maximum extent permitted by applicable law, this material is provided AS IS AND WITH ALL FAULTS, and the authors and developers of this material and MIPI hereby disclaim all other warranties and conditions, either express, implied or statutory, including, but not limited to, any (if any) implied warranties, duties or conditions of merchantability, of fitness for a particular purpose, of accuracy or completeness of responses, of results, of workmanlike effort, of lack of viruses, and of lack of negligence.

All materials contained herein are protected by copyright laws, and may not be reproduced, republished, distributed, transmitted, displayed, broadcast or otherwise exploited in any manner without the express prior written permission of MIPI Alliance. MIPI, MIPI Alliance and the dotted rainbow arch and all related trademarks, tradenames, and other intellectual property are the exclusive property of MIPI Alliance and cannot be used without its express prior written permission.

ALSO, THERE IS NO WARRANTY OF CONDITION OF TITLE, QUIET ENJOYMENT, QUIET POSSESSION, CORRESPONDENCE TO DESCRIPTION OR NON-INFRINGEMENT WITH REGARD TO THIS MATERIAL OR THE CONTENTS OF THIS DOCUMENT. IN NO EVENT WILL ANY AUTHOR OR DEVELOPER OF THIS MATERIAL OR THE CONTENTS OF THIS DOCUMENT OR MIPI BE LIABLE TO ANY OTHER PARTY FOR THE COST OF PROCURING SUBSTITUTE GOODS OR SERVICES, LOST PROFITS, LOSS OF USE, LOSS OF DATA, OR ANY INCIDENTAL, CONSEQUENTIAL, DIRECT, INDIRECT, OR SPECIAL DAMAGES WHETHER UNDER CONTRACT, TORT, WARRANTY, OR OTHERWISE, ARISING IN ANY WAY OUT OF THIS OR ANY OTHER AGREEMENT, SPECIFICATION OR DOCUMENT RELATING TO THIS MATERIAL, WHETHER OR NOT SUCH PARTY HAD ADVANCE NOTICE OF THE POSSIBILITY OF SUCH DAMAGES.

Without limiting the generality of this Disclaimer stated above, the user of the contents of this Document is further notified that MIPI: (a) does not evaluate, test or verify the accuracy, soundness or credibility of the contents of this Document; (b) does not monitor or enforce compliance with the contents of this Document; and (c) does not certify, test, or in any manner investigate products or services or any claims of compliance with the contents of this Document. The use or implementation of the contents of this Document may involve or require the use of intellectual property rights ("IPR") including (but not limited to) patents, patent applications, or copyrights owned by one or more parties, whether or not Members of MIPI. MIPI does not make any search or investigation for IPR, nor does MIPI require or request the disclosure of any IPR or claims of IPR as respects the contents of this Document or otherwise.

Questions pertaining to this document, or the terms or conditions of its provision, should be addressed to:

MIPI Alliance, Inc.
c/o IEEE-ISTO
445 Hoes Lane
Piscataway, NJ 08854
Attn: Board Secretary

REFERENCES

1. MIPI Alliance Specification for D-PHY, Version 0.90.00 (October 8, 2007)
2. MIPI Alliance Specification for Display Serial Interface, Version 1.01.00 (February 21, 2008)
3. MIPI Alliance Specification for Display Bus Interface, Version 2.00 (November 29, 2005)
4. MIPI Alliance Specification for Display Pixel Interface(DPI-2), Version 2.00 (September 15, 2005)

1. Overview

TC358763XBG provides data conversion between multiple input formats to a specified output format for mobile display systems. As the middle-range to high-end mobile phone sets are going to integrate higher-resolution, wider color depth, and larger size display in the clam-shell style body, connection between base body and display system is getting more difficult

TC358763XBG supports MIPI DSI (Display Serial Interface) as a LCD interface. TC358763XBG also supports conventional LCD interface protocols; MIPI-DPI (Display Port Interface), MIPI-DBI (Display Bus Interface) as Host interface.

TC358763XBG can support 24-bit RGB Color format up to XGA size LCD module, when DPI is selected as Host interface. It also supports many different color format, and different LCD resolutions.

By using latest power saving technology, TC358763XBG can be controlled to minimize the power consumption in the target system.

Figure 1.1 shows the system overview and a block diagram of TC358763XBG.

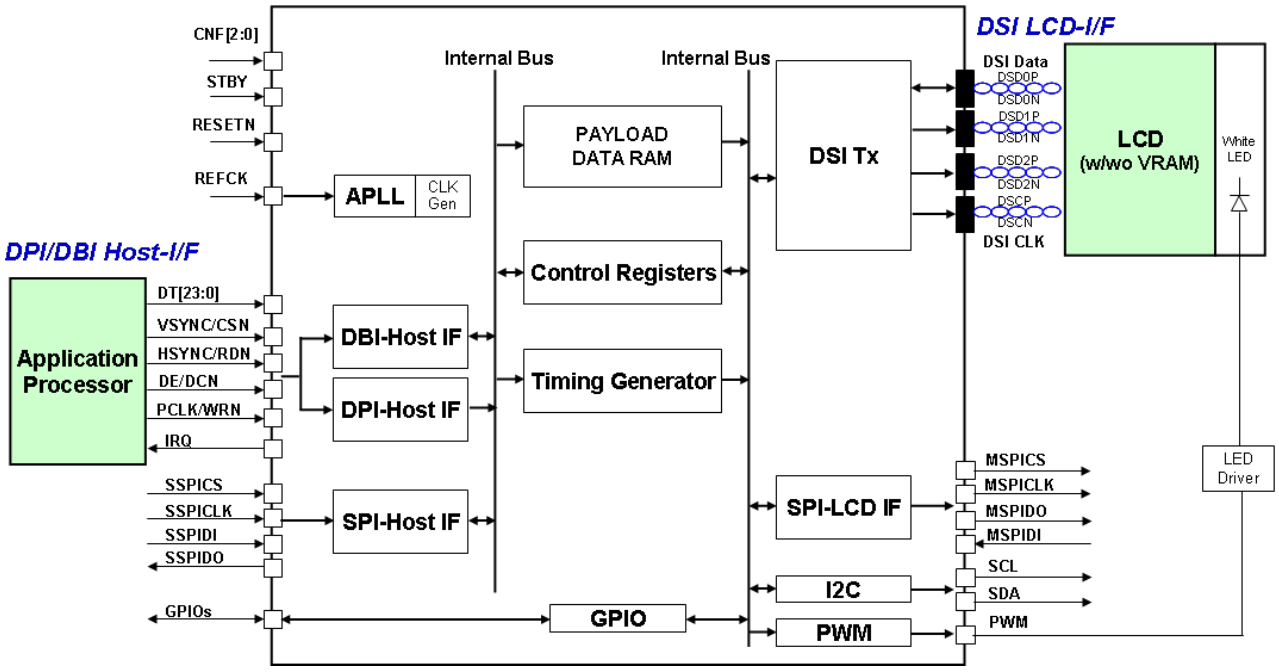


Figure 1.1 System Block Diagram of TC358763XBG

Pin Name Abbreviation:

GPIOs: GPIO0 to GPIO6

2. Features

- LCD module interface
  - MIPI DSI-TX Data 3-lane, CLK 1-lane with data rates up to 500Mbps/lane
  - ✧ Support up to XGA size LCD panel. (When DPI is selected as host interface)
  - ✧ Output format: RGB888, RGB666 and RGB565.
  - ✧ Maximum LCD resolution setting size: 1024 × 1024

- Host interface
  - ✧ MIPI DPI 24-bit bus interface
  - ✧ MIPI DBI Type-B 16-bit bus interface
  - ✧ Serial input interface
    - 3 or 4-wire 8-bit SPI synchronous transfer
    - 3-wire 9-bit SSI synchronous transfer

- Peripheral control ports
  - ✧ SPI or SSI serial I/F ports
  - ✧ Single I^2C serial I/F port
  - ✧ Up to 13 General Purpose I/O ports
  - ✧ One PWM signals for LED intensity control

- PLL with 9.6MHz to 40MHz external reference clock to generate internal clock.

- Power supply
  - ✧ Core: 1.2 V ± 0.1 V
  - ✧ DSI I/O: 1.2 V ± 0.1 V
  - ✧ I/O: 1.8 V ± 0.1 V to 3.0 V ± 0.3 V

- Package
  - ✧ 4.5mm×4.5mm body, 72 ball, 0.4mm ball pitch, 1.0mm height (max)

3. External Pins

3.1. Pin layout

Top View

A1 VDDS	A2 DT10	A3 DT11	A4 AVSS	A5 AVSS	A6 AVSS	A7 AVSS	A8 VSSO	A9 VDDS
B1 VSSO	B2 DT9	B3 DE	B4 AVDD18	B5 AVSS	B6 AVDD12	B7 HSYNC	B8 DT12	B9 DT13
C1 PCLK	C2 STBY	C3 DT8	C4 GPIO1	C5 GPIO3	C6 VSYNC	C7 GPIO0	C8 DT14	C9 VDDC
D1 VDDC	D2 DT7	D3 CNF0	D4 No ball	D5 No ball	D6 No ball	D7 DT15	D8 DT16	D9 VSSC
E1 VSSC	E2 DT6	E3 GPIO4	E4 No ball	E5 No ball	E6 No ball	E7 GPIO2	E8 CNF2	E9 VSSO
F1 DT4	F2 DT3	F3 DT5	F4 No ball	F5 No ball	F6 No ball	F7 DT17	F8 DT20	F9 VDDS
G1 VSSO	G2 DT2	G3 GPIO5	G4 SCL	G5 DT21	G6 DT18	G7 DT19	G8 SDA	G9 REFCK
H1 VDDS	H2 DT1	H3 DSD0P	H4 DSCP	H5 VDDDS12	H6 DSD1P	H7 DSD2P	H8 RESETN	H9 DT22
J1 GPIO6	J2 DT0	J3 DSD0N	J4 DSCN	J5 VSSDS	J6 DSD1N	J7 DSD2N	J8 DT23	J9 CNF1

Figure 3.1 Ball layout (TC358763XBG)

3.2. Signal Description

Table 3.1 shows the signal functionality of TC358763XBG.

Notation for Table 3.1;

1. “I/O” column shows direction of pin
   “I” means input pin. “O” means output pin. “I/O” means “Input / Output” pin.
   “NA” means “not applicable”.
2. “Type” column shows the type of IO pin
   “CMOS” means “CMOS” type input or inout pin. “CMOS” inout supports drive current value selection from 1mA, 2mA, 3mA, and 4mA by register settings. “SMT” means “Schmitt” type input or inout pin with pull-up/down control. “SMT” inout is 2mA drive current. “OD” means “Open Drain” type input or inout pin. “P” means Power supply. “G” means Ground.
3. “Initial” column shows the initial setting after reset with STBY=”H”.
   “In” means “Input pin, without pull-up nor pull-up resistor”. “PD” means “Input with internal pull-down”. “PU” means “Input internal pull-up”.
   “L” means “Low level output”. “H” means “High level output”, “Hi-Z” means “Hi-Impedance”. “NA” means “not applicable”. “NC” means “no connection”. No connection pin should be open.

   When STBY=”L”, all pin except for GPIO6, is Hi-Impedance state.

   GPIO6 is “PD” state even if STBY=”L”.

Note: Pull-up and Pull-down register is implemented by MOS Tr. They work as register only when IO power (VDDS) is supplied.

Table 3.1 Signal Functionality of TC358763XBG

Group	Pin Name	Ball	I/O	Typ.	Initial	Function	Note
LSI Mode	CNF2	E8	I/O	SMT	In	LSI mode control pin, Configure Host Interface types	*1
	CNF1	J9	I/O	SMT	In		
	CNF0	D3	I/O	SMT	In		
Reset & Clock	RESETN	H8	I/O	SMT	In	System Reset Input L: Reset H: Operation	–
	REFCK	G9	I/O	CMOS	In	System Clock Input	–
	STBY	C2	I	CMOS	In	Sleep Enable L: Standby H: Operation	–
DBI/DPI	VSYNC	C6	I/O	CMOS	*4	This pin has multiple functions. DPI: VSYNC (Vertical synchronization signal) DBI Type B: CSN	–
	HSYNC	B7	I/O	CMOS	*4	This pin has multiple functions. DPI: HSYNC (Horizontal synchronization signal) DBI Type B: RDN	–
	DE	B3	I/O	CMOS	*5	This pin has multiple functions. DPI: DE (valid Data Enable) DBI Type B: DCN	–
	PCLK	C1	I/O	CMOS	*4	This pin has multiple functions. DPI: PCLK (Pixel Clock) DBI Type B: WRN	–
	DT[17:0]	-	I/O	CMOS	*5	Video Data. Bus width is selectable among 8, 16, 18 or 24 bits.	*2
GPIO	DT18	G6	I/O	CMOS	*5	This pin has multiple functions. DBI/DPI bus width select = 1: DT[18] DBI/DPI bus width select = 0: GPIO[7]	–
	DT19	G7	I/O	CMOS	*5	This pin has multiple functions. DBI/DPI bus width select = 1: DT[19] DBI/DPI bus width select = 0: GPIO[8]	–
	DT20	F8	I/O	CMOS	*5	This pin has multiple functions. DBI/DPI bus width select = 1: DT[20] DBI/DPI bus width select = 0: GPIO[9]	–
	DT21	G5	I/O	CMOS	*5	This pin has multiple functions. { DBI/DPI bus width select, GPIO10 Function Select} = {1, x}: DT[21] {0, 1}: IRQ {0, 0}: GPIO[10]	–
	DT22	H9	I/O	CMOS	*5	This pin has multiple functions. { DBI/DPI bus width select, GPIO11 Function Select} = {1, x}: DT[22] {0, 1}: PWM {0, 0}: GPIO[11]	–
	DT23	J8	I/O	CMOS	*5	This pin has multiple functions. { DBI/DPI bus width select, GPIO10 Function Select} = {1, x}: DT[23] {0, 1}: CLKOUT {0, 0}: GPIO[12]	–

	GPIO0	C7	I/O	SMT	*7	This pin has multiple functions. If CNF[2:0]=[001 or 010 or 011 or 100]:SSPICS else if GPIO0 Function Select [1:0] = [00]: GPIO0 [01]: IRQ [10]: PWM [11]: Reserved	
	GPIO1	C4	I/O	CMOS	*6	This pin has multiple functions. If CNF[2:0]=[001 or 010 or 011 or 100]:SSPICLK else if GPIO1 Function Select [1:0] = [00]: GPIO1 [01]: IRQ [10]: CLKOUT [11]: Reserved	
	GPIO2	E7	I/O	SMT	*7	This pin has multiple functions. If CNF[2:0]=[001 or 010 or 011 or 100]:SSPIDI else if GPIO2 Function Select [1:0] = [00]: GPIO2 [01]: IRQ [10]: TE [11]: Reserved	
	GPIO3	C5	I/O	CMOS	H	This pin has multiple functions. If CNF[2:0]=[001 or 010 or 011 or 100] & Slave SPI CS bypass output enable = [1] :SSPICS bypass output else if {Master SPI Enable} = [1]: MSPICS (Master SPI Chip Select) else GPIO3 Function Select} = [00]: GPIO3 [01]: CLKOUT [10]: Host image write line end pulse output [11]: Reserved	–
	GPIO4	E3	I/O	CMOS	L	This pin has multiple functions. {Master SPI Enable, GPIO4 Function Select} = [0,00]: GPIO4 [0,01]: PWM [0,10]: HDE output [0,11]: Reserved [1,xx]: MSPICLK (Master SPI Clock)	
	GPIO5	G3	I/O	CMOS	L	This pin has multiple functions. {Master SPI Enable, GPIO5 Function Select} = [0,0]: GPIO5 [0,1]: IIRQ [1,x]: MSPIDOI (Master SPI Data Out/In)	

	GPIO6	J1	I/O	SMT	PD	This pin has multiple functions.
						If CNF[2:0]=[001 or 010 or 011 or 100] {
						If {Slave SPI 4-wire Enable,
						Slave SPI CS bypass output enable} =
						[0, 1]: SSPICS bypass output
						[1, x]: SSPIDO (Slave SPI Data Out)
						}
						}
						else if {Master SPI Enable,
						Master SPI CS pin select,
						GPIO6 Function Select [2:0]} =
						[1, 1, xx]: MSPICS2 (Master SPI CS2)
						[1, 0, xx]: MSPIDI (Master SPI Data In)
						[0, x, 11]: IRQ
						[0, x, 10]: PWM
						[0, x, 01]: TE
						[0, x, 00]: GPIO6	

I2C (master)	SCL	G4	O	OD	Hi-Z	I^2C Clock signal (Master)	–
	SDA	G8	I/O	OD	Hi-Z	I^2C Data signal (Master)	
DSI special I/O	DSD0P	H3	I/O	NA	NA	DSI Data Lane 0 Positive Input/Output	*1
	DSD0N	J3	I/O	NA	NA	DSI Data Lane 0 Negative Input/Output	
	DSD1P	H6	O	NA	NA	DSI Data Lane 1 Positive Output	
	DSD1N	J6	O	NA	NA	DSI Data Lane 1 Negative Output	
	DSD2P	H7	O	NA	NA	DSI Data Lane 2 Positive Output	
	DSD2N	J7	O	NA	NA	DSI Data Lane 2 Negative Output	
	DSCP	H4	O	NA	NA	DSI Clock Positive Output	
	DSCN	J4	O	NA	NA	DSI Clock Negative Output	
Power & Ground	VDDC	-	-	P	NA	VDD for Internal Core(1.2 V)	*3
	VDDS	-	-	P	NA	VDD for I/O	
	VDDDS12	H5	-	P	NA	VDD for DSI Analog (1.2 V)	
	VSSDS	J5	-	G	NA	VSS for DSI	
	AVDD12	B6	-	P	NA	Internal Analog core Power Please connect to AVSS	
	AVDD18	B4	-	P	NA	Internal Analog core Power Please connect to AVSS	
	AVSS	-	-	G	NA	VSS for Internal Analog Core	
	VSSC	-	-	G	NA	Ground for Internal Core	
	VSSO	-	-	G	NA	Ground for I/O	

*1: CNF[2:0] pin is used for Operation mode configuration of TC358763XBG. LCD Interface Configuration is specified by register settings. Initial State will change by the CNF[2:0] setting.

Table 3.2 CNF[2:0] Host I/F Configuration (LSI Mode)

CNF[2:0]	LSI Mode	Host I/F Configuration	Initial State				Note
			*4	*5	*6	*7	
000	-	Reserved	-	-	-	-	LSI Test mode
001	-	Reserved	-	-	-	-	LSI Test mode
010	-	Reserved	-	-	-	-	LSI Test mode
011	Mode 2-1	DPI + SPI slave	In	In	In	In	-
100	Mode 2-2	DPI + SSI slave	In	In	In	In	-
101	Mode 3	DBI Type-B	In	In	L	PD	-
110	-	Reserved	-	-	-	-	LSI Test mode
111	-	Reserved	-	-	-	-	LSI Test mode

*2: DT[23:0] pin assignment

Table 3.3 DT[23:0] pin assignment

DT	Loc	DT	Loc	DT	Loc	DT	Loc	DT	Loc	DT	Loc
[23]	J8	[19]	G7	[15]	D7	[11]	A3	[7]	D2	[3]	F2
[22]	H9	[18]	G6	[14]	C8	[10]	A2	[6]	E2	[2]	G2
[21]	G5	[17]	F7	[13]	B9	[9]	B2	[5]	F3	[1]	H2
[20]	F8	[16]	D8	[12]	B8	[8]	C3	[4]	F1	[0]	J2

*3: VDD/VSS pin assignment

All VSS pins (VSSDS, VSSC,VSSO and AVSS) have to be connected to Ground. DSI analog power supply pin have to connect 1.2 V power supply for both with/without DSI use case.

Table 3.4 VDD/VSS pin assign

Name	Pin					Function
VDDC	C9	D1	-	-	-	VDD for Internal Core
VDDS	A1	A9	F9	H1	J5	VDD for I/O
VSSC	D9	E1	-	-	-	VSS for Internal Core
VSSO	A8	B1	E9	G1	-	VSS for I/O
AVSS	B5	A4	A5	A6	A7	VSS for Internal Analog Core

*A4, A5, A6, A7 can be tied to GND or can be left open.

*4 to *7: Refer to Initial state field of Table 3.2.

*8: If signals are not used, please connect as follows.

DT16 to DT23: GND

SDA and SCL: GND

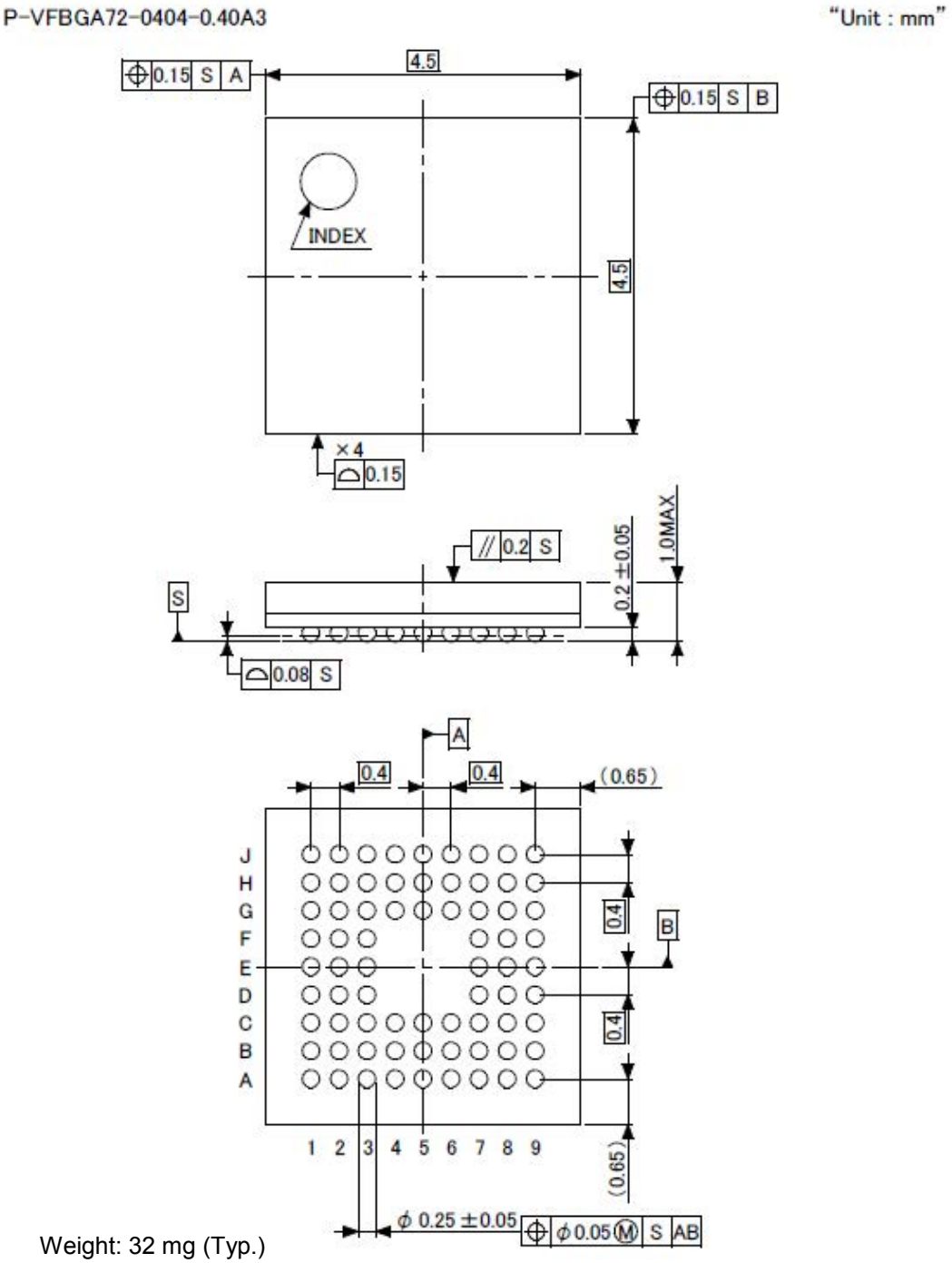
GPIO3 to GPIO6: Open

DSD1P, DSD1N, DSD2P, DSD2N: Open

GPIO0 to GPIO2: Open (Mode3 (CNF[2:0]=101) only)

4. Package

4.1. Package Dimensions (P-VFBGA72-0404-0.40A3)



Weight: 32 mg (Typ.)

Figure 4.1 Package Dimensions of TC358763XBG

5. Electrical Characteristics

5.1. Absolute Maximum Ratings

VSS= 0V reference

Table 5.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Power Supply voltage	VDDS	-0.3 to +3.9	V
	VDDDS12	-0.3 to +1.8	V
	VDDC	-0.3 to +1.8	V
Input voltage	VIN	-0.3 to VDDS+0.3	V
Output voltage	VOUT	-0.3 to VDDS+0.3	V
Input Current	IIN	-10 to +10	mA
Storage temperature	Tstg	-40 to +125	°C

5.2. Operating Condition

VSS= 0V reference

Table 5.2 Operation Condition

Parameter	Symbol	Min	Typ.	Max	Unit
Power Supply voltage	VDDS	1.7	-	3.3	V
	VDDDS12	1.1	1.2	1.3	
	VDDC	1.1	1.2	1.3	
Operating frequency (internal system clock)	Fopr	-	-	125	MHz
Operating temperature	Ta	-20	-	+85	°C

6. Revision History

Table 6.1 Revision History

Revision	Date	Description
1.60g	2014-04-10	Newly released
1.61	2016-04-01	Package's weight is rounding up digits after the decimal point to form an integer.
1.71	2017-11-09	Corrected *2 in section 3.2. Changed header, footer and the last page. Changed corporate name.

RESTRICTIONS ON PRODUCT USE

Toshiba Corporation and its subsidiaries and affiliates are collectively referred to as “TOSHIBA”.
Hardware, software and systems described in this document are collectively referred to as “Product”.

- TOSHIBA reserves the right to make changes to the information in this document and related Product without notice.
- This document and any information herein may not be reproduced without prior written permission from TOSHIBA. Even with TOSHIBA's written permission, reproduction is permissible only if reproduction is without alteration/omission.
- Though TOSHIBA works continually to improve Product's quality and reliability, Product can malfunction or fail. Customers are responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of Product could cause loss of human life, bodily injury or damage to property, including data loss or corruption. Before customers use the Product, create designs including the Product, or incorporate the Product into their own applications, customers must also refer to and comply with (a) the latest versions of all relevant TOSHIBA information, including without limitation, this document, the specifications, the data sheets and application notes for Product and the precautions and conditions set forth in the "TOSHIBA Semiconductor Reliability Handbook" and (b) the instructions for the application with which the Product will be used with or for. Customers are solely responsible for all aspects of their own product design or applications, including but not limited to (a) determining the appropriateness of the use of this Product in such design or applications; (b) evaluating and determining the applicability of any information contained in this document, or in charts, diagrams, programs, algorithms, sample application circuits, or any other referenced documents; and (c) validating all operating parameters for such designs and applications. **TOSHIBA ASSUMES NO LIABILITY FOR CUSTOMERS' PRODUCT DESIGN OR APPLICATIONS.**
- **PRODUCT IS NEITHER INTENDED NOR WARRANTED FOR USE IN EQUIPMENTS OR SYSTEMS THAT REQUIRE EXTRAORDINARILY HIGH LEVELS OF QUALITY AND/OR RELIABILITY, AND/OR A MALFUNCTION OR FAILURE OF WHICH MAY CAUSE LOSS OF HUMAN LIFE, BODILY INJURY, SERIOUS PROPERTY DAMAGE AND/OR SERIOUS PUBLIC IMPACT ("UNINTENDED USE").** Except for specific applications as expressly stated in this document, Unintended Use includes, without limitation, equipment used in nuclear facilities, equipment used in the aerospace industry, medical equipment, equipment used for automobiles, trains, ships and other transportation, traffic signaling equipment, equipment used to control combustions or explosions, safety devices, elevators and escalators, devices related to electric power, and equipment used in finance-related fields. **IF YOU USE PRODUCT FOR UNINTENDED USE, TOSHIBA ASSUMES NO LIABILITY FOR PRODUCT.** For details, please contact your TOSHIBA sales representative.
- Do not disassemble, analyze, reverse-engineer, alter, modify, translate or copy Product, whether in whole or in part.
- Product shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable laws or regulations.
- The information contained herein is presented only as guidance for Product use. No responsibility is assumed by TOSHIBA for any infringement of patents or any other intellectual property rights of third parties that may result from the use of Product. No license to any intellectual property right is granted by this document, whether express or implied, by estoppel or otherwise.
- **ABSENT A WRITTEN SIGNED AGREEMENT, EXCEPT AS PROVIDED IN THE RELEVANT TERMS AND CONDITIONS OF SALE FOR PRODUCT, AND TO THE MAXIMUM EXTENT ALLOWABLE BY LAW, TOSHIBA (1) ASSUMES NO LIABILITY WHATSOEVER, INCLUDING WITHOUT LIMITATION, INDIRECT, CONSEQUENTIAL, SPECIAL, OR INCIDENTAL DAMAGES OR LOSS, INCLUDING WITHOUT LIMITATION, LOSS OF PROFITS, LOSS OF OPPORTUNITIES, BUSINESS INTERRUPTION AND LOSS OF DATA, AND (2) DISCLAIMS ANY AND ALL EXPRESS OR IMPLIED WARRANTIES AND CONDITIONS RELATED TO SALE, USE OF PRODUCT, OR INFORMATION, INCLUDING WARRANTIES OR CONDITIONS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ACCURACY OF INFORMATION, OR NONINFRINGEMENT.**
- Do not use or otherwise make available Product or related software or technology for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). Product and related software and technology may be controlled under the applicable export laws and regulations including, without limitation, the Japanese Foreign Exchange and Foreign Trade Law and the U.S. Export Administration Regulations. Export and re-export of Product or related software or technology are strictly prohibited except in compliance with all applicable export laws and regulations.
- Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product. Please use Product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. **TOSHIBA ASSUMES NO LIABILITY FOR DAMAGES OR LOSSES OCCURRING AS A RESULT OF NONCOMPLIANCE WITH APPLICABLE LAWS AND REGULATIONS.**