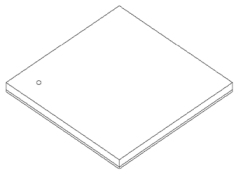
CMOS Digital Integrated Circuit Silicon Monolithic

# TC358767AXBG

**Mobile Peripheral Devices**

TC358767AXBG



P-VFBGA81-0505-0.50-001
Weight: 45mg (Typ.)

## Overview

TC358767AXBG is a bridge device that enables video streaming from a host (application or baseband processor) over MIPI® DSI$^{SM}$ or DPI$^{SM}$ link to drive DisplayPort$^{TM}$ display panels. TC358767AXBG also supports audio streaming from the host via I2S interface to the Display panels. TC358767AXBG provides a low power bridge solution to efficiently translate MIPI DSI or DPI transfers to DisplayPort$^{TM}$ transfers. As the DisplayPort$^{TM}$ uses fewer wires compared to other existing display panel standards, it simplifies the LCD connectivity. The effect of using TC358767AXBG is to enable existing baseband devices supporting DSI or DPI streaming to connect to new panels supporting DisplayPort$^{TM}$ interface and also to connect to existing panels over longer distance using DisplayPort$^{TM}$ adaptors at far-end. TC358767AXBG can interface to up to two independent devices.

## Features

- Translates MIPI DSI/DPI Link video stream from host to DisplayPort$^{TM}$ Link data to external display devices.
- The inputs are driven by a DSI Host with 4-Data Lanes, up to 1 Gbps/lane or DPI Host with 16/18/24-bits interface up to154 MHz parallel clock.
- Supports HDCP Digital Content Protection version 1.3 (DisplayPort$^{TM}$ amendment Rev1.1).
- Embeds audio information from the I2S port into the DisplayPort$^{TM}$ data stream.
- The output Interface consists of a DisplayPort$^{TM}$ Tx with a 2-lane Main Link and AUX-Ch.
- Register Configuration**:** From DSI link or I$^2$C interface.
- Interrupt to host to inform any error status or status needing attention from host.
- Internal test pattern (color bar) generator for DP o/p testing without any video (DSI/DPI) i/p.
- Debug/Test Port**:** I$^2$C Slave
- **DSI Receiver**
  - ✧ MIPI DSI**:** v1.01 / MIPI D-PHY$^{SM}$**:** v0.90 Compliant.
  - ✧ Up to four (4) Data Lanes with Bi-direction support on Data Lane 0.
  - ✧ Maximum speed at 1 Gbps/lane.
  - ✧ Supports Burst as well as Non-Burst Mode Video Data.
    - Video data packets are limited to one row per Hsync period.
  - ✧ Supports video stream packets for video data transmission.
  - ✧ Supports generic long packets for accessing the chip's register set.
  - ✧ Video input data formats**:**
    - RGB-565, RGB-666 and RGB-888.
    - New DSI V1.02 Data Type Support**:** 16-bit YCbCr 422
  - ✧ Interlaced video mode is not supported.
- **DPI Receiver**
  - ✧ Up to 16/18/24-bits parallel data interface.
  - ✧ Maximum speed at 154 MPs (MPixel per sec.).
  - ✧ Video input data formats**:** RGB-565, RGB-666 and RGB-888.
  - ✧ Only Progressive mode supported.
- **I2S Audio Interface:** Supports one I2S port for audio streaming from the host to TC358767AXBG.
  - ✧ Supports slave mode (BCLK, LRCLK & over-sampling clock input from Host).
  - ✧ Supports sampling frequencies of 32, 44.1, 48, 88.2, 96, 176.4 & 192 kHz.
  - ✧ Supports up to 2 audio channels.
  - ✧ Supports 16, 18, 20 or 24-bits per sample.
  - ✧ Optionally inserts IEC60958 status bits and preamble bits per channel.
- **DisplayPort$^{TM}$ Interface:** Supports a DisplayPort$^{TM}$ link from TC358767AXBG to display panels.
  - ✧ High speed serial bridge chip using VESA® DisplayPort$^{TM}$ 1.1a Standard.
  - ✧ Supports one dual-lane DisplayPort$^{TM}$ port for high bandwidth applications
  - ✧ Support 1.62 or 2.7 Gbps/lane data rate with voltage swings @0.4, 0.6, 0.8 or 1.2 V
  - ✧ Support of pre-emphasis levels of 0, 3.5dB and 6dB.

- ✧ Supports Audio related Secondary Data Packets.
- ✧ AUX channel supported at 1 Mbps.
- ✧ HPD support through GPIO[0] based interrupts
- ✧ Enhanced mode supported for content protection.
- ✧ Support HDCP encryption Version 1.3 with DisplayPort™ amendment Revision 1.1.
- ✧ Secure ASSR (Alternate Scrambler Seed Reset) support for eDP panels
  - System designer connects ASSR_DisablePad to VSS to enable eDP panels and ASSR
  - Drive ASSR_DisablePad with an inner ring VDDS for using DP panels and disable ASSR
  - System software read Revision ID field, 0x0500 [7:0]:
    - ➢ 0x01 indicates eDP panels are used, DPCD register bit 0x0010A [0] of eDP panel should be set
    - ➢ 0x03 assumes DP panels are connected, DPCD register bit 0x0010A [0] of DP panel should Not be set
- ✧ Stream Policy Maker is assumed handled by the Host (software/firmware).
  - Start Link training in response to HPD & read final Link training status
  - Configure DP link for actual video streaming & start video streaming
- ✧ Link Policy maker is assumed shared between the Host and TC358767AXBG chip.
  - In auto_correction = 0 mode, control link training
  - Initiate Display device capabilities read and configure TC358767AXBG accordingly.
- ✧ Video timing generation as per panel requirement.
- ✧ SSCG with up to 30 kHz modulation to reduce EMI.
- ✧ Toshiba Magic Square algorithm – RGB666 18b produces RGB888 24b like quality (with up to 16-million colors).
- ✧ Built in PRBS7 Generator to test DisplayPort™ Link.

- **RGB Parallel Output Interface:**
  - ✧ RGB888 output (DisplayPort™ disabled) with only DSI input supported in this mode
  - ✧ PCLK max. = 100 MHz
  - ✧ Polarity control for PCLK, VSYNC, HSYNC & DE
- **I²C Interface:**
  - ✧ I²C slave interface for chip register set access enabled using a boot-strap option.
  - ✧ I²C compliant slave interface support for normal (100 kHz) and fast mode (400 kHz).
- **GPIO Interface:**
  - ✧ 2 bits of GPIO (shared with other digital logic).
  - ✧ Direction controllable by Host I²C accesses.
- **Clock Source:**
  - ✧ DisplayPort™ clock source is from an external clock input or clock from DSI interface (13, 26, 19.2 or 38.4 MHz) – generates all internal & output clocks to interfacing display devices.
  - ✧ Built-in PLLs generate high-speed DisplayPort™ link clock requiring no external components. These PLLs are part of the DisplayPort™ PHY.
- Clock and power management support to achieve low power states.
- **Possible modes of Operation:**
  - ✧ MODE S21: TC358767AXBG uses DisplayPort™ Tx as single 2-lane DisplayPort™ link to interface to single DisplayPort™ display device. Video stream source is from MIPI DSI Host.
  - ✧ MODE P21: TC358767AXBG uses DisplayPort™ Tx as single 2-lane DisplayPort™ link to interface to single DisplayPort™ display device. Video stream source is from MIPI DPI Host.
  - ✧ MODE S2P: TC358767A uses only Parallel output port and disables DisplayPort™ Tx to interface to single RGB display device. Video stream source is from MIPI DSI Host.
- **Power supply inputs**
  - ✧ Core and MIPI D-PHY: 1.2 V ± 0.06 V
  - ✧ Digital I/O: 1.8 V ± 0.09 V
  - ✧ DisplayPort™: 1.8 V ± 0.09 V
  - ✧ DisplayPort™: 1.2 V ± 0.06 V
- **Power Consumption (Typical value based on estimation)**
  - ✧ Power-down mode (DSI-Rx in ULPS, DP PHY & PLLs disabled, clocks stopped):
    - DSI Rx: 0.01 mW
    - DP PHY: 2.34 mW
    - PLL9: 0.01 mW
    - Core: 0.96 mW
    - Rest: 0.01 mW
  - ✧ Normal operation (1920 × 1080 resolution with DSI-Rx in 4-lane @925 Mbps per lane, DP PHY in dual lane link @2.7 Gbps per lane):
    - DSI Rx: 21.79 mW
    - DP PHY: 142.70 mW
    - PLL9: 2.42 mW
    - Core: 87.64 mW
    - IOs: 1.68 mW
- **Package**
  - 0.5mm ball pitch, 81 balls, 5 × 5 mm BGA package

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## REFERENCES


1. MIPI® DSI℠, "MIPI Alliance Specification for DSI Version 1.01.00 - 21 February 2008"
2. MIPI® DPI℠, “MIPI Alliance Standard for Display Pixel Interface (DPI-2) Version 2.00 – 15 September 2005”
3. MIPI® D-PHY℠, “DRAFT MIPI Alliance Specification for D-PHY Version 0.91.00 – r0.01 14-March-2008"
4. VESA® DisplayPort™ Standard (Version 1, Revision 1A January 11, 2008)
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6. Digital Content Protection LLC, HDCP (Version 1.3 with DisplayPort™ amendment Revision 1.1, Jan. 15 2010)
7. $I^2C$ bus specification, version 2.1, January 2000, Philips Semiconductor
8. Draft CEA-861-C, A DTV Profile for Uncompressed High Speed Digital Interfaces (Doc. Number: CEA-861rCv9.pdf (PNXXX)) Date: 05/04/2005
9. DisplayPort™ PHY DFT Strategy Specification Rev 1.3

# 1. Overview

The DSI/DPI to DisplayPort™ converter (TC358767AXBG) is a bridge device that enables video streaming from a Host (application or baseband processor) over MIPI DSI or DPI link to drive DisplayPort™ display panels. TC358767AXBG also supports audio streaming from the host via I2S interface to the Display panels. TC358767AXBG provides a low power bridge solution to efficiently translate MIPI DSI or DPI transfers to DisplayPort™ transfers. As the DisplayPort™ uses fewer wires compared to other existing display panel standards, it simplifies the LCD connectivity. The effect of using TC358767AXBG is to enable existing baseband devices supporting DSI or DPI streaming to connect to new panels supporting DisplayPort™ interface and also to connect to existing panels over longer distance using DisplayPort™ adaptors at far-end. TC358767AXBG can interface to up to two independent devices.

The chip can be configured through the DSI link by sending write/read register commands through DSI Generic Long Write packets. It can also be configured through the $I^2C$ Slave interface.

The DSI-RX receiver supports from 1 to 4-Lane configurations at bit rate up to 1 Gbps per lane. Host can transmit video in continuous video streaming mode. Host controls video timing by sending video frame and line sync events together with video pixel data; video data transmission can be burst or non-burst. Since the chip integrates only a small video buffer, Host still has to take care of transmitting pixel data at appropriate video line time in order to avoid buffer overflow (or underflow).

The DPI-Rx receiver supports 16, 18 or 24 bits parallel interface along with the required control signals for the Pixel clock and HSync/VSync/DE.

The TC358767AXBG also supports content protection using HDCP copy protection. (Option)

The DisplayPort™ transmitter supports data throughput at 1.62 Gbps or 2.7 Gbps per lane of main link.

TC358767AXBG supports three configuration modes. These modes mainly differ based on the source of input stream and number of display devices that TC358767AXBG can be connected to.

- Mode_S21**:** A system configuration where TC358767AXBG may typically be used is shown in Figure 1.1. In this configuration, the TC358767AXBG can support displays with resolution up to WUXGA (1920×1200) at 24bit, 60 fps or WUXGA (1920×1200) at 18bit, 60 fps. Video stream source is from DSI Host.

- Mode_P21**:** A system configuration where TC358767AXBG may typically be used is shown in Figure 1.2. This is similar to the Mode_S21 except that the video stream source is from DPI Host. In this configuration, the TC358767AXBG can support displays with resolution up to WUXGA (1920×1200) at 24bit, 60 fps.

- Mode_S2P**:** A system configuration where TC358767AXBG may typically be used is shown in Figure 1.3. In this mode, DisplayPort™ output is not used and the chip rather behaves as a DSI to RGB convertor. In this system, TC358767AXBG could be connected to a single display. In this configuration, the TC358767AXBG can support displays with resolution up to WXGA (1280x800 or 1366x768). Max. output PCLK is 100 MHz. Video stream source is from DSI Host.

The chip supports power management to conserve power when its functions are not in use. Host manages the chip's power consumption modes by using ULPS messages over DSI link during DPI input mode.

The following figures show all these modes, where TC358767AXBG, display panels and a Host are connected in target Reference system for mobile large display panel applications.

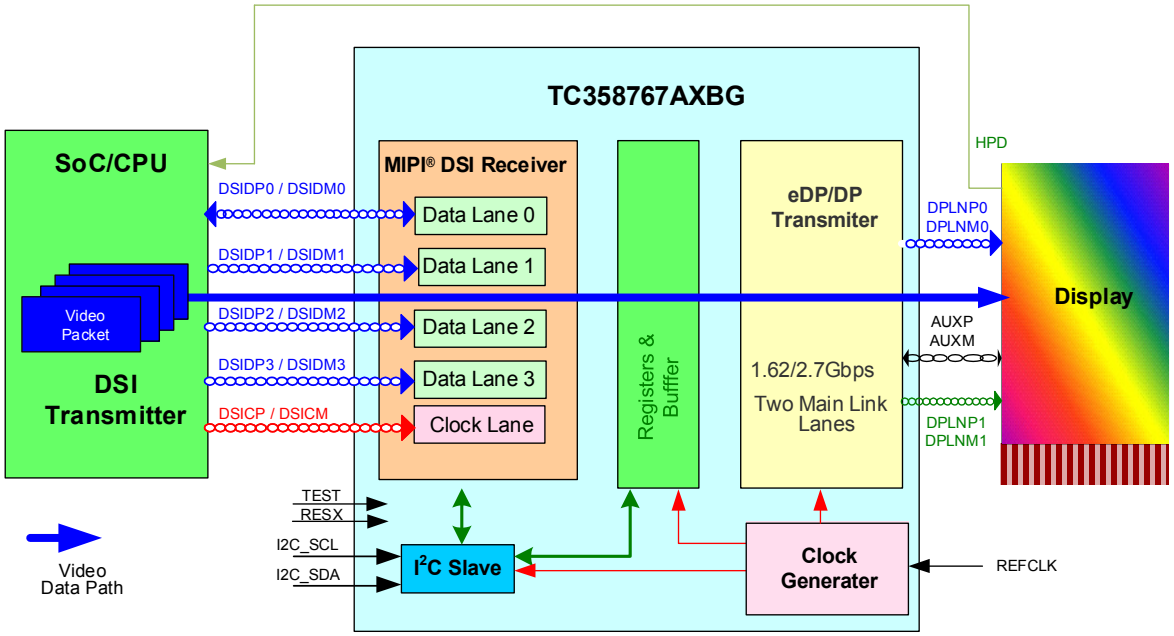



**Figure 1.1 System Overview with TC358767AXBG in MODE_S21 Configuration**

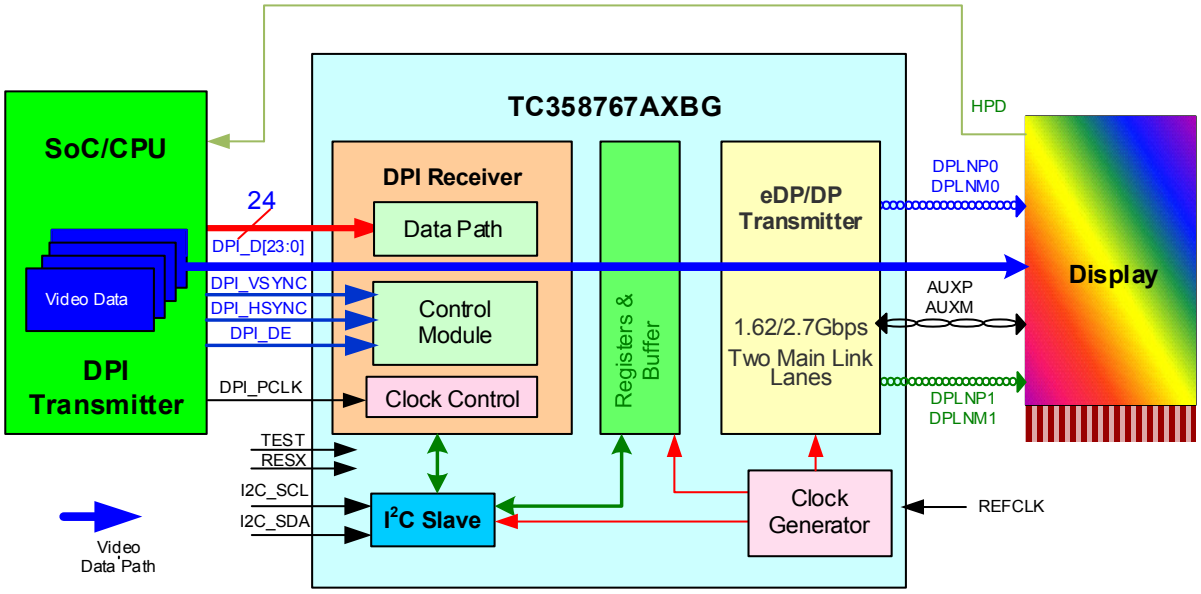



**Figure 1.2 System Overview with TC358767AXBG in MODE_P21 Configuration**

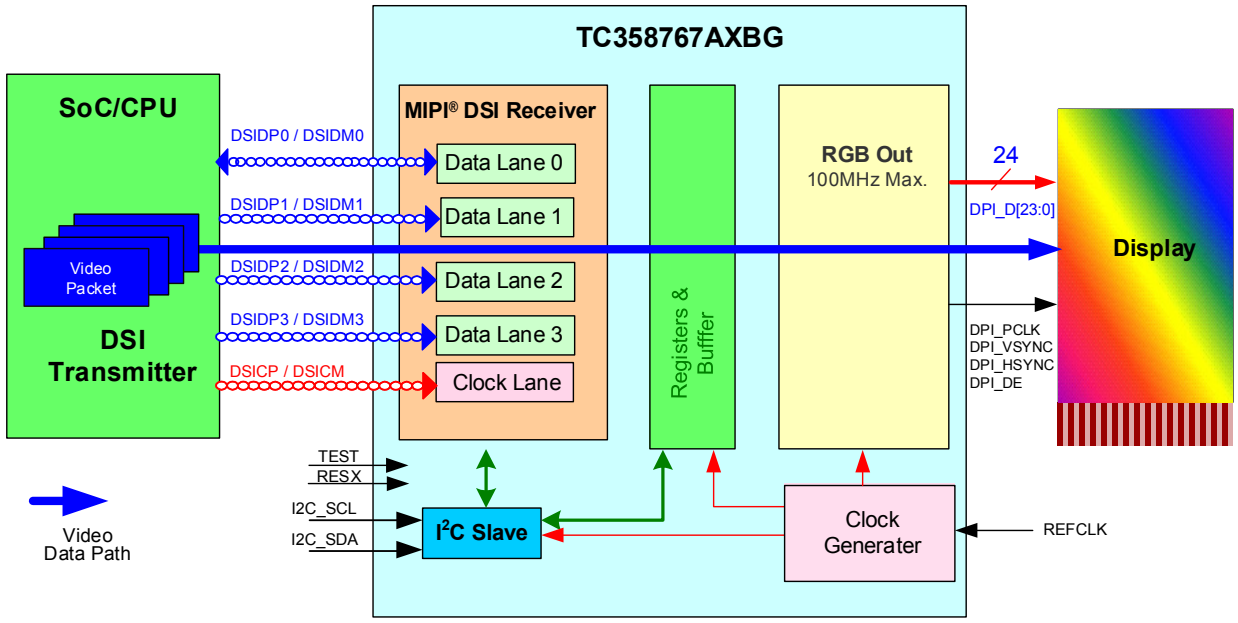



**Figure 1.3 System Overview with TC358767AXBG in MODE_S2P Configuration**

# 2. Features

Below are the main features supported by TC358767AXBG.

- Translates MIPI DSI/DPI Link video stream from Host to DisplayPort™ Link data to external display devices.
- The inputs are driven by a DSI Host with 4-Data Lanes, up to 1 Gbps/lane or DPI Host with 16/18/24 bit interface upto154 MHz parallel clock.
- Supports HDCP Digital Content Protection version 1.3 (DisplayPort™ amendment Rev1.1).
- Embeds audio information from the I2S port into the DisplayPort™ data stream.
- The output Interface consists of a DisplayPort™ Tx with a 2-lane Main Link and AUX-Ch.
- Register Configuration**:** From DSI link or I²C interface.
- Interrupt to host to inform any error status or status needing attention from Host.
- Internal test pattern (color bar) generator for DP o/p testing without any video (DSI/DPI) i/p.
- Debug/Test Port**:** I²C Slave
- **DSI Receiver**
  - ✧ MIPI DSI**:** v1.01 / MIPI D-PHY**:** v0.90 Compliant.
  - ✧ Up to four (4) Data Lanes with Bi-direction support on Data Lane 0.
  - ✧ Maximum speed at 1 Gbps/lane.
  - ✧ Supports Burst as well as Non-Burst Mode Video Data.
    - Video data packets are limited to one row per Hsync period.
  - ✧ Supports video stream packets for video data transmission.
  - ✧ Supports generic long packets for accessing the chip's register set.
  - ✧ Video input data formats**:**
    - RGB-565, RGB-666 and RGB-888.
    - New DSI V1.02 Data Type Support**:** 16-bit YCbCr 422
  - ✧ Interlaced video mode is not supported.
- **DPI Receiver**
  - ✧ Up to 16 / 18 / 24 bit parallel data interface.
  - ✧ Maximum speed at 154 MPs (MPixel per sec).
  - ✧ Video input data formats**:** RGB-565, RGB-666 and RGB-888.
  - ✧ Only Progressive mode supported.
- **I2S Audio Interface:** Supports one I2S port for audio streaming from the host to TC358767AXBG.
  - ✧ Supports slave mode (BCLK, LRCLK & over-sampling clock input from Host).
  - ✧ Supports sampling frequencies of 32, 44.1, 48, 88.2, 96, 176.4 & 192 kHz.
  - ✧ Supports up to 2 audio channels.
  - ✧ Supports 16, 18, 20 or 24 bits per sample.
  - ✧ Optionally inserts IEC60958 status bits and preamble bits per channel.
- **DisplayPort™ Interface:** Supports a DisplayPort™ link from TC358767AXBG to display panels.
  - ✧ High speed serial bridge chip using VESA® DisplayPort™ 1.1a Standard.
  - ✧ Supports one dual-lane DisplayPort™ port for high bandwidth applications.
  - ✧ Support 1.62 or 2.7 Gbps/lane data rate with voltage swings @0.4, 0.6, 0.8 or 1.2 V.
  - ✧ Support of pre-emphasis levels of 0, 3.5 dB and 6 dB.
  - ✧ Supports Audio related Secondary Data Packets.
  - ✧ AUX channel supported at 1 Mbps.
  - ✧ HPD support through GPIO[0] based interrupts
  - ✧ Enhanced mode supported for content protection.
  - ✧ Support HDCP encryption Version 1.3 with DisplayPort™ amendment Revision 1.1.
  - ✧ Secure ASSR (Alternate Scrambler Seed Reset) support for eDP panels
    - System designer connects ASSR_DisablePad to VSS to enable eDP panels and ASSR
    - Drive ASSR_DisablePad with an inner ring VDDS for using DP panels and disable ASSR
    - System software read Revision ID field, 0x0500[7:0]**:**
      - ➢ 0x01 indicates eDP panels are used, DPCD register bit 0x0010A [0] of eDP panel should be set.
      - ➢ 0x03 assumes DP panels are connected, DPCD register bit 0x0010A [0] of DP panel should Not be set.

- ✧ Stream Policy Maker is assumed handled by the Host (software/firmware).
  - Start Link training in response to HPD & read final Link training status
  - Configure DP link for actual video streaming & start video streaming
- ✧ Link Policy maker is assumed shared between the Host and TC358767AXBG chip.
  - In auto_correction = 0 mode, control link training
  - Initiate Display device capabilities read and configure TC358767AXBG accordingly.
- ✧ Video timing generation as per panel requirement.
- ✧ SSCG with up to 30 kHz modulation to reduce EMI.
- ✧ Toshiba Magic Square algorithm – RGB666 18b produces RGB888 24b like quality (with up to 16-million colors).
- ✧ Built in PRBS7 Generator to test DisplayPort™ Link.

- **RGB Parallel Output Interface:**
  - ✧ RGB888 output (DisplayPort™ disabled) with only DSI input supported in this mode
  - ✧ PCLK max. = 100 MHz
  - ✧ Polarity control for PCLK, VSYNC, HSYNC & DE
- **I²C Interface:**
  - ✧ I²C slave interface for chip register set access enabled using a boot-strap option.
  - ✧ I²C compliant slave interface support for normal (100 kHz) and fast mode (400 kHz).
- **GPIO Interface:**
  - ✧ 2 bits of GPIO (shared with other digital logic).
  - ✧ Direction controllable by Host I²C accesses.
- **Clock Source:**
  - ✧ DisplayPort™ clock source is from an external clock input or clock from DSI interface (13, 26, 19.2 or 38.4 MHz) – generates all internal & output clocks to interfacing display devices.
  - ✧ Built-in PLLs generate high-speed DisplayPort™ link clock requiring no external components. These PLLs are part of the DisplayPort™ PHY.
- Clock and power management support to achieve low power states.
- **Possible modes of Operation:**
  - ✧ MODE S21: TC358767AXBG uses DisplayPort™ Tx as single 2-lane DisplayPort™ link to interface to single DisplayPort™ display device. Video stream source is from MIPI DSI Host.
  - ✧ MODE P21: TC358767AXBG uses DisplayPort™ Tx as single 2-lane DisplayPort™ link to interface to single DisplayPort™ display device. Video stream source is from MIPI DPI Host.
  - ✧ MODE S2P: TC358767AXBG uses only Parallel output port and disables DisplayPort™ Tx to interface to single RGB display device. Video stream source is from MIPI DSI Host.
- **Power supply inputs**
  - ✧ Core and MIPI D-PHY: 1.2 V ± 0.06 V
  - ✧ Digital I/O: 1.8 V ± 0.09 V
  - ✧ DisplayPort™: 1.8 V ± 0.09 V
  - ✧ DisplayPort™: 1.2 V ± 0.06 V
- **Power Consumption (Typical value based on estimation)**
  - ✧ Power-down mode (DSI-Rx in ULPS, DP PHY & PLLs disabled, clocks stopped):
    - DSI Rx: 0.01 mW
    - DP PHY: 2.34 mW
    - PLL9: 0.01 mW
    - Core: 0.96 mW
    - Rest: 0.01 mW
  - ✧ Normal operation (1920×1080 resolution with DSI-Rx in 4-lane @925 Mbps per lane, DP PHY in dual lane link @2.7 Gbps per lane):
    - DSI Rx: 21.79 mW
    - DP PHY: 142.70 mW
    - PLL9: 2.42 mW
    - Core: 87.64 mW
    - IOs: 1.68 mW

- **Package**
  - 0.5mm ball pitch, 81 balls, 5 × 5 mm BGA package

**Note:** Attention about ESD. This product is weak against ESD. Please handle it carefully.

**Table 2.1 TC358767AXBG operational modes summary with panel size support information**

| Mode | Input Configuration | | Register Access Method | Max Panel size example |
|---|---|---|---|---|
| | DSI input | DPI input | | |
| S21 | Active | X | DSI or $I^2C$ | WUXGA 18bpp @ 60fps<br>WUXGA 24bpp @ 60fps |
| P21 | X | Active | $I^2C$ | WUXGA 24bpp @ 60fps |

Tables below provide an idea of different panel sizes that can be supported by using different data link lane configurations.

**Table 2.2 Panel Size v/s Data link required by TC358767AXBG in DSI input case**

| Frame Size | | | FPS | Pixel Clock (MHz) | RGB666 | | | | RGB888 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | With OverHead | | | Bit Rate (Gbps) | # DSI Data lanes | # DP Main links | | Bit Rate (Gbps) | # DSI Data lanes | # DP Main links | |
| | | | | | | | 1.62G | 2.7G | | | 1.62G | 2.7G |
| XGA | 1024×768 | 1184×790 | 60 | 56 | 1.01 | 2 | 1 | 1 | 1.34 | 2 | 2 | 1 |
| WXGA+ / WSXGA | 1440×900 | 1600×926 | 60 | 89 | 1.60 | 2 | 2 | 1 | 2.13 | 3 | 2 | 1 |
| SXGA+ | 1400×1050 | 1560×1080 | 60 | 89 | 1.82 | 2 | 2 | 1 | 2.43 | 3 | 2 | 2 |
| WSXGA+ | 1680×1050 | 1840×1080 | 60 | 119 | 2.15 | 3 | 2 | 1 | 2.86 | 3 | – | 2 |
| UXGA | 1600×1200 | 1760×1235 | 60 | 130 | 2.35 | 3 | 2 | 2 | 3.13 | 4 | – | 2 |
| WUXGA | 1920×1200 | 2080×1235 | 60 | 154 | 2.77 | 3 | – | 2 | 3.70 | 4 | – | 2 |

**Table 2.3 Panel Size v/s Data link required by TC358767AXBG in DPI input case**

| Frame Size | | | FPS | Pixel Clock (MHz) | DPI Support 154 MHz PCLK | RGB666 | | | RGB888 | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | With OverHead | | | | Bit Rate (Gbps) | # DP Main links | | Bit Rate (Gbps) | # DP Main links | |
| | | | | | | | 1.62G | 2.7G | | 1.62G | 2.7G |
| XGA | 1024×768 | 1184×790 | 60 | 56 | Yes | 1.01 | 1 | 1 | 1.34 | 2 | 1 |
| WXGA+ / WSXGA | 1440×900 | 1600×926 | 60 | 89 | Yes | 1.60 | 2 | 1 | 2.13 | 2 | 1 |
| SXGA+ | 1400×1050 | 1560×1080 | 60 | 89 | Yes | 1.82 | 2 | 1 | 2.43 | 2 | 2 |
| WSXGA+ | 1680×1050 | 1840×1080 | 60 | 119 | Yes | 2.15 | 2 | 1 | 2.86 | – | 2 |
| UXGA | 1600×1200 | 1760×1235 | 60 | 130 | Yes | 2.35 | 2 | 2 | 3.13 | – | 2 |
| WUXGA | 1920×1200 | 2080×1235 | 60 | 154 | Yes | 2.77 | – | 2 | 3.70 | – | 2 |

Note: These are the formats commonly used by displays. Support for other sizes is possible as long as they satisfy the maximum data rate constraints on the DSI and DisplayPort™ link interfaces.

**Note: Throughout the rest of the document, "DP" is used to denote "DisplayPort™". Both these words have been used interchangeably and refer to the VESA® DisplayPort™ specification as mentioned in the references.**

# 3. External Pins

## 3.1. TC358767AXBG External Pins

TC358767AXBG uses an 81pin package. Following table gives the signals of TC358767AXBG and their function.

**Table 3.1 TC358767AXBG Functional Signal List for 81-pin Package**

| Group | Pin Name | I/O | Type | Function | Note |
|---|---|---|---|---|---|
| System: Reset, Clock, Mode select, Test (9) | RESX | I | Sch | System Reset – active Low<br>0: Reset<br>1: Normal operation | — |
| | REFCLK | I | Sch | 13, 26, 19.2 or 38.4 MHz<br>50ps phase jitter p2p / WC duty cycle 40 - 60% | — |
| | INT | O | N | Interrupt to Host – active High<br>0: No interrupt is generated<br>1: Interrupt is generated | 4mA |
| | DISABLE_ASSR | I | N | ASSR control<br>0: Enable ASSR<br>1: Disable ASSR | — |
| | MODE[1:0] | I | N | Mode Selection pins<br>MODE_0:<br>0: REFCLK is source of internal DP PLL<br>1: When REFCLK = ”0”, DSI clock is source of internal DP PLL.<br>When REFCLK = ”1”, DPI PCLK is source of internal DP PLL.<br>MODE_1:<br>When MODE_0 = ”1” & REFCLK = ”0” this pin will be effective.<br>0: DSI clock/2/7 is source of internal DP PLL.<br>1: DSI clock/2/9 is source of internal DP PLL. | — |
| | TEST | I | N | Test Pin - active high<br>0: Normal operation<br>1: Test mode | — |
| | TEST3 | O | N | Test Pin, Open | — |
| | VPGM0 | NA | — | eFUSE programming voltage. Connect to GND | — |
| DSI Rx (10) | DSICP | I | MIPI-PHY | MIPI-DSI Rx Clock Lane Pos. | — |
| | DSICM | I | MIPI-PHY | MIPI-DSI Rx Clock Lane Neg. | — |
| | DSIDP0 | I/O | MIPI-PHY | MIPI-DSI Rx Data Lane Pos. | — |
| | DSIDM0 | I/O | MIPI-PHY | MIPI-DSI Rx Data Lane Neg. | — |
| | DSIDP[3:1] | I | MIPI-PHY | MIPI-DSI Rx Data Lane Pos. | — |
| | DSIDM[3:1] | I | MIPI-PHY | MIPI-DSI Rx Data Lane Neg. | — |
| DP Out (8) | DPLNP[1:0] | O | DP-PHY | embedded DisplayPort™ Output Main Link Pos. | — |
| | DPLNM[1:0] | O | DP-PHY | embedded DisplayPort™ Output Main Link Neg. | — |
| | DPAUXP | I/O | DP-PHY | embedded DisplayPort™ Output AUX Channel Pos. | — |
| | DPAUXM | I/O | DP-PHY | embedded DisplayPort™ Output AUX Channel Neg. | — |
| | PREC_RES[1:0] | I | DP-PHY | Precision Resistance (3kΩ @ 1%) connection | — |
| DPI Tx/Rx (28) | DPI_PCLK | I/O | N | DPI Pixel Clock (max 154 MHz) (default: Input) | 4mA |
| | DPI_VSYNC | I/O | N | DPI Vertical Sync (default: Input) | 4mA |
| | DPI_HSYNC | I/O | N | DPI Horizontal Sync (default: Input) | 4mA |
| | DPI_DE | I/O | N | DPI Data Enable (default: Input) | 4mA |
| | DPI_D[23:0] | I/O | N | DPI Parallel Data (default: Input) | 4mA |
| I²C (3) | I2C_SCL | OD | Sch | I²C Clock | — |
| | I2C_SDA | OD | Sch | I²C Data | 4mA |
| | I2C_ADR_SEL | I | N | I²C Slave Address Select<br>0: Slave address = 7’b1101_000<br>1: Slave address = 7’b0001_111 | — |

| | | | | | |
|---|---|---|---|---|---|
| I2S (4) | SD/I2S_OSCLK | I | N | I2S Over Sampling Clock | — |
| | I2S_BCLK | I | N | I2S Bit Clock (max 12.5 MHz) | — |
| | I2S_LRCLK | I | N | I2S sample clock (max 192 kHz) | — |
| | I2S_DATA | I | N | I2S Data | — |
| GPIO (2) | GPIO[1:0] | OD | 5T-OD | GPIO or Test Control Note1<br>GPIO[1:0] can be used for HPD support | 4mA |
| POWER (10) | VDDC (1.2V) | NA | — | VDD for Internal Core (2) | — |
| | VDDS (1.8V) | NA | — | VDDS for IO Ring power supply (1) | — |
| | VDD_PLL18 (1.8V) | NA | — | VDD for DP PHY PLLs (1) | — |
| | VDD_PLL12 (1.2V) | NA | — | VDD for DP PHY PLLs (1) | — |
| | VDD_DP18 (1.8V) | NA | — | VDD for DP PHY Main Channels (2) | — |
| | VDD_PLL912 (1.2V) | NA | — | VDD for PLL9 (1) | — |
| | VDD_DP12 (1.2V) | NA | — | VDD for DP PHY (1) | — |
| | VDD_DSI12 (1.2V) | NA | — | VDD for the MIPI DSI PHY (1) | — |
| GROUND (7) | VSS | NA | — | Ground (Core, I/O) (3) | — |
| | VSS_DSI | NA | — | Ground (DSI) (1) | — |
| | VSS_DP | NA | — | Ground (DP) (3) | — |

Total 81 pins TC358767AXBG BGA package.
Note 1: Pins with multiplexed Functional mode functions

N: Normal IO
FS: Fail safe IO - gated
PHY: Either DP analog front end or MIPI D-PHY
Sch: Schmitt trigger input
OD: Open drain
5T-OD: 5 V tolerant bi-direction buffer with Open drain
Pd: Pull Down

## 3.2. TC358767AXBG Pin Mapping

The mapping of TC358767AXBG signals to the external pins is given in the following figure. (BGA array)

**Top View (through the die)**

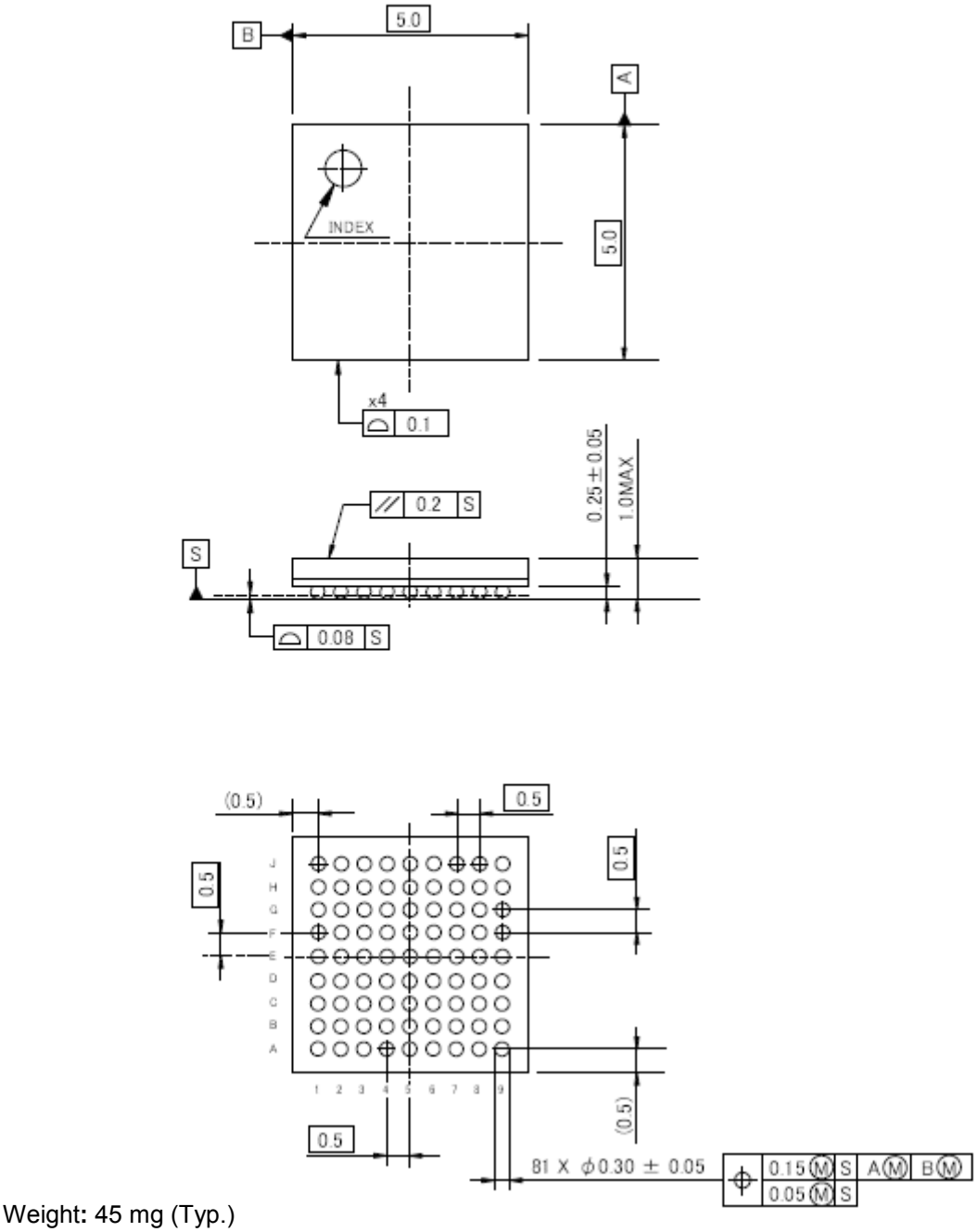
| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **A1** DSIDM_0 | **A2** DSIDP_0 | **A3** I2S_LRCLK | **A4** VDDC | **A5** VDDC | **A6** INT | **A7** VDDS | **A8** I2C_SDA | **A9** I2C_SCL |
| **B1** DSIDM_1 | **B2** DSIDP_1 | **B3** GPIO_0 | **B4** I2S_BCLK | **B5** I2S_DATA | **B6** MODE_0 | **B7** MODE_1 | **B8** GPIO_1 | **B9** I2C_ADR_SEL |
| **C1** DSICM | **C2** DSICP | **C3** DPI_DE | **C4** DPI_VSYNC | **C5** DPI_D_5 | **C6** DPI_D_7 | **C7** DPI_D_10 | **C8** TEST_3 | **C9** I2S_OSCLK |
| **D1** VDD_DSI12 | **D2** VSS_DSI | **D3** DPI_HSYNC | **D4** DPI_D_0 | **D5** VSS | **D6** DPI_D_9 | **D7** DPI_D_12 | **D8** DPI_D_13 | **D9** DSI_D_14 |
| **E1** DSIDM_2 | **E2** DSIDP_2 | **E3** DPI_D_1 | **E4** DPI_D_3 | **E5** VSS | **E6** VSS | **E7** DPI_D_16 | **E8** VPGM_0 | **E9** DPI_D_11 |
| **F1** DSIDM_3 | **F2** DSIDP_3 | **F3** DPI_D_2 | **F4** DPI_D_6 | **F5** DPI_D_8 | **F6** DPI_D_15 | **F7** DPI_D_18 | **F8** DPI_D_17 | **F9** DPI_D_20 |
| **G1** PREC_RES_0 | **G2** Disable_ASSR | **G3** DPI_D_4 | **G4** TEST | **G5** DPI_D_19 | **G6** DPI_PCLK | **G7** DPI_D_21 | **G8** DPI_D_23 | **G9** DPI_D_22 |
| **H1** PREC_RES_1 | **H2** VSS_DP | **H3** DPLNP_0 | **H4** VDD_DP12 | **H5** VSS_DP | **H6** DPLNP_1 | **H7** VSS_DP | **H8** DPAUXP_0 | **H9** VDD_PLL912 |
| **J1** REFCLK | **J2** VDD_DP18 | **J3** DPLNM_0 | **J4** VDD_PLL12 | **J5** VDD_PLL18 | **J6** DPLNM_1 | **J7** VDD_DP18 | **J8** DPAUXM_0 | **J9** RESX |

**Figure 3.1 TC358767AXBG 81-Pin Layout**

# 4. Package

The package for TC358767AXBG is described in the figure below.

P-VFBGA81-0505-0.50-001 "Unit:mm"




Weight: 45 mg (Typ.)

**Figure 4.1 81 pin TC358767AXBG package**

The mechanical dimension of BGA81 package is listed below.

**Table 4.1 Mechanical Dimension of P-VFBGA81-0505-0.50-001**

| Package | Solder Ball Pitch | Solder Ball Height | Package Dimension | Package Height | Note |
|---|---|---|---|---|---|
| 81-Pin | 0.50 mm | 0.25 mm | 5.0 × 5.0 $mm^2$ | 1.0 mm | — |

# 5. Electrical Characteristics

## 5.1. Absolute Maximum Ratings

VSS = 0 V reference
VDD18 used for VDDS as well as VDD-DP18; VDD12 used for VDDC as well as VDD-DSI12.

**Table 5.1 Absolute Maximum Ratings**

| Parameter | Symbol | Rating | Unit |
|---|---|---|---|
| **Supply voltage (1.8 V)** | VDD18 | -0.3 to +3.5 | V |
| **Supply voltage (1.2 V)** | VDD12 | -0.3 to +2.0 | V |
| **Supply voltage (IO)** | VDD18 | -0.3 to +3.5 | V |
| | VREF | -0.3 to +3.5 | V |
| **Input voltage** | VIN | -0.3 to VDDS+0.3 | V |
| **Output voltage** | VOUT | -0.3 to VDDS+0.3 | V |
| **Storage temperature** | Tstg | -40 to +125 | °C |

## 5.2. Operating Condition

VSS = 0 V reference
VDD18 used for VDDS as well as VDD-DP18; VDD12 used for VDDC as well as VDD-DSI12.

**Table 5.2 Operating Condition**

| Parameter | Symbol | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|
| **Supply voltage (1.8 V)** | VDD18 | 1.71 | 1.8 | 1.89 | V |
| **Supply voltage (1.2 V)** | VDD12 | 1.14 | 1.2 | 1.26 | V |
| **Operating frequency (internal)** | Fopr | — | — | 200 | MHz |
| **Operating temperature** | Ta | -20 | — | +85 | °C |

## 5.3. DC Electrical Specification

VSS = VSS_C = VSS_IO = VSS_DSI = VSS_DP = VSS_PLL = VSS_REG = 0V reference

**Table 5.3 DC Electrical Specification**

| Parameter | Symbol | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|
| **Input voltage High level CMOS input** Note1 | VIH | 0.7 VDDS | — | VDDS | V |
| **Input voltage Low level CMOS input** Note1 | VIL | 0 | — | 0.3 VDDS | V |
| **Input voltage High level CMOS Schmitt Trigger** Note1 | VIHS | 0.7 VDDS | — | VDDS | V |
| **Input voltage Low level CMOS Schmitt Trigger** Note1 | VILS | 0 | — | 0.3 VDDS | V |
| **Output voltage High level** Note1, Note2 | VOH | 0.8 VDDS | — | VDDS | V |
| **Output voltage Low level** Note1, Note2 | VOL | 0 | — | 0.2 VDDS | V |
| **Input leak current High level** | IIH1 (Note3) | -10 | — | 10 | μA |
| **Input leak current Low level** | IIL1 (Note4) | -10 | — | 10 | μA |
| | IIL2 (Note5) | -200 | — | -10 | μA |

Note1: VDDS within operating condition.

Note2: Output current value is according to each IO buffer specification. Output voltage changes with output current value.

Note3: Normal pin, or Pull-up I/O pin applied VDD18_IO supply voltage to input pin

Note4: Normal pin applied VSS (0 V) to input pin

Note5: Pull-up I/O pin applied VSS (0 V) to input pin

## 5.4. Power Consumption (Typical value based on estimation)

Typical power consumption as measured for the power-down modes and for normal operation are provided below:

- Power-down mode (DSI-Rx in ULPS, DP PHY & PLLs disabled, clocks stopped):
  - ✧ DSI Rx: 0.01 mW
  - ✧ DP PHY: 2.34 mW
  - ✧ PLL9: 0.01 mW
  - ✧ Core: 0.96 mW
  - ✧ Rest: 0.01 mW

- Normal operation (1920×1080 resolution with DSI-Rx in 4-lane @925 Mbps per lane, DP PHY in dual lane link @2.7 Gbps per lane):
  - ✧ DSI Rx: 21.79 mW
  - ✧ DP PHY: 142.70 mW
  - ✧ PLL9: 2.42 mW
  - ✧ Core: 87.64 mW
  - ✧ IOs: 1.68 mW

# 6. Revision History

**Table 6.1 Revision History**

| Revision | Date | Description |
|---|---|---|
| 0.97 | 2014-04-10 | Newly released |
| 0.972 | 2016-04-01 | Modified the weight of TC358767AXBG's package by rounding up digits after the decimal point to form an integer. |
| 1.30 | 2017-07-10 | Changed header, footer and the last page.<br>Added Figure 1.3 and modified descriptions in section 1.<br>Modified descriptions in Features and section 2.<br>Modified Table 3.1 and Figure 3.1.<br>Added Table numbers in section 5. |
| 1.31 | 2017-12-27 | Modified Figure 1.1, Figure 1.2, Figure 1.3.<br>Changed frequency to 100MHz in Figure 1.3.<br>Added description, trademarks and registered trademarks. |
| 1.4 | 2018-05-28 | Modified Figure 1.1, Figure 1.2 and Figure 1.3.<br>Modified Table 2.2 and Table 2.3.<br>Modified Table 3.1.<br>Deleted Table 3.2. (Table 3.2 is the same as Table 4.1.)<br>Modified description in 5.4. |
| 1.5 | 2018-07-09 | Added description to power consumption.<br>Modified Table 3.1. |
| 1.62 | 2019-02-19 | Modified descriptions of trademark and service mark, and marks.<br>Corrected typos.<br>Modified "Note1" in section 5.3.<br>Corrected weight of TC358767AXBG in cover page and chapter 4.<br>Revised the last page "RESTRICTIONS ON PRODUCT USE" and added URL. |

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