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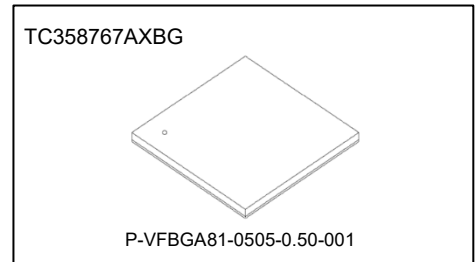
TC358767AXBG/TC358867XBG/TC9595XBG

Mobile Peripheral Devices

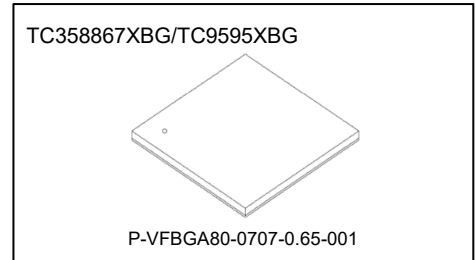
Overview

TC358767AXBG/TC358867XBG/TC9595XBG is a bridge device that enables video streaming from a Host (application or baseband processor) over MIPI® DSI® or DPISM link to drive DisplayPort™ display panels. TC358767AXBG/TC358867XBG/TC9595XBG also supports audio streaming from the host via I²S interface to the Display panels. TC358767AXBG/TC358867XBG/TC9595XBG provides a low power bridge solution to efficiently translate MIPI DSI or DPI transfers to DisplayPort transfers. As the DisplayPort uses fewer wires compared to other existing display panels standards, it simplifies the LCD connectivity.

The effect of using TC358767AXBG/TC358867XBG/TC9595XBG is to enable existing baseband devices supporting DSI or DPI streaming to connect to new panels supporting DisplayPort interface and also to connect to existing panels over longer distance using DisplayPort adaptors at far-end.



Weight: 45 mg (typ.)



Weight: 76 mg (typ.)

Features

- Translates MIPI DSI/DPI Link video stream from Host to DisplayPort Link data to external display devices.
- The inputs are driven by a DSI Host with 4-Data Lanes, up to 1 Gbps/lane or DPI Host with 16/18/24 bit interface up to 154 MHz parallel clock.
- Embeds audio information from the I²S port into the DisplayPort data stream.
- The output interface consists of a DisplayPort Tx with a 2-lane Main Link and AUX-Ch.
- Register Configuration: From DSI link or I²C interface.
- Interrupt to host to inform any error status or status needing attention from Host.
- Internal test pattern (color bar) generator for DP output testing without any video (DSI/DPI) input.
- **DSI Receiver**
 - MIPI DS/MIPI D-PHYSM Compliant.
 - Up to 4 Data Lanes with Bi-direction support on Data Lane 0.
 - Maximum speed at 1 Gbps/lane.
 - Supports Burst as well as Non-Burst Mode video data.
 - Video data packets are limited to one row per HSYNC period.
 - Supports video stream packets for video data transmission.
 - Supports generic long packets for accessing the chip's register set.
- Video input data formats:
 - RGB-565, RGB-666 and RGB-888.
 - DSI Data Type Support: 16-bit YCbCr 422.
- Interlaced video mode is not supported.
- **DPI Receiver**
 - Up to 16/18/24 bit parallel data interface.
 - Maximum speed at 154 MP/s (Mpixel per sec).
 - Video input data formats: RGB-565, RGB-666 and RGB-888.
 - Only Progressive mode supported.
- **I²S Audio Interface:** Supports one I²S port for audio streaming from the host to TC358767AXBG/TC358867XBG/TC9595XBG.
 - Supports target mode (BCLK, LRCLK & OSCLK input from Host).
 - Supports sampling frequencies of 32, 44.1, 48, 88.2, 96, 176.4 & 192 kHz.
 - Supports up to 2 audio channels.
 - Supports 16, 18, 20 or 24 bits per sample.
 - Optionally inserts IEC60958 status bits and preamble bits per channel.

- **DisplayPort Interface:** Supports a DisplayPort link from TC358767AXBG/TC358867XBG/TC9595XBG to display panels.
 - High speed serial bridge chip using VESA® DisplayPort Standard.
 - Supports one dual-lane DisplayPort port for high bandwidth applications.
 - Supports 1.62 or 2.7 Gbps/lane data rate with voltage swings @0.4, 0.6, 0.8 or 1.2 V.
 - Supports of pre-emphasis levels of 0, 3.5 dB and 6 dB.
 - Supports Audio related Secondary Data Packets.
 - AUX channel supported at 1 Mbps.
 - HPD support through GPIO based interrupts.
 - Enhanced mode supported for content protection.
 - Secure ASSR (Alternate Scrambler Seed Reset) support.
 - Stream Policy Maker is assumed handled by the Host (software/firmware).
 - Start Link training in response to HPD & read final Link training status.
 - Configure DP link for actual video streaming & start video streaming.
 - Link Policy maker is assumed shared between the Host and TC358767AXBG/TC358867XBG/TC9595XBG chip.
 - In auto_correction = 0 mode, control link training.
 - Initiate Display device capabilities read and configure TC358767AXBG/TC358867XBG/TC9595XBG accordingly.
 - Video timing generation as per panel requirement.
 - SSCG with to 30 kHz modulation to reduce EMI.
 - Built in PRBS7 Generator to test DisplayPort Link.
- **RGB Parallel Output Interface:**
 - RGB888 output (DisplayPort disabled) with only DSI input supported in this mode.
 - PCLK max = 100 MHz.
 - Polarity control for PCLK, VSYNC, HSYNC & DE.
- **I²C Interface:**
 - I²C target interface for chip register set.
 - I²C compliant target interface support for normal (100 kHz) and fast mode (400 kHz).
- **GPIO Interface:**
 - 2 bits of GPIO (shared with other digital logic).
 - Direction controllable by Host I²C accesses.
- **Clock Source:**
 - DisplayPort clock source is from an external clock input (13, 26, 19.2 or 38.4 MHz) or clock from DSI interface – generates all internal & output clocks to interfacing display devices.
 - Built-in PLLs generate high-speed DisplayPort link clock requiring no external components. These PLLs are part of the DisplayPort PHY.
- Clock and power management support to achieve low power states.
- **Possible modes of Operation:**
 - **MODE S21:**
TC358767AXBG/TC358867XBG/TC9595XBG uses DisplayPort Tx as single 2-lane DisplayPort link to interface to single DisplayPort display device. Video stream source is from MIPI DSI Host.
 - **MODE P21:**
TC358767AXBG/TC358867XBG/TC9595XBG uses DisplayPort Tx as single 2-lane DisplayPort link to interface to single DisplayPort display device. Video stream source is from MIPI DPI Host.
 - **MODE S2P:**
TC358767AXBG/TC358867XBG/TC9595XBG uses only Parallel output port and disables DisplayPort Tx to interface to single RGB display device. Video stream source is from MIPI DSI Host.
- **Power supply inputs**
 - Core and MIPI D-PHY: 1.2 V
 - Digital I/O: 1.8 V
 - DisplayPort: 1.8 V
 - DisplayPort: 1.2 V
- **Power Consumptions (Typical value based on estimations)**
 - Power-down mode (DSI-Rx in ULPS, DP PHY & PLLs disabled, clocks stopped):
 - DSI Rx: 0.1 mW
 - DP PHY: 2.3 mW
 - PLL9: 0.1 mW
 - Core: 1.0 mW
 - Rest: 0.1 mW
 - Normal operation (1920 × 1080 resolution with DSI-Rx in 4-lane @925 Mbps per lane, DP PHY in dual lane link @2.7 Gbps per lane):
 - DSI Rx: 21.8 mW
 - DP PHY: 142.7 mW
 - PLL9: 2.4 mW
 - Core: 87.6 mW
 - IOs: 1.7 mW

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2. MIPI DPI, “MIPI Alliance Standard for Display Pixel Interface (DPI-2) Version 2.00 – 15 September 2005”
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5. VESA embedded DisplayPort (eDP) Standard (Version 1.1 October 23, 2009)
6. I²C bus specification, version 2.1, January 2000, Philips Semiconductor
7. Draft CEA-861-C, A DTV Profile for Uncompressed High Speed Digital Interfaces (Doc. Number: CEA-861rCv9.pdf (PNXXX)) Date: 05/04/2005
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1. Overview

The DSI/DPI to DisplayPort converter (TC358767AXBG/TC358867XBG/TC9595XBG) is a bridge device that enables video streaming from a Host (application or baseband processor) over MIPI DSI or DPI link to drive DisplayPort display panels. TC358767AXBG/TC358867XBG/TC9595XBG also supports audio streaming from the host via I²S interface to the Display panels. TC358767AXBG/TC358867XBG/TC9595XBG provides a low power bridge solution to efficiently translate MIPI DSI or DPI transfers to DisplayPort transfers. As the DisplayPort uses fewer wires compared to other existing display panel standards, it simplifies the LCD connectivity. The effect of using TC358767AXBG/TC358867XBG/TC9595XBG is to enable existing baseband devices supporting DSI or DPI streaming to connect to new panels supporting DisplayPort interface and also to connect to existing panels over longer distance using DisplayPort adaptors at far-end.

The chip can be configured through the DSI link by sending write/read register commands through DSI Generic Long Write packets. It can also be configured through the I²C Target interface.

The DSI-RX receiver supports from 1 to 4-Lane configurations at bit rate up to 1 Gbps per lane. Host can transmit video in continuous video streaming mode. Host controls video timing by sending video frame and line sync events together with video pixel data; video data transmission can be burst or non-burst. Since the chip integrates only a small video buffer, Host still has to take care of transmitting pixel data at appropriate video line time in order to avoid buffer overflow (or underflow).

The DPI-Rx receiver supports 16, 18 or 24 bits parallel interface along with the required control signals for the Pixel clock and HSYNC/VSYNC/DE.

The DisplayPort transmitter supports data throughput at 1.62 Gbps or 2.7 Gbps per lane of main link.

TC358767AXBG/TC358867XBG/TC9595XBG supports three configuration modes. These modes mainly differ based on the source of input stream and output interface.

- Mode_S21: A system configuration where TC358767AXBG/TC358867XBG/TC9595XBG may typically be used is shown in Figure 1.1. In this configuration, the TC358767AXBG/TC358867XBG/TC9595XBG can support displays with resolution up to WUXGA (1920 × 1200) at 24 bit, 60 fps or WUXGA (1920 × 1200) at 18 bit, 60 fps. Video stream source is from DSI Host.
- Mode_P21: A system configuration where TC358767AXBG/TC358867XBG/TC9595XBG may typically be used is shown in Figure 1.2. This is similar to the Mode_S21 except that the video stream source is from DPI Host. In this configuration, the TC358767AXBG/TC358867XBG/TC9595XBG can support displays with resolution up to WUXGA (1920 × 1200) at 24 bit, 60 fps.
- Mode_S2P: A system configuration where TC358767AXBG/TC358867XBG/TC9595XBG may typically be used is shown in Figure 1.3. In this mode, DisplayPort output is not used and the chip rather behaves as a DSI to RGB convertor. In this system, TC358767AXBG/TC358867XBG/TC9595XBG could be connected to a single display. In this configuration, the TC358767AXBG/TC358867XBG/TC9595XBG can support displays with resolution up to WXGA (1280x800 or 1366x768). Maximum output PCLK is 100 MHz. Video stream source is from DSI Host.

The chip supports power management to conserve power when its functions are not in use. Host manages the chip's power consumption modes by using ULPS messages over DSI link during DPI input mode.

The following figures show all these modes, where TC358767AXBG/TC358867XBG/TC9595XBG, display panels and a Host are connected in target Reference system for mobile large display panel applications.

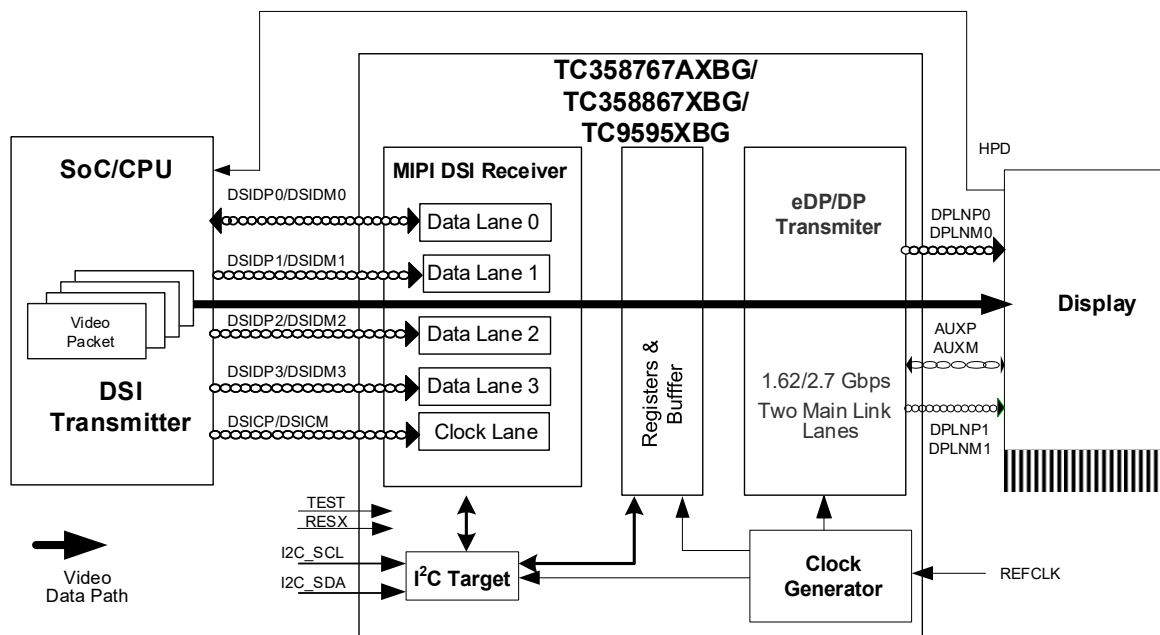


Figure 1.1 System Overview with TC358767AXBG/TC358867XBG/TC9595XBG in MODE_S21 Configuration

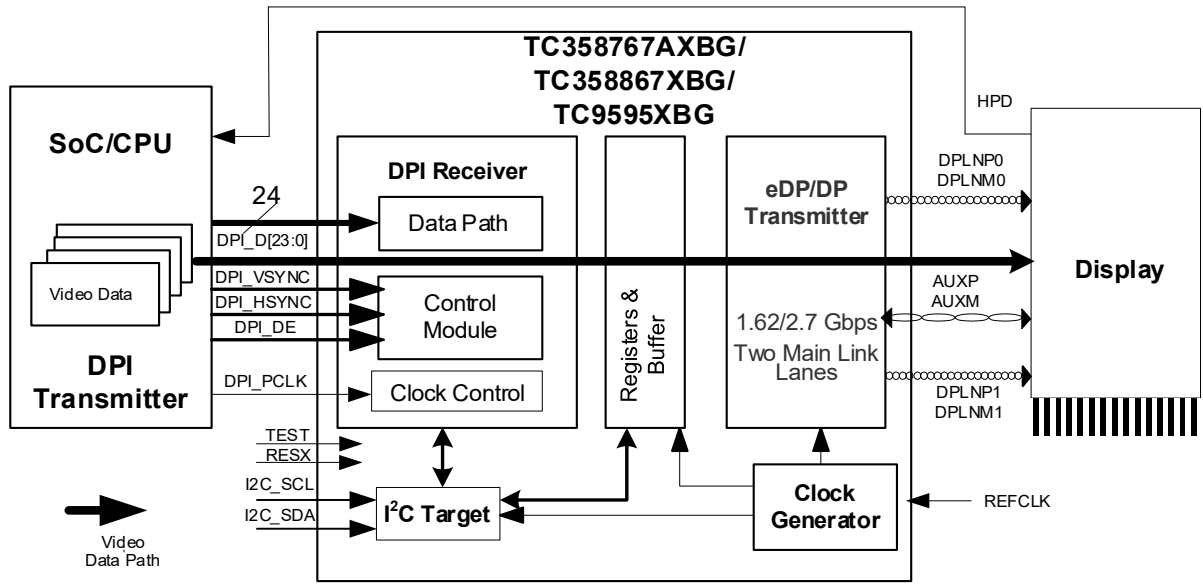


Figure 1.2 System Overview with TC358767AXBG/TC358867XBG/TC9595XBG in MODE_P21 Configuration

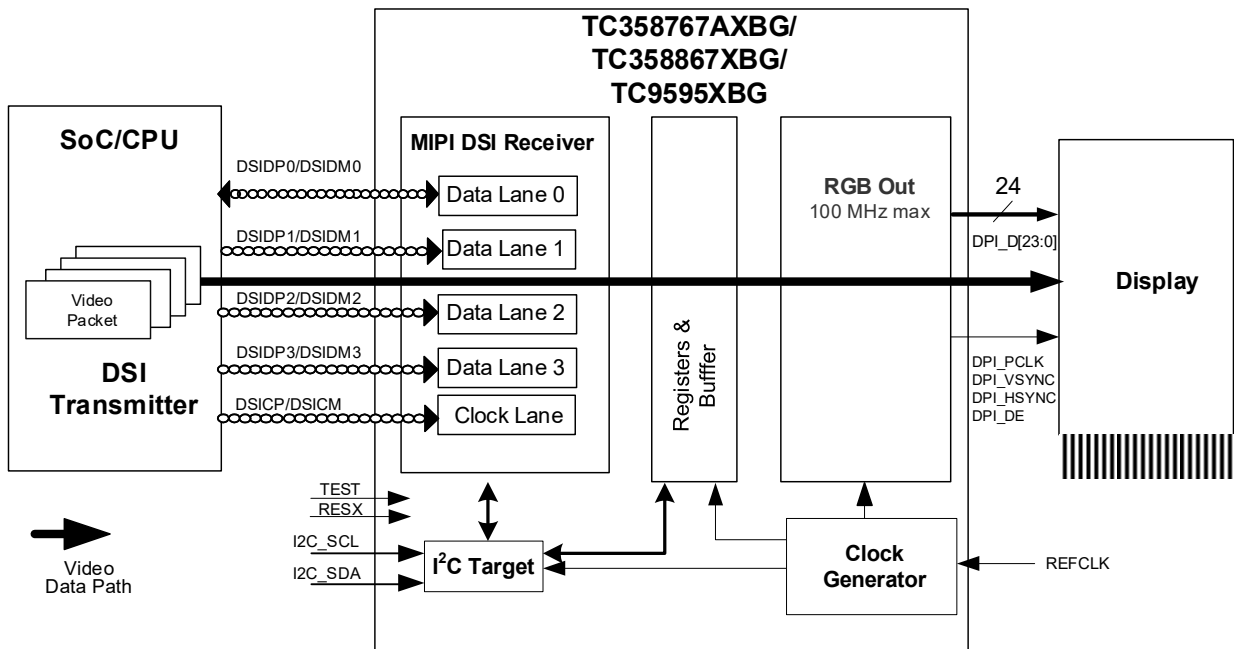


Figure 1.3 System Overview with TC358767AXBG/TC358867XBG/TC9595XBG in MODE_S2P Configuration

2. Features

Below are the main features supported by TC358767AXBG/TC358867XBG/TC9595XBG.

- Translates MIPI DSI/DPI Link video stream from Host to DisplayPort Link data to external display devices.
- The inputs are driven by a DSI Host with 4-Data Lanes, up to 1 Gbps/lane or DPI Host with 16/18/24 bit interface up to 154 MHz parallel clock.
- Embeds audio information from the I²S port into the DisplayPort data stream.
- The output Interface consists of a DisplayPort Tx with a 2-lane Main Link and AUX-Ch.
- Register Configuration: From DSI link or I²C interface.
- Interrupt to host to inform any error status or status needing attention from Host.
- Internal test pattern (color bar) generator for DP output testing without any video (DSI/DPI) input.

• DSI Receiver

- MIPI DSI/MIPI D-PHY Compliant.
- Up to 4 Data Lanes with Bi-direction support on Data Lane 0.
- Maximum speed at 1 Gbps/lane.
- Supports Burst as well as Non-Burst Mode video data.
Video data packets are limited to one row per HSYNC period.
- Supports video stream packets for video data transmission.
- Supports generic long packets for accessing the chip's register set.
- Video input data formats:
RGB-565, RGB-666 and RGB-888.
DSI Data Type Support: 16-bit YCbCr 422.
- Interlaced video mode is not supported.

• DPI Receiver

- Up to 16/18/24 bit parallel data interface.
- Maximum speed at 154 MPs (MPixel per sec).
- Video input data formats: RGB-565, RGB-666 and RGB-888.
- Only Progressive mode supported.

• I²S Audio Interface: Supports one I²S port for audio streaming from the host to TC358767AXBG/TC358867XBG/TC9595XBG.

- Supports target mode (BCLK, LRCLK & OSCLK input from Host).
- Supports sampling frequencies of 32, 44.1, 48, 88.2, 96, 176.4 & 192 kHz.
- Supports up to 2 audio channels.
- Supports 16, 18, 20 or 24 bits per sample.
- Optionally inserts IEC60958 status bits and preamble bits per channel.

• DisplayPort Interface: Supports a DisplayPort link from TC358767AXBG/TC358867XBG/TC9595XBG to display panels.

- High speed serial bridge chip using VESA DisplayPort Standard.
- Supports one dual-lane DisplayPort port for high bandwidth applications.
- Supports 1.62 or 2.7 Gbps/lane data rate with voltage swings @0.4, 0.6, 0.8 or 1.2 V.
- Supports of pre-emphasis levels of 0, 3.5 dB and 6 dB.
- Supports Audio related Secondary Data Packets.
- AUX channel supported at 1 Mbps.
- HPD support through GPIO based interrupts.
- Enhanced mode supported for content protection.
- Secure ASSR (Alternate Scrambler Seed Reset) support for embedded DisplayPort panels.
- Stream Policy Maker is assumed handled by the Host (software/firmware).
Start Link training in response to HPD & read final Link training status.
Configure DP link for actual video streaming & start video streaming.
- Link Policy maker is assumed shared between the Host and TC358767AXBG/TC358867XBG/TC9595XBG chip.
In auto_correction = 0 mode, control link training.
Initiate Display device capabilities read and configure TC358767AXBG/TC358867XBG/TC9595XBG accordingly.

- Video timing generation as per panel requirement.
- SSCG with to 30 kHz modulation to reduce EMI.
- Built in PRBS7 Generator to test DisplayPort Link.
- **RGB Parallel Output Interface:**
 - RGB888 output (DisplayPort disabled) with only DSI input supported in this mode.
 - PCLK max = 100 MHz.
 - Polarity control for PCLK, VSYNC, HSYNC & DE.
- **I²C Interface:**
 - I²C target interface for chip register set.
 - I²C compliant target interface support for normal (100 kHz) and fast mode (400 kHz).
- **GPIO Interface:**
 - 2 bits of GPIO (shared with other digital logic).
 - Direction controllable by Host I²C accesses.
- **Clock Source:**
 - DisplayPort clock source is from an external clock input (13, 26, 19.2 or 38.4 MHz) or clock from DSI interface – generates all internal & output clocks to interfacing display devices.
 - Built-in PLLs generate high-speed DisplayPort link clock requiring no external components. These PLLs are part of the DisplayPort PHY.
- Clock and power management support to achieve low power states.
- **Possible modes of Operation:**
 - MODE S21: TC358767AXBG/TC358867XBG/TC9595XBG uses DisplayPort Tx as single 2-lane DisplayPort link to interface to single DisplayPort display device. Video stream source is from MIPI DSI Host.
 - MODE P21: TC358767AXBG/TC358867XBG/TC9595XBG uses DisplayPort Tx as single 2-lane DisplayPort link to interface to single DisplayPort display device. Video stream source is from MIPI DPI Host.
 - MODE S2P: TC358767AXBG/TC358867XBG/TC9595XBG uses only Parallel output port and disables DisplayPort Tx to interface to single RGB display device. Video stream source is from MIPI DSI Host.
- **Power supply inputs**
 - Core and MIPI D-PHY: 1.2 V
 - Digital I/O: 1.8 V
 - DisplayPort: 1.8 V
 - DisplayPort: 1.2 V
- **Power Consumptions (Typical value based on estimations)**
 - Power-down mode (DSI-Rx in ULPS, DP PHY & PLLs disabled, clocks stopped):
 - DSI Rx: 0.1 mW
 - DP PHY: 2.3 mW
 - PLL9: 0.1 mW
 - Core: 1.0 mW
 - Rest: 0.1 mW
 - Normal operation (1920 × 1080 resolution with DSI-Rx in 4-lane @925 Mbps per lane, DP PHY in dual lane link @2.7 Gbps per lane):
 - DSI Rx: 21.8 mW
 - DP PHY: 142.7 mW
 - PLL9: 2.4 mW
 - Core: 87.6 mW
 - IOs: 1.7 mW

Note: Attention about ESD. This product is weak against ESD. Please handle it carefully.

Table 2.1 TC358767AXBG/TC358867XBG/TC9595XBG operational modes summary with panel size support information

Mode	Input Configuration		Register Access Method	Max Panel size example
	DSI input	DPI input		
S21	Active	X	DSI or I ² C	WUXGA 18 bpp @ 60 fps WUXGA 24 bpp @ 60 fps
P21	X	Active	I ² C	WUXGA 24 bpp @ 60 fps

Tables below provide an idea of different panel sizes that can be supported by using different data link lane configurations.

Table 2.2 Panel Size v/s Data link required by TC358767AXBG/TC358867XBG/TC9595XBG in DSI input case

Frame Size			FPS	Pixel Clock (MHz)	RGB666				RGB888			
		With OverHead			Bit Rate (Gbps)	# DSI Data lanes	# DP Main links		Bit Rate (Gbps)	# DSI Data lanes	# DP Main links	
							1.62 G	2.7 G			1.62 G	2.7 G
XGA	1024 × 768	1184 × 790	60	56	1.01	2	1	1	1.34	2	2	1
WXGA+ /WSXGA	1440 × 900	1600 × 926	60	89	1.60	2	2	1	2.13	3	2	1
SXGA+	1400 × 1050	1560 × 1080	60	89	1.82	2	2	1	2.43	3	2	2
WSXGA+	1680 × 1050	1840 × 1080	60	119	2.15	3	2	1	2.86	3	—	2
UXGA	1600 × 1200	1760 × 1235	60	130	2.35	3	2	2	3.13	4	—	2
WUXGA	1920 × 1200	2080 × 1235	60	154	2.77	3	—	2	3.70	4	—	2

Table 2.3 Panel Size v/s Data link required by TC358767AXBG/TC358867XBG/TC9595XBG in DPI input case

Frame Size			FPS	Pixel Clock (MHz)	DPI Support 154 MHz PCLK	RGB666			RGB888		
		With OverHead				Bit Rate (Gbps)	# DP Main links		Bit Rate (Gbps)	# DP Main links	
							1.62 G	2.7 G		1.62 G	2.7 G
XGA	1024 × 768	1184 × 790	60	56	Yes	1.01	1	1	1.34	2	1
WXGA+ /WSXGA	1440 × 900	1600 × 926	60	89	Yes	1.60	2	1	2.13	2	1
SXGA+	1400 × 1050	1560 × 1080	60	89	Yes	1.82	2	1	2.43	2	2
WSXGA+	1680 × 1050	1840 × 1080	60	119	Yes	2.15	2	1	2.86	—	2
UXGA	1600 × 1200	1760 × 1235	60	130	Yes	2.35	2	2	3.13	—	2
WUXGA	1920 × 1200	2080 × 1235	60	154	Yes	2.77	—	2	3.70	—	2

Note: These are the formats commonly used by displays. Support for other sizes is possible as long as they satisfy the maximum data rate constraints on the DSI and DisplayPort link interfaces.

Note: Throughout the rest of the document, “DP” is used to denote “DisplayPort”. Both these words have been used interchangeably and refer to the VESA DisplayPort specification as mentioned in the references.

3. External Pins

3.1. TC358767AXBG External Pins

3.1.1. TC358767AXBG Pin List

TC358767AXBG uses an 81 pin package. Following table gives the signals of TC358767AXBG and their function.

Table 3.1 TC358767AXBG Functional Signal List for 81-pin Package

Group	Pin Name	I/O	Type	Function	Note
System: Reset, Clock, Mode select, Test (9)	RESX	I	Sch	System Reset – active Low 0: Reset 1: Normal operation	—
	REFCLK	I	Sch	13, 26, 19.2 or 38.4 MHz 50 ps phase jitter(max.), duty cycle 40 to 60%	—
	INT	O	N	Interrupt to Host – active High 0: No interrupt is generated 1: Interrupt is generated	4 mA
	DISABLE_ASSR	I	N	ASSR control 0: Enable ASSR 1: Disable ASSR	—
	MODE[1:0]	I	N	Mode Selection pins MODE_0: 0: REFCLK is source of internal DP PLL 1: When REFCLK = “0”, DSI clock is source of internal DP PLL. When REFCLK = “1”, DPI PCLK is source of internal DP PLL. MODE_1: When MODE_0 = “1” & REFCLK = “0” this pin will be effective. 0: DSI clock/2/7 is source of internal DP PLL. 1: DSI clock/2/9 is source of internal DP PLL.	—
	TEST	I	N	Test Pin, Connect to GND	—
	TEST3	O	N	Test Pin, Open	—
	VPGM0	NA	—	Test Pin, Connect to GND	—
DSI Rx (10)	DSICP	I	MIPI®-PHY	MIPI®-DSI Rx Clock Lane Pos.	—
	DSICM	I	MIPI®-PHY	MIPI®-DSI Rx Clock Lane Neg.	—
	DSIDP0	I/O	MIPI®-PHY	MIPI®-DSI Rx Data Lane Pos.	—
	DSIDM0	I/O	MIPI®-PHY	MIPI®-DSI Rx Data Lane Neg.	—
	DSIDP[3:1]	I	MIPI®-PHY	MIPI®-DSI Rx Data Lane Pos.	—
	DSIDM[3:1]	I	MIPI®-PHY	MIPI®-DSI Rx Data Lane Neg.	—
DP Out (8)	DPLNP[1:0]	O	DP-PHY	DisplayPort Output Main Link Pos.	—
	DPLNM[1:0]	O	DP-PHY	DisplayPort Output Main Link Neg.	—
	DPAUXP	I/O	DP-PHY	DisplayPort Output AUX Channel Pos.	—
	DPAUXM	I/O	DP-PHY	DisplayPort Output AUX Channel Neg.	—
	PREC_RES[1:0]	I	DP-PHY	Precision Resistance (3 kΩ @ 1%) connection	—
DPI Tx/Rx (28)	DPI_PCLK	I/O	N	DPI Pixel Clock (default: Input)	4 mA
	DPI_VSYNC	I/O	N	DPI Vertical Sync (default: Input)	4 mA
	DPI_HSYNC	I/O	N	DPI Horizontal Sync (default: Input)	4 mA
	DPI_DE	I/O	N	DPI Data Enable (default: Input)	4 mA
	DPI_D[23:0]	I/O	N	DPI Parallel Data (default: Input)	4 mA
I ² C (3)	I2C_SCL	OD	Sch	I ² C Clock	—
	I2C_SDA	OD	Sch	I ² C Data	4 mA
	I2C_ADR_SEL	I	N	I ² C Target Address Select 0: Target address = 7'b1101_000 1: Target address = 7'b0001_111	—

Group	Pin Name	I/O	Type	Function	Note
I ² S (4)	SD/I2S_OSCLK	I	N	I ² S Over Sampling Clock	—
	I2S_BCLK	I	N	I ² S Bit Clock (max 12.5 MHz)	—
	I2S_LRCLK	I	N	I ² S sample clock (max 192 kHz)	—
	I2S_DATA	I	N	I ² S Data	—
GPIO (2)	GPIO[1:0]	OD	5T-OD	GPIO or Test Control (Note 1) GPIO[1:0] can be used for HPD support	4 mA
POWER (10)	VDDC (1.2 V)	NA	—	VDD for Internal Core (2)	—
	VDDS (1.8 V)	NA	—	VDDS for IO Ring power supply (1)	—
	VDD_PLL18 (1.8 V)	NA	—	VDD for DP PHY PLLs (1)	—
	VDD_PLL12 (1.2 V)	NA	—	VDD for DP PHY PLLs (1)	—
	VDD_DP18 (1.8 V)	NA	—	VDD for DP PHY Main Channels (2)	—
	VDD_PLL912 (1.2 V)	NA	—	VDD for PLL9 (1)	—
	VDD_DP12 (1.2 V)	NA	—	VDD for DP PHY (1)	—
	VDD_DSI12 (1.2 V)	NA	—	VDD for the MIPI [®] DSI PHY (1)	—
GROUND (7)	VSS	NA	—	Ground (Core, I/O) (3)	—
	VSS_DSI	NA	—	Ground (DSI) (1)	—
	VSS_DP	NA	—	Ground (DP) (3)	—

Note 1: Pins with multiplexed Functional mode functions

- N: Normal IO
- FS: Fail safe IO - gated
- PHY: Either DP analog front end or MIPI[®] D-PHY
- Sch: Schmitt trigger input
- OD: Open drain
- 5T-OD: 5 V tolerant bi-direction buffer with Open drain
- Pd: Pull Down

3.1.2. TC358767AXBG Pin Mapping

The mapping of TC358767AXBG signals to the external pins is given in the following figure. (BGA array)

Top View (through the die)

A1	A2	A3	A4	A5	A6	A7	A8	A9
DSIDM_0	DSIDP_0	I2S_LRCLK	VDDC	VDDC	INT	VDDS	I2C_SDA	I2C_SCL
B1	B2	B3	B4	B5	B6	B7	B8	B9
DSIDM_1	DSIDP_1	GPIO_0	I2S_BCLK	I2S_DATA	MODE_0	MODE_1	GPIO_1	I2C_ADR_SEL
C1	C2	C3	C4	C5	C6	C7	C8	C9
DSICM	DSICP	DPI_DE	DPI_VSYNC	DPI_D_5	DPI_D_7	DPI_D_10	TEST_3	I2S_OSCLK
D1	D2	D3	D4	D5	D6	D7	D8	D9
VDD_DSI12	VSS_DSI	DPI_HSYNC	DPI_D_0	VSS	DPI_D_9	DPI_D_12	DPI_D_13	DPI_D_14
E1	E2	E3	E4	E5	E6	E7	E8	E9
DSIDM_2	DSIDP_2	DPI_D_1	DPI_D_3	VSS	VSS	DPI_D_16	VPGM_0	DPI_D_11
F1	F2	F3	F4	F5	F6	F7	F8	F9
DSIDM_3	DSIDP_3	DPI_D_2	DPI_D_6	DPI_D_8	DPI_D_15	DPI_D_18	DPI_D_17	DPI_D_20
G1	G2	G3	G4	G5	G6	G7	G8	G9
PREC_RES_0	Disable_ASSR	DPI_D_4	TEST	DPI_D_19	DPI_PCLK	DPI_D_21	DPI_D_23	DPI_D_22
H1	H2	H3	H4	H5	H6	H7	H8	H9
PREC_RES_1	VSS_DP	DPLNP_0	VDD_DP12	VSS_DP	DPLNP_1	VSS_DP	DPAUXP_0	VDD_PLL912
J1	J2	J3	J4	J5	J6	J7	J8	J9
REFCLK	VDD_DP18	DPLNM_0	VDD_PLL12	VDD_PLL18	DPLNM_1	VDD_DP18	DPAUXM_0	RESX

Figure 3.1 TC358767AXBG 81-Pin Layout

3.2. TC358867XBG/TC9595XBG External Pins

3.2.1. TC358867XBG/TC9595XBG Pin List

TC358867XBG/TC9595XBG uses an 80-ball package. Following table gives the signals of TC358867XBG/TC9595XBG and their function.

Table 3.2 TC358867XBG/TC9595XBG Functional Signal List for 80-ball Package

Group	Pin Name	I/O	Type	Function	Note
System: Reset, Clock, Mode select, Test (9)	RESX	I	Sch	System Reset – active Low 0: Reset 1: Normal operation	—
	REFCLK	I	Sch	13, 26, 19.2 or 38.4 MHz 50 ps phase jitter(max.), duty cycle 40 to 60%	—
	INT	O	N	Interrupt to Host – active High 0: No interrupt is generated 1: Interrupt is generated	4 mA
	DISABLE_ASSR	I	N	ASSR control 0: Enable ASSR 1: Disable ASSR	—
	MODE[1:0]	I	N	Mode Selection pins MODE_0: 0: REFCLK is source of internal DP PLL 1: When REFCLK = “0”, DSI clock is source of internal DP PLL. When REFCLK = “1”, DPI PCLK is source of internal DP PLL. MODE_1: When MODE_0 = “1” & REFCLK = “0” this pin will be effective. 0: DSI clock/2/7 is source of internal DP PLL. 1: DSI clock/2/9 is source of internal DP PLL.	—
	TEST	I	N	Test Pin, Connect to GND	—
	TEST3	O	N	Test Pin, Open	—
	VPGM0	NA	—	Test Pin, Connect to GND	—
DSI Rx (10)	DSICP	I	MIPI-PHY	MIPI-DSI Rx Clock Lane Pos.	—
	DSICM	I	MIPI-PHY	MIPI-DSI Rx Clock Lane Neg.	—
	DSIDP0	I/O	MIPI-PHY	MIPI-DSI Rx Data Lane Pos.	—
	DSIDM0	I/O	MIPI-PHY	MIPI-DSI Rx Data Lane Neg.	—
	DSIDP[3:1]	I	MIPI-PHY	MIPI-DSI Rx Data Lane Pos.	—
	DSIDM[3:1]	I	MIPI-PHY	MIPI-DSI Rx Data Lane Neg.	—
DP Out (8)	DPLNP[1:0]	O	DP-PHY	DisplayPort Output Main Link Pos.	—
	DPLNM[1:0]	O	DP-PHY	DisplayPort Output Main Link Neg.	—
	DPAUXP	I/O	DP-PHY	DisplayPort Output AUX Channel Pos	—
	DPAUXM	I/O	DP-PHY	DisplayPort Output AUX Channel Neg	—
	PREC_RES[1:0]	I	DP-PHY	Precision Resistance (3 kΩ @ 1%) connection	—
DPI Tx/Rx (28)	DPI_PCLK	I/O	N	DPI Pixel Clock (default: Input)	4 mA
	DPI_VSYNC	I/O	N	DPI Vertical Sync (default: Input)	4 mA
	DPI_HSYNC	I/O	N	DPI Horizontal Sync (default: Input)	4 mA
	DPI_DE	I/O	N	DPI Data Enable (default: Input)	4 mA
	DPI_D [23:0]	I/O	N	DPI Parallel Data (default: Input)	4 mA
I ² C (3)	I2C_SCL	OD	Sch	I ² C Clock	—
	I2C_SDA	OD	Sch	I ² C Data	4 mA
	I2C_ADR_SEL	I	N	I ² C Target Address Select 0: Target address = 7'b1101_000 1: Target address = 7'b0001_111	—

Group	Pin Name	I/O	Type	Function	Note
I ² S (4)	SD/I2S_OSCLK	I	N	I ² S Over Sampling Clock	—
	I2S_BCLK	I	N	I ² S Bit Clock (max 12.5 MHz)	—
	I2S_LRCLK	I	N	I ² S sample clock (max 192 kHz)	—
	I2S_DATA	I	N	I ² S Data	—
GPIO (2)	GPIO[1:0]	OD	5T-OD	GPIO or Test Control (Note 1) GPIO[1:0] can be used for HPD support	4 mA
POWER (10)	VDDC (1.2 V)	NA	—	VDD for Internal Core (2)	—
	VDDS (1.8 V)	NA	—	VDDS for IO Ring power supply (1)	—
	VDD_PLL18 (1.8 V)	NA	—	VDD for DP PHY PLLs (1)	—
	VDD_DP18 (1.8 V)	NA	—	VDD for DP PHY Main Channels (2)	—
	VDD_PLL912 (1.2 V)	NA	—	VDD for PLL9 (1)	—
	VDD_DP12 (1.2 V)	NA	—	VDD for DP PHY (2)	—
	VDD_DSI12 (1.2 V)	NA	—	VDD for the MIPI DSI PHY (1)	—
GROUND (6)	VSS	NA	—	Ground (Core, DSI, I/O) (3)	—
	VSS_DP	NA	—	Ground (DP) (3)	—

Note 1: Pins with multiplexed Functional mode functions.

- N: Normal IO
- PHY: Either DP analog front end or MIPI D-PHY
- Sch: Schmitt trigger input
- OD: Open drain
- 5T-OD: 5 V tolerant bi-direction buffer with Open drain

3.2.2. TC358867XBG/TC9595XBG Pin Mapping

The mapping of TC358867XBG/TC9595XBG signals to the external pins is given in the following figure. (BGA array)

Top View

	1	2	3	4	5	6	7	8	9	10
A	INT	GPIO0	DPI_VSYNC	DPI_D0	VDDC	VDDC	DPI_D3	VDDS	I2C_SDA	I2C_SCL
B	DSIDM0	DSIDP0	DPI_DE	DPI_HSYNC	DPI_D1	DPI_D2	DPI_D4	DPI_D7	DPI_D5	DPI_D6
C	DSIDM1	DSIDP1							DPI_D9	DPI_D8
D	DSICM	DSICP		I2S_LRCLK	I2S_BCLK	SD/ I2S_OSCLK	I2S_DATA		DPI_D13	DPI_D14
E	VDD_DS12	I2C_ADR_SEL		VSS	TEST3	VPGM0	DPI_D10		DPI_D16	DPI_D15
F	DSIDM2	DSIDP2		VSS	VSS	TEST	DPI_D11		DPI_D17	DPI_D18
G	DSIDM3	DSIDP3		VSS_DP	VSS_DP	VSS_DP	DPI_D12		DPI_D19	DPI_PCLK
H	PREC_RES0	DISABLE_ASSR							DPI_D20	DPI_D21
J	PREC_RES1	MODE1	DPLNP0	VDD_DP12	MODE0	DPLNP1	GPIO1	DPAUXP	RESX	DPI_D23
K	REFCLK	VDD_DP18	DPLNM0	VDD_DP12	VDD_PLL18	DPLNM1	VDD_DP18	DPAUXM	VDD_PLL912	DPI_D22

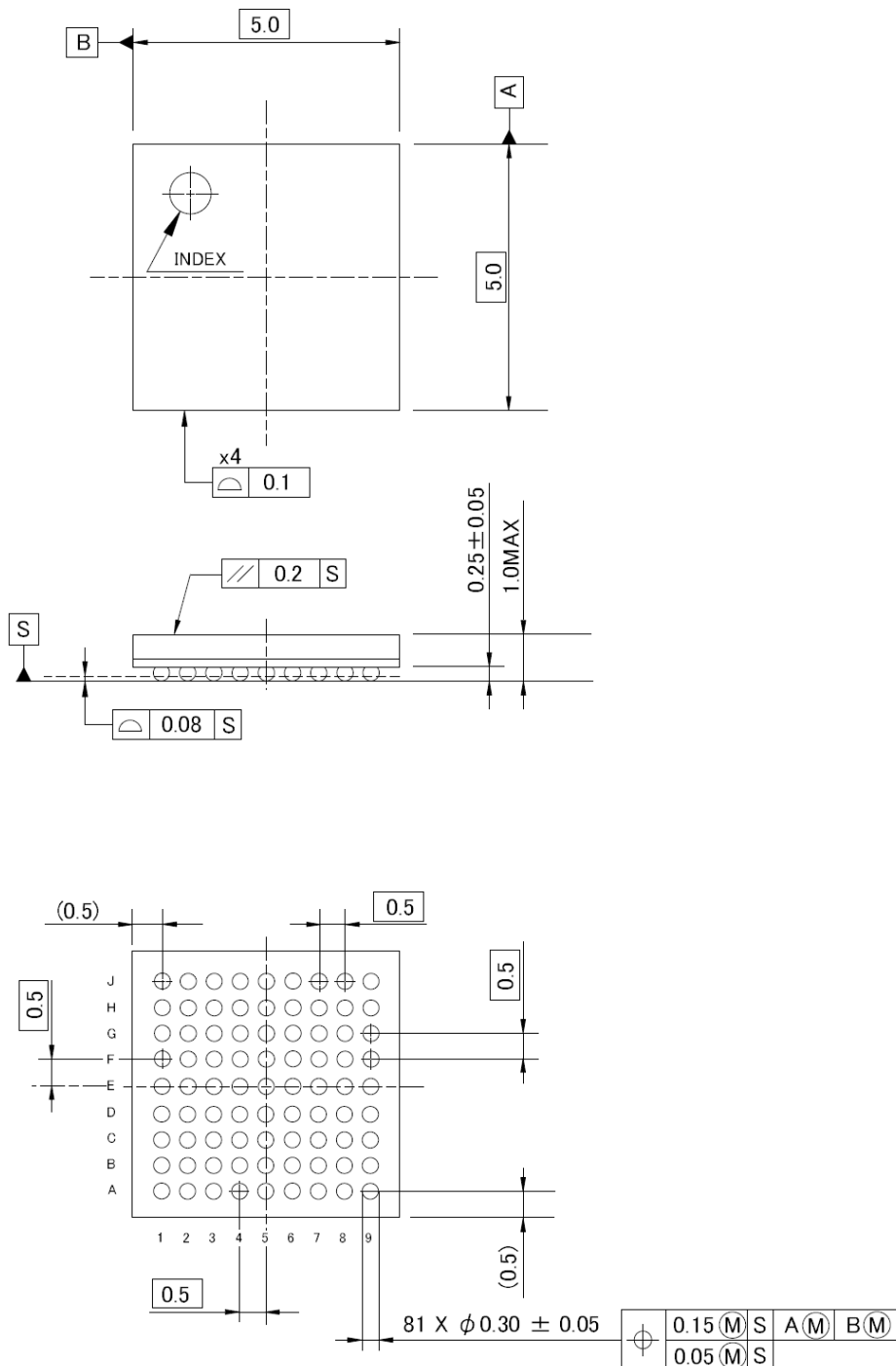
Figure 3.2 TC358867XBG/TC9595XBG 80-ball Layout

4. Package

4.1. TC358767AXBG Package

The package for TC358767AXBG is described in the figure below.

Unit: mm



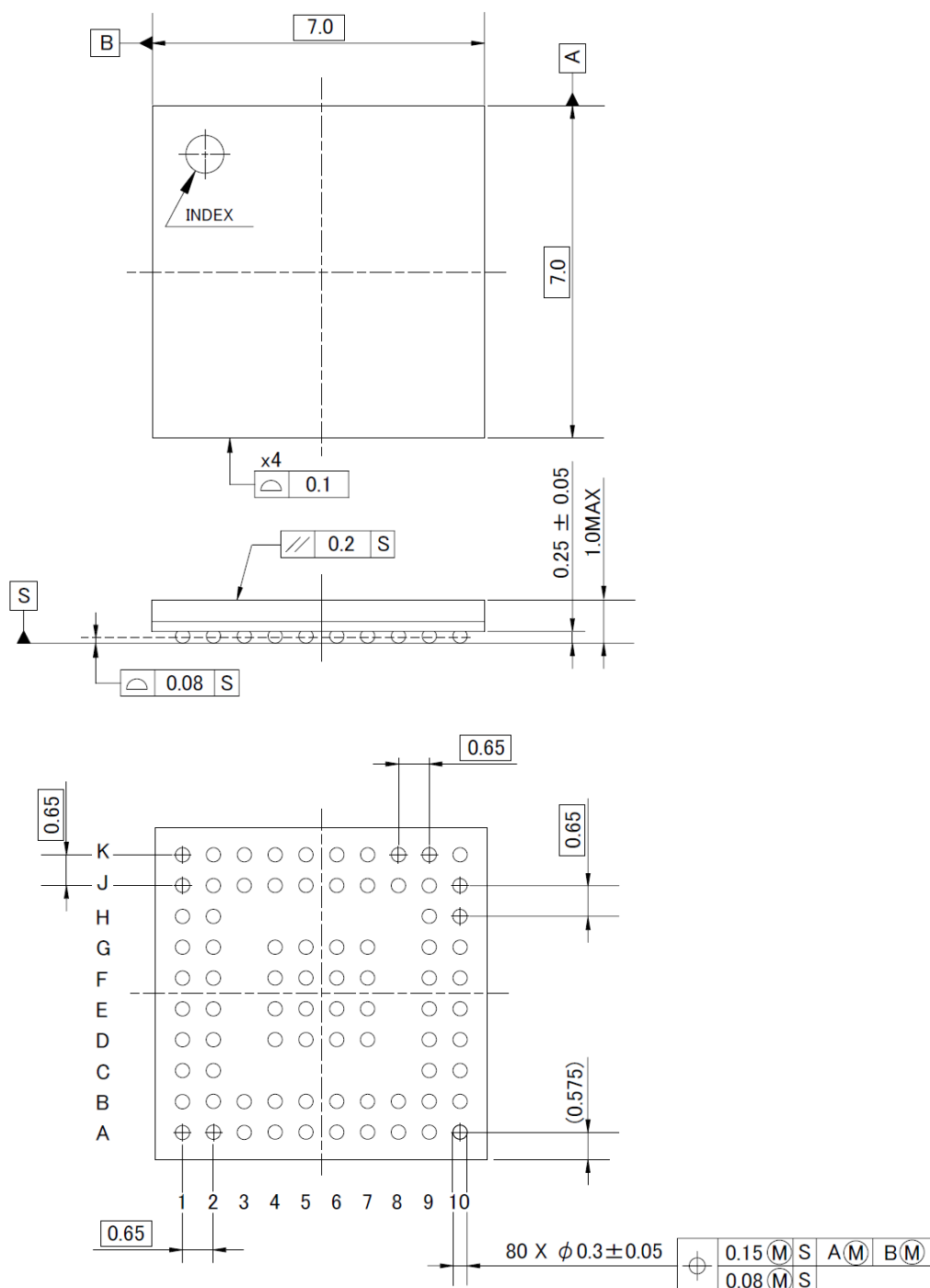
Weight: 45 mg (typ.)

Figure 4.1 TC358767AXBG (P-VFBGA81-0505-0.50-001) package

4.2. TC358867XBG/TC9595XBG Package

The package for TC358867XBG/TC9595XBG is described in the figure below.

Unit: mm



Weight: 76 mg (typ.)

Figure 4.2 TC358867XBG/TC9595XBG (P-VFBGA80-0707-0.65-001) package

5. Electrical Characteristics

5.1. Absolute Maximum Ratings

VSS, VSS_DP and VSS_DSI (TC358767AXBG only) = 0 V reference

VDD18 used for VDDS, VDD_DP18 and VDD_PLL18; VDD12 used for VDDC, VDD_DSI12, VDD_DP12, VDD_PLL912 and VDD_PLL12 (TC358767AXBG only).

Table 5.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage (1.8 V)	VDD18	-0.3 to +3.5	V
Supply voltage (1.2 V)	VDD12	-0.3 to +2.0	V
Supply voltage (IO)	VDD18	-0.3 to +3.5	V
	VREF	-0.3 to +3.5	V
Input voltage	VIN	-0.3 to VDDS + 0.3	V
Output voltage	VOU	-0.3 to VDDS + 0.3	V
Storage temperature	Tstg	-40 to +125	°C

5.2. Operating Condition

VSS, VSS_DP and VSS_DSI (TC358767AXBG only) = 0 V reference

VDD18 used for VDDS, VDD_DP18 and VDD_PLL18; VDD12 used for VDDC, VDD_DSI12, VDD_DP12, VDD_PLL912 and VDD_PLL12 (TC358767AXBG only).

Table 5.2 Operating Condition

Parameter	Symbol	Min	Typ.	Max	Unit
Supply voltage (1.8 V)	VDD18	1.71	1.8	1.89	V
Supply voltage (1.2 V)	VDD12	1.14	1.2	1.26	V
Operating temperature for TC358767AXBG/TC358867XBG	Ta	-20	—	+85	°C
Operating temperature for TC9595XBG	Ta	-40	—	+85	°C

5.3. DC Electrical Specification

VSS, VSS_DP and VSS_DSI (TC358767AXBG only) = 0 V reference

Table 5.3 DC Electrical Specification

Parameter	Symbol	Min	Typ.	Max	Unit
Input voltage High level CMOS input (Note 1)	V _{IH}	0.7 V _{DD} S	—	V _{DD} S	V
Input voltage Low level CMOS input (Note 1)	V _{IL}	0	—	0.3 V _{DD} S	V
Input voltage High level CMOS Schmitt Trigger (Note 1)	V _{IHS}	0.7 V _{DD} S	—	V _{DD} S	V
Input voltage Low level CMOS Schmitt Trigger (Note 1)	V _{ILS}	0	—	0.3 V _{DD} S	V
Output voltage High level (Note 1), (Note 2)	V _{OH}	0.8 V _{DD} S	—	V _{DD} S	V
Output voltage Low level (Note 1), (Note 2)	V _{OL}	0	—	0.2 V _{DD} S	V
Input leak current High level	I _{IH1} (Note 3)	-10	—	10	μA
Input leak current Low level	I _{IL1} (Note 4)	-10	—	10	μA
	I _{IL2} (Note 5)	-200	—	-10	μA

Note 1: V_{DD}S within recommended operating condition.

Note 2: Output current value is according to each IO buffer specification. Output voltage changes with output current value.

Note 3: Normal pin, or Pull-up I/O pin applied V_{DD}S supply voltage to input pin

Note 4: Normal pin applied VSS (0 V) to input pin

Note 5: Pull-up I/O pin applied VSS (0 V) to input pin

6. Revision History

Table 6.1 Revision History

Revision	Date	Description
0.97	2014-04-10	Newly released
0.972	2016-04-01	Modified the weight of TC358767AXBG's package by rounding up digits after the decimal point to form an integer.
1.30	2017-07-10	Changed header, footer and the last page. Added Figure 1.3 and modified descriptions in section 1. Modified descriptions in Features and section 2. Modified Table 3.1 and Figure 3.1. Added Table numbers in section 5.
1.31	2017-12-27	Modified Figure 1.1, Figure 1.2, Figure 1.3. Changed frequency to 100MHz in Figure 3.1. Added description, trademarks and registered trademarks.
1.4	2018-05-28	Modified Figure 1.1, Figure 1.2 and Figure 1.3. Modified Table 2.2 and Table 2.3. Modified Table 3.1. Deleted Table 3.2. (Table 3.2 is the same as Table 4.1.) Modified description in 5.4.
2.00	2026-05-15	Added description to power consumption. Modified Table 3.1.
1.66	2020-12-15	Modified Figure 3.1
1.70	2022-08-23	Corrected Typos in Features
1.80	2023-07-31	Removed supporting HDCP
2.00	2026-05-15	Marged with TC358867XBG and TC359595XBG. Updated the term "Master/Slave " to "Controller/Target". Deleted section 5.4. Corrected typos. Revised the last page "RESTRICTIONS ON PRODUCT USE".

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