

SSM3K347R

1. Applications

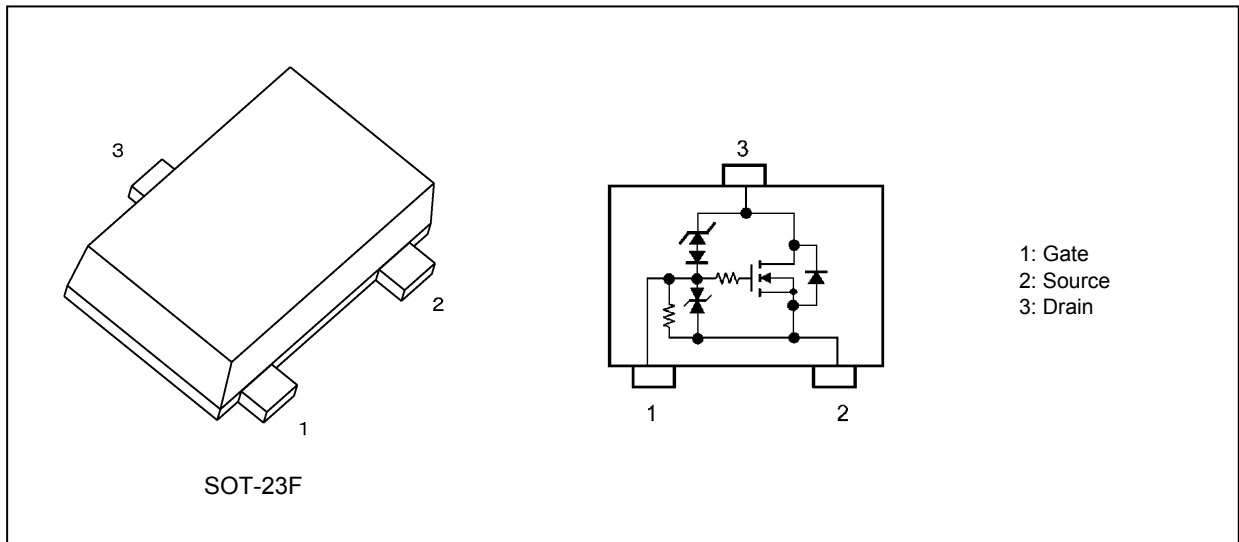
- Relay Drivers

2. Features

- (1) AEC-Q101 (Rev. D) qualified. (Note 1)
- (2) 4.0 V drive
- (3) Built-in pull down resistance 47 kΩ.
- (4) Low drain-source on-resistance
 : $R_{DS(ON)} = 480 \text{ m}\Omega$ (max) (@ $V_{GS} = 4.0 \text{ V}$)
 $R_{DS(ON)} = 410 \text{ m}\Omega$ (max) (@ $V_{GS} = 4.5 \text{ V}$)
 $R_{DS(ON)} = 340 \text{ m}\Omega$ (max) (@ $V_{GS} = 10 \text{ V}$)

Note 1: For detail information, please contact to our sales.

3. Packaging and Pin Assignment



Start of commercial production
 2016-04

4. Absolute Maximum Ratings (Note) (Unless otherwise specified, T_a = 25 °C)

Characteristics	Symbol	Rating	Unit
Drain-source voltage	V _{DS(DC)}	38	V
Gate-source voltage	V _{GSS}	±20	
Drain current (DC) (Note 1)	I _D	2	A
Drain current (pulsed) (Note 1), (Note 2)	I _{DP}	4	
Power dissipation (Note 3)	P _D	1	W
Power dissipation (t = 10 s) (Note 3)	P _D	2	
Channel temperature	T _{ch}	150	°C
Single-pulse active clamp capability (Note 4)	E _{AS}	2.2	mJ
Storage temperature	T _{stg}	-55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Ensure that the channel temperature does not exceed 150 °C.

Note 2: pulse width ≤ 10 μs, Duty ≤ 1 %

Note 3: Device mounted on a 25.4 mm × 25.4 mm × 1.6 mm FR4 glass epoxy board (Cu pad: 645 mm²)

Note 4: V_{DD} = 25 V, T_{ch} = 25 °C (Initial state)

Note: The MOSFETs in this device are sensitive to electrostatic discharge. When handling this device, the worktables, operators, soldering irons and other objects should be protected against anti-static discharge.

Note: The channel-to-ambient thermal resistance, R_{th(ch-a)}, and the drain power dissipation, P_D, vary according to the board material, board area, board thickness and pad area. When using this device, be sure to take heat dissipation fully into account.

5. Electrical Characteristics

5.1. Static Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Drain-source clamp voltage	$V_{(CL)DSS}$	$I_D = 1\text{ mA}, V_{GS} = 0\text{ V}$	38	43	48	V
Drain cut-off current	I_{DSS}	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$	—	—	10	μA
Gate leakage current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 5\text{ V}$	—	—	± 152	
Gate threshold voltage (Note 1)	V_{th}	$V_{DS} = 10\text{ V}, I_D = 1\text{ mA}$	1.4	—	2.4	V
Forward transfer admittance (Note 2)	$ Y_{fs} $	$V_{DS} = 10\text{ V}, I_D = 1.0\text{ A}$	—	4.1	—	S
Drain-source on-resistance (Note 2)	$R_{DS(ON)}$	$I_D = 0.5\text{ A}, V_{GS} = 4.0\text{ V}$	—	350	480	$\text{m}\Omega$
		$I_D = 1.0\text{ A}, V_{GS} = 4.5\text{ V}$	—	340	410	
		$I_D = 1.0\text{ A}, V_{GS} = 10\text{ V}$	—	280	340	
Pull-down resistance	R_{pd}	—	32.9	47	61.1	$\text{k}\Omega$

Note 1: Let V_{th} be the voltage applied between gate and source that causes the drain current (I_D) to be below (0.1 mA for this device). Then, for normal switching operation, $V_{GS(ON)}$ must be higher than V_{th} , and $V_{GS(OFF)}$ must be lower than V_{th} . This relationship can be expressed as: $V_{GS(OFF)} < V_{th} < V_{GS(ON)}$.

Take this into consideration when using the device.

Note 2: Pulse measurement.

5.2. Dynamic Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Input capacitance	C_{iss}	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	—	86	—	μF
Reverse transfer capacitance	C_{rss}		—	13	—	
Output capacitance	C_{oss}		—	27	—	
Switching time (turn-on time)	t_{on}	$V_{DD} = 20\text{ V}, I_D = 0.5\text{ A}, V_{GS} = 0\text{ to }4.5\text{ V}, R_G = 50\text{ }\Omega$ Duty $\leq 1\%$, Input: $t_r, t_f < 5\text{ ns}$, Common source, See Chapter 5.3.	—	380	—	ns
Switching time (turn-off time)	t_{off}		—	800	—	

5.3. Switching Time Test Circuit

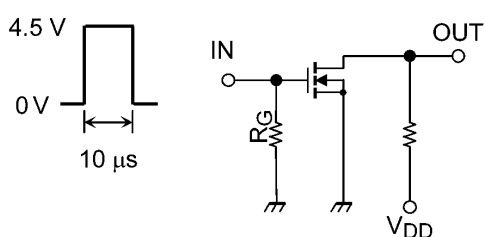


Fig. 5.3.1 Switching Time Test Circuit

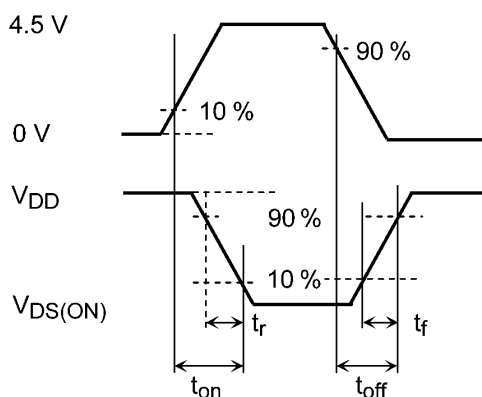


Fig. 5.3.2 Input Waveform/Output Waveform

5.4. Gate Charge Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Total gate charge (gate-source plus gate-drain)	Q_g	$V_{DD} = 20\text{ V}, I_D = 1.0\text{ A}, V_{GS} = 10\text{ V}$	—	2.5	—	nC
Gate-source charge 1	Q_{gs1}		—	0.8	—	
Gate-drain charge	Q_{gd}		—	0.5	—	

5.5. Source-Drain Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Diode forward voltage (Note 1)	V_{DSF}	$I_D = -2\text{ A}, V_{GS} = 0\text{ V}$	—	-0.87	-1.2	V

Note 1: Pulse measurement.

6. Marking

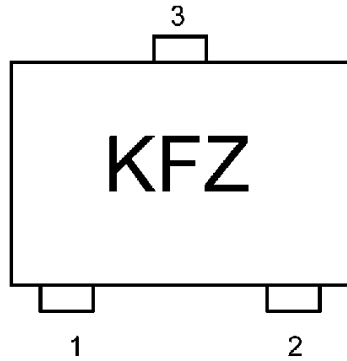


Fig. 6.1 Marking

7. Characteristics Curves (Note)

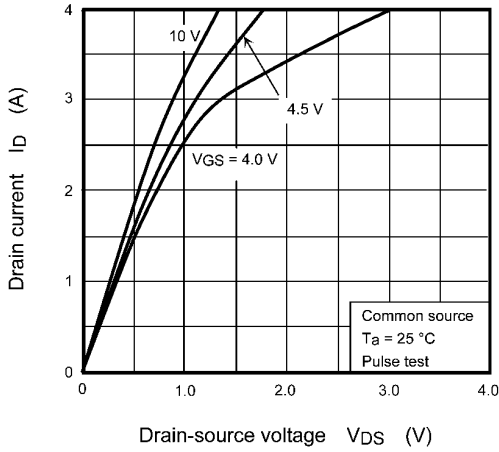


Fig. 7.1 $I_D - V_{DS}$

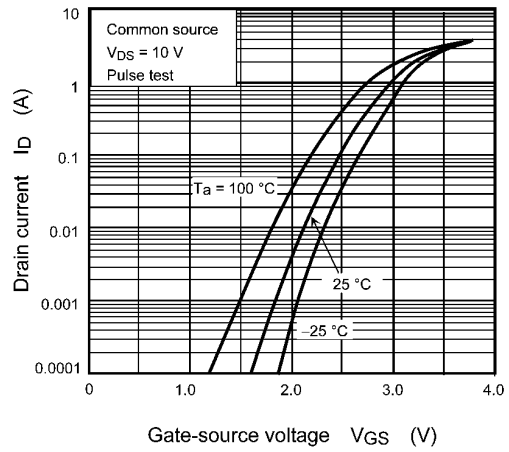


Fig. 7.2 $I_D - V_{GS}$

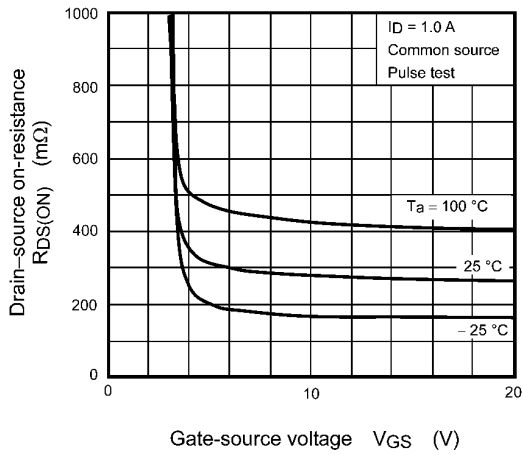


Fig. 7.3 $R_{DS(ON)} - V_{GS}$

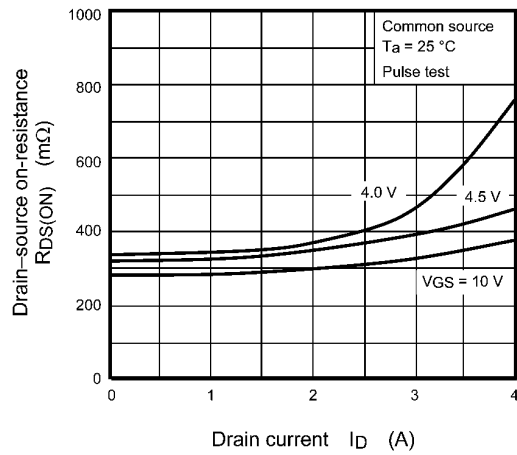


Fig. 7.4 $R_{DS(ON)} - I_D$

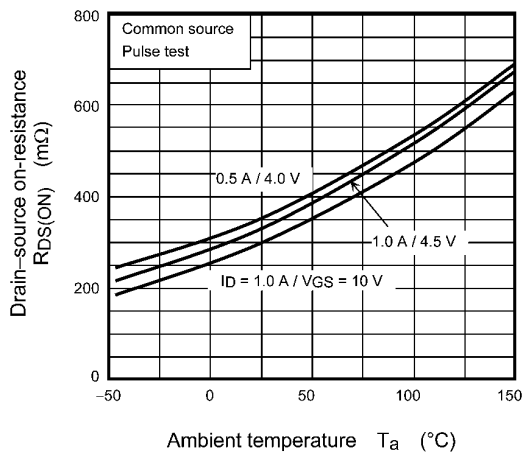


Fig. 7.5 $R_{DS(ON)} - T_a$

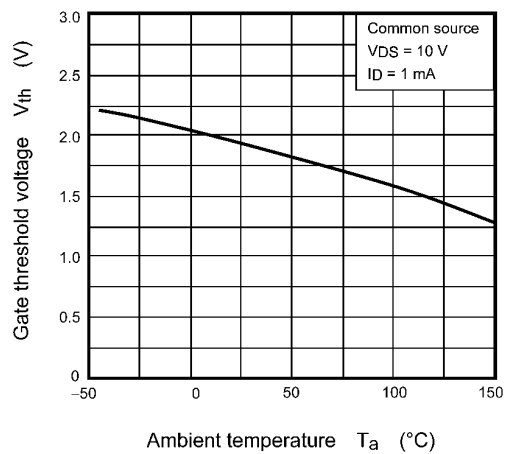


Fig. 7.6 $V_{th} - T_a$

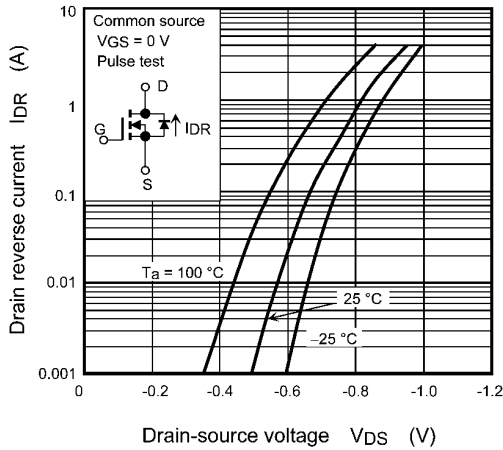


Fig. 7.7 IDR - VDS

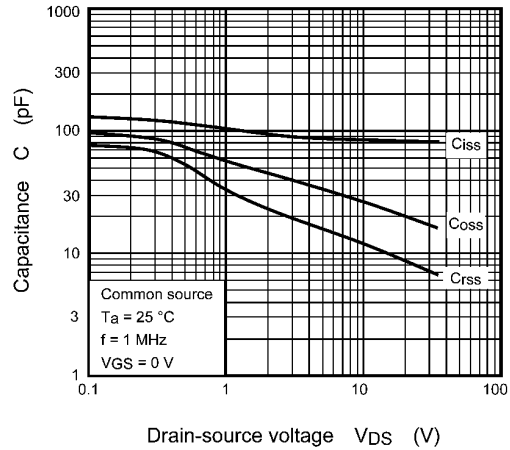


Fig. 7.8 C - VDS

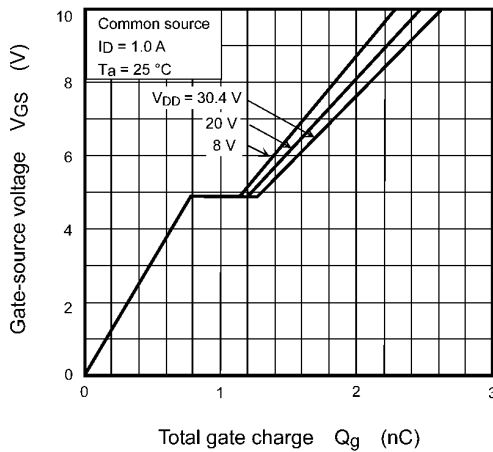


Fig. 7.9 Dynamic Input Characteristics

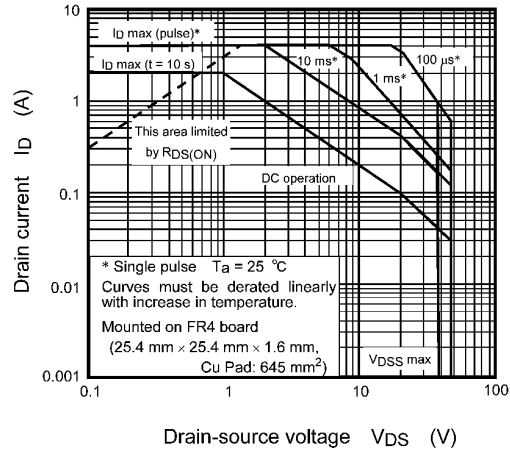


Fig. 7.10 Safe Operating Area

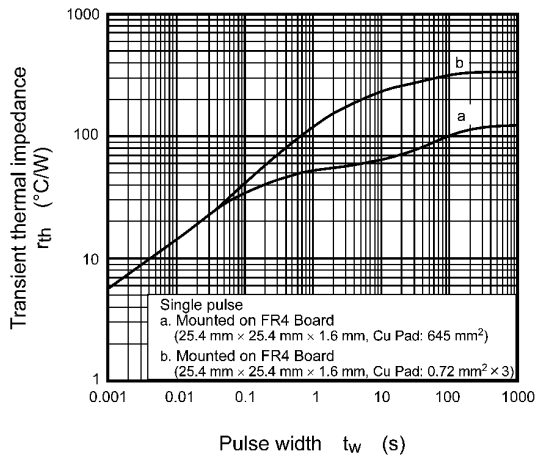


Fig. 7.11 rth - tw

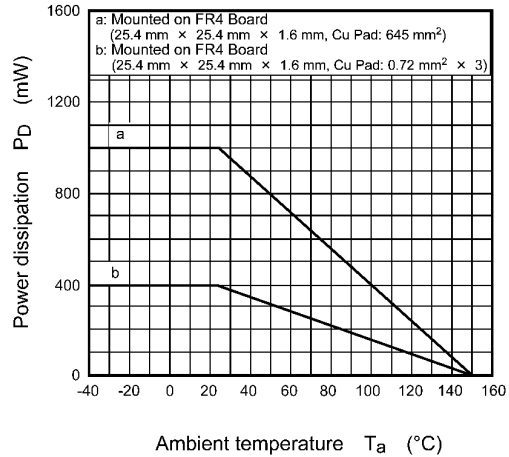


Fig. 7.12 PD - Ta

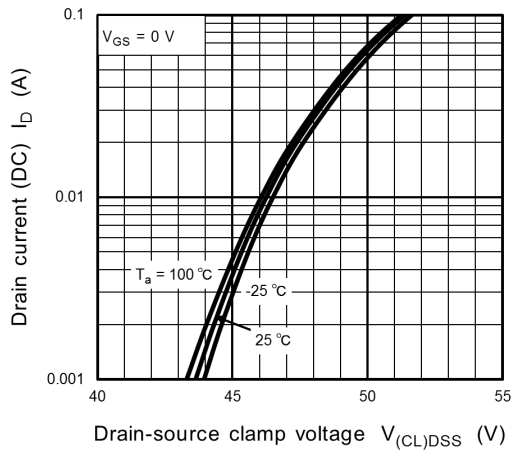
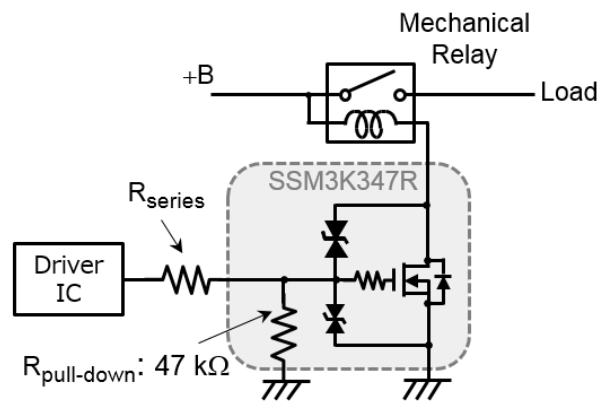


Fig. 7.13 $I_D - V_{(CL)DSS}$

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

8. ACTIVE CLAMP APPLICATION



R_{series} : Input series resistance is necessary to set to a value (range: 1 k Ω to 5 k Ω)

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