

# 74HC574D

## 1. Functional Description

- Octal D-Type Flip Flop with 3-State Outputs

## 2. General

The 74HC574D is a high speed CMOS OCTAL FLIP-FLOP with 3-STATE OUTPUT fabricated with silicon gate C<sup>2</sup>MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

These 8-bit D-type flip-flops are controlled by a clock input (CK) and an output enable input ( $\overline{OE}$ ).

When the  $\overline{OE}$  input is high, the eight outputs are in a high impedance state.

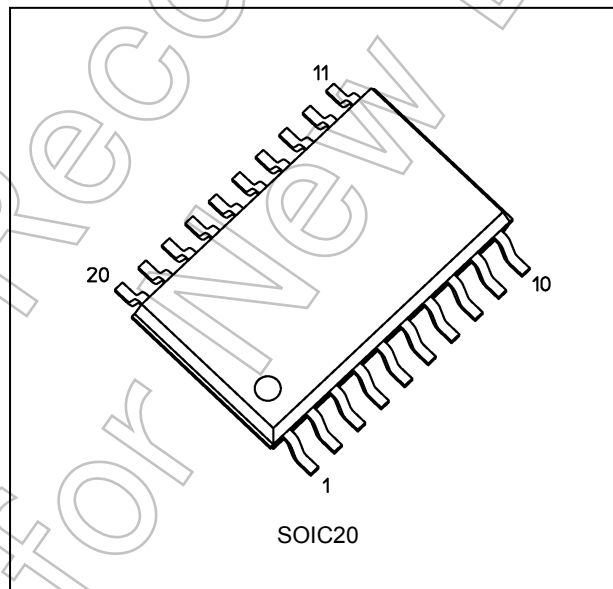
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

## 3. Features

- (1) Wide operating temperature range:  $T_{opr} = -40$  to  $125$  °C (Note 1)
- (2) High speed:  $f_{MAX} = 59$  MHz (typ.) at  $V_{CC} = 6.0$  V
- (3) Low power dissipation:  $I_{CC} = 4.0$   $\mu$ A (max) at  $T_a = 25$  °C
- (4) Balanced propagation delays:  $t_{PLH} \approx t_{PHL}$
- (5) Wide operating voltage range:  $V_{CC(opr)} = 2.0$  V to  $6.0$  V

Note 1: Operating Range spec of  $T_{opr} = -40$  °C to  $125$  °C is applicable only for the products which manufactured after July 2020.

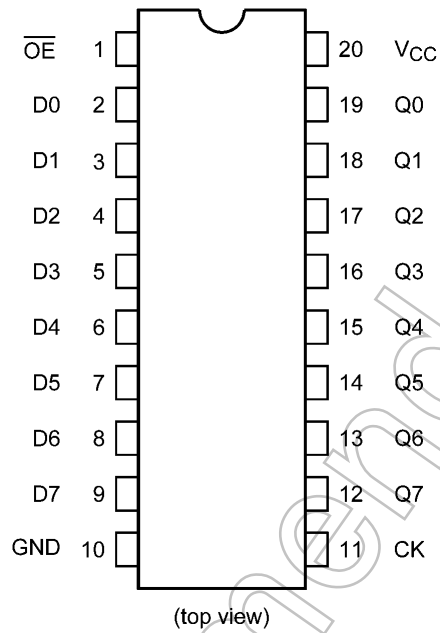
## 4. Packaging



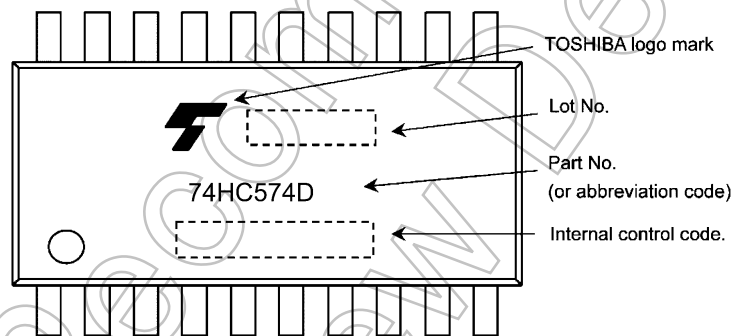
Start of commercial production

2020-07

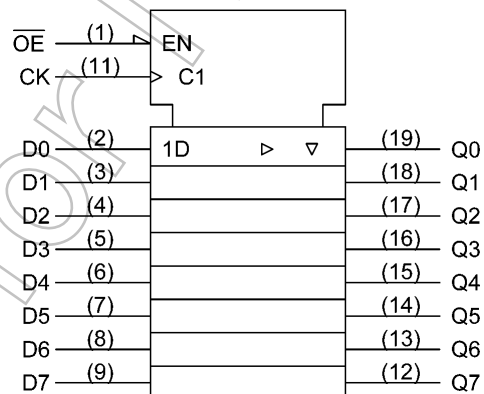
### 5. Pin Assignment






### 6. Marking



### 7. IEC Logic Symbol

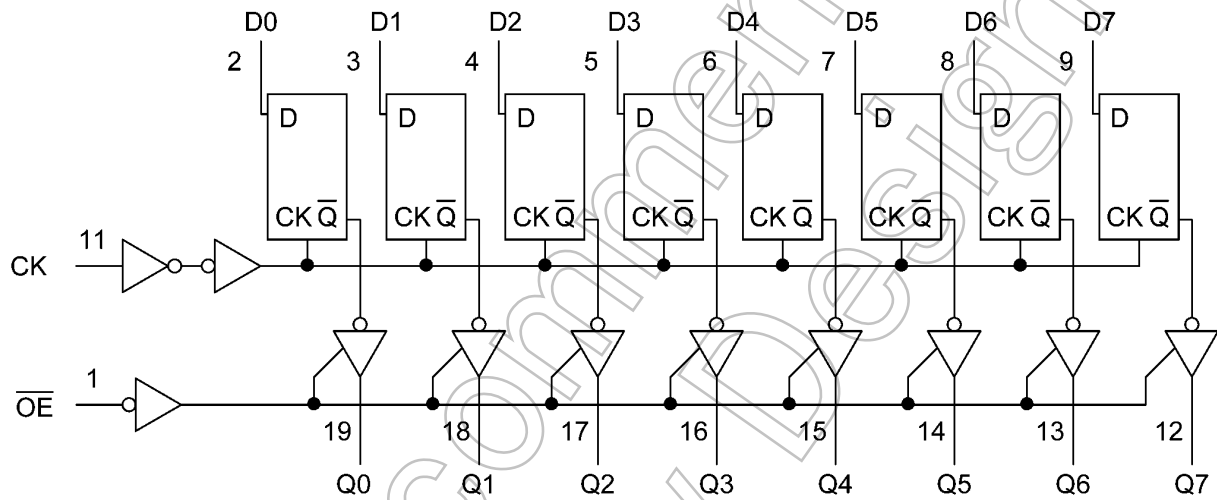


## 8. Truth Table

Inputs			Output
$\overline{OE}$	CK	D	
H	X	X	Z
L		X	Qn
L		L	L
L		H	H

X: Don't care  
 Z: High impedance  
 Qn: No change

## 9. System Diagram



### 10. Absolute Maximum Ratings (Note)

Characteristics	Symbol	Note	Rating	Unit
Supply voltage	$V_{CC}$		-0.5 to 7.0	V
Input voltage	$V_{IN}$		-0.5 to $V_{CC} + 0.5$	V
Output voltage	$V_{OUT}$		-0.5 to $V_{CC} + 0.5$	V
Input diode current	$I_{IK}$		$\pm 20$	mA
Output diode current	$I_{OK}$		$\pm 20$	mA
Output current	$I_{OUT}$		$\pm 35$	mA
$V_{CC}$ /ground current	$I_{CC}$		$\pm 75$	mA
Power dissipation	$P_D$	(Note 1)	500	mW
Storage temperature	$T_{stg}$		-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1:  $P_D$  derates linearly with -8 mW/°C above 85 °C

### 11. Operating Ranges (Note)

Characteristics	Symbol	Note	Test Condition	Rating	Unit
Supply voltage	$V_{CC}$			2.0 to 6.0	V
Input voltage	$V_{IN}$			0 to $V_{CC}$	V
Output voltage	$V_{OUT}$			0 to $V_{CC}$	V
Operating temperature	$T_{opr}$	(Note 1)		-40 to 125	°C
Input rise and fall times	$t_r, t_f$		$V_{CC} = 2.0$ V	0 to 1000	ns
			$V_{CC} = 4.5$ V	0 to 500	
			$V_{CC} = 6.0$ V	0 to 400	
	(Note 1)	—	0 to 50	$\mu$ s	

Note: The operating ranges must be maintained to ensure the normal operation of the device.

Unused inputs must be tied to either  $V_{CC}$  or GND.

Note 1: Operating Range spec of  $T_{opr} = -40$  °C to 125 °C is applicable only for the products which manufactured after July 2020.

### 12. Electrical Characteristics

#### 12.1. DC Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$ )

Characteristics	Symbol	Test Condition		$V_{CC}$ (V)	Min	Typ.	Max	Unit
High-level input voltage	$V_{IH}$	—		2.0	1.50	—	—	V
				4.5	3.15	—	—	
				6.0	4.20	—	—	
Low-level input voltage	$V_{IL}$	—		2.0	—	—	0.50	V
				4.5	—	—	1.35	
				6.0	—	—	1.80	
High-level output voltage	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -20\text{ }\mu\text{A}$	2.0	1.9	2.0	—	V
				4.5	4.4	4.5	—	
			6.0	5.9	6.0	—		
			$I_{OH} = -6\text{ mA}$	4.5	4.18	4.31	—	
			$I_{OH} = -7.8\text{ mA}$	6.0	5.68	5.80	—	
Low-level output voltage	$V_{OL}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 20\text{ }\mu\text{A}$	2.0	—	0.0	0.1	V
				4.5	—	0.0	0.1	
			6.0	—	0.0	0.1		
			$I_{OL} = 6\text{ mA}$	4.5	—	0.17	0.26	
			$I_{OL} = 7.8\text{ mA}$	6.0	—	0.18	0.26	
3-state output OFF-state leakage current	$I_{OZ}$	$V_{IN} = V_{IH}$ or $V_{IL}$ $V_{OUT} = V_{CC}$ or GND		6.0	—	—	$\pm 0.5$	$\mu\text{A}$
Input leakage current	$I_{IN}$	$V_{IN} = V_{CC}$ or GND		6.0	—	—	$\pm 0.1$	$\mu\text{A}$
Quiescent supply current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND		6.0	—	—	4.0	$\mu\text{A}$

#### 12.2. DC Characteristics (Unless otherwise specified, $T_a = -40$ to $85\text{ }^\circ\text{C}$ )

Characteristics	Symbol	Test Condition		$V_{CC}$ (V)	Min	Max	Unit
High-level input voltage	$V_{IH}$	—		2.0	1.50	—	V
				4.5	3.15	—	
				6.0	4.20	—	
Low-level input voltage	$V_{IL}$	—		2.0	—	0.50	V
				4.5	—	1.35	
				6.0	—	1.80	
High-level output voltage	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -20\text{ }\mu\text{A}$	2.0	1.9	—	V
				4.5	4.4	—	
			6.0	5.9	—		
			$I_{OH} = -6\text{ mA}$	4.5	4.13	—	
			$I_{OH} = -7.8\text{ mA}$	6.0	5.63	—	
Low-level output voltage	$V_{OL}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 20\text{ }\mu\text{A}$	2.0	—	0.1	V
				4.5	—	0.1	
			6.0	—	0.1		
			$I_{OL} = 6\text{ mA}$	4.5	—	0.33	
			$I_{OL} = 7.8\text{ mA}$	6.0	—	0.33	
3-state output OFF-state leakage current	$I_{OZ}$	$V_{IN} = V_{IH}$ or $V_{IL}$ $V_{OUT} = V_{CC}$ or GND		6.0	—	$\pm 5.0$	$\mu\text{A}$
Input leakage current	$I_{IN}$	$V_{IN} = V_{CC}$ or GND		6.0	—	$\pm 1.0$	$\mu\text{A}$
Quiescent supply current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND		6.0	—	40.0	$\mu\text{A}$

### 12.3. DC Characteristics (Note) (Unless otherwise specified, $T_a = -40$ to $125$ °C)

Characteristics	Symbol	Test Condition	$V_{CC}$ (V)	Min	Max	Unit		
High-level input voltage	$V_{IH}$	—	2.0	1.50	—	V		
			4.5	3.15	—			
			6.0	4.20	—			
Low-level input voltage	$V_{IL}$	—	2.0	—	0.50	V		
			4.5	—	1.35			
			6.0	—	1.80			
High-level output voltage	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -20$ $\mu$ A	2.0	1.9	—	V	
				4.5	4.4	—		
				6.0	5.9	—		
			$I_{OH} = -6$ mA	4.5	3.7	—		
				6.0	$I_{OH} = -7.8$ mA	5.2		—
						—		—
Low-level output voltage	$V_{OL}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 20$ $\mu$ A	2.0	—	0.1	V	
				4.5	—	0.1		
				6.0	—	0.1		
			$I_{OL} = 6$ mA	4.5	—	0.4		
				6.0	$I_{OL} = 7.8$ mA	—		0.4
						—		—
3-state output OFF-state leakage current	$I_{OZ}$	$V_{IN} = V_{IH}$ or $V_{IL}$ $V_{OUT} = V_{CC}$ or GND	6.0	—	$\pm 5.0$	$\mu$ A		
Input leakage current	$I_{IN}$	$V_{IN} = V_{CC}$ or GND	6.0	—	$\pm 1.0$	$\mu$ A		
Quiescent supply current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND	6.0	—	80.0	$\mu$ A		

Note: Operating Range spec of  $T_{opr} = -40$  °C to  $125$  °C is applicable only for the products which manufactured after July 2020.

Not Recommended for New Design

### 12.4. Timing Requirements (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$ , Input: $t_r = t_f = 6\text{ ns}$ )

Characteristics	Symbol	Test Condition	$V_{CC}$ (V)	Typ.	Limit	Unit
Minimum pulse width (CK)	$t_{w(L)}, t_{w(H)}$	—	2.0	—	75	ns
			4.5	—	15	
			6.0	—	13	
Minimum setup time (Dn)	$t_s$	—	2.0	—	75	ns
			4.5	—	15	
			6.0	—	13	
Minimum hold time (Dn)	$t_h$	—	2.0	—	0	ns
			4.5	—	0	
			6.0	—	0	
Clock frequency	f	—	2.0	—	6	MHz
			4.5	—	31	
			6.0	—	36	

### 12.5. Timing Requirements (Unless otherwise specified, $T_a = -40\text{ to }85\text{ }^\circ\text{C}$ , Input: $t_r = t_f = 6\text{ ns}$ )

Characteristics	Symbol	Test Condition	$V_{CC}$ (V)	Limit	Unit
Minimum pulse width (CK)	$t_{w(L)}, t_{w(H)}$	—	2.0	95	ns
			4.5	19	
			6.0	16	
Minimum setup time (Dn)	$t_s$	—	2.0	95	ns
			4.5	19	
			6.0	16	
Minimum hold time (Dn)	$t_h$	—	2.0	0	ns
			4.5	0	
			6.0	0	
Clock frequency	f	—	2.0	5	MHz
			4.5	24	
			6.0	28	

### 12.6. Timing Requirements (Note) (Unless otherwise specified, $T_a = -40\text{ to }125\text{ }^\circ\text{C}$ , Input: $t_r = t_f = 6\text{ ns}$ )

Characteristics	Symbol	Test Condition	$V_{CC}$ (V)	Limit	Unit
Minimum pulse width (CK)	$t_{w(L)}, t_{w(H)}$	—	2.0	108	ns
			4.5	22	
			6.0	18	
Minimum setup time (Dn)	$t_s$	—	2.0	108	ns
			4.5	22	
			6.0	18	
Minimum hold time (Dn)	$t_h$	—	2.0	0	ns
			4.5	0	
			6.0	0	
Clock frequency	f	—	2.0	4	MHz
			4.5	19	
			6.0	23	

Note: Operating Range spec of  $T_{opr} = -40\text{ }^\circ\text{C}$  to  $125\text{ }^\circ\text{C}$  is applicable only for the products which manufactured after July 2020.

### 12.7. AC Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$ , Input: $t_r = t_f = 6\text{ ns}$ )

Characteristics	Symbol	Note	Test Condition	$C_L$ (pF)	$V_{CC}$ (V)	Min	Typ.	Max	Unit
Output transition time	$t_{TLH}, t_{THL}$		—	50	2.0	—	25	60	ns
					4.5	—	7	12	
					6.0	—	6	10	
Propagation delay time (CK-Q)	$t_{PLH}, t_{PHL}$		—	50	2.0	—	70	150	ns
					4.5	—	20	30	
					6.0	—	15	26	
				150	2.0	—	88	190	
					4.5	—	25	38	
					6.0	—	19	33	
Output enable time	$t_{PZL}, t_{PZH}$		$R_L = 1\text{ k}\Omega$	50	2.0	—	48	125	ns
					4.5	—	15	25	
					6.0	—	12	21	
				150	2.0	—	60	165	
					4.5	—	20	33	
					6.0	—	16	28	
Output disable time	$t_{PLZ}, t_{PHZ}$		$R_L = 1\text{ k}\Omega$	50	2.0	—	34	125	ns
					4.5	—	17	25	
					6.0	—	15	21	
Maximum clock frequency	$f_{MAX}$		—	50	2.0	6	17	—	MHz
					4.5	31	50	—	
					6.0	36	59	—	
Input capacitance	$C_{IN}$		—			—	5	10	pF
Output capacitance	$C_{OUT}$		—			—	10	—	pF
Power dissipation capacitance	$C_{PD}$	(Note 1)	—			—	54	—	pF

Note 1:  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation.

$$I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/8 \text{ (per latch)}$$

And the total  $C_{PD}$  when n pcs of latch operate can be gained by the following equation.

$$C_{PD} \text{ (total)} = 39 + 15 \times n$$

### 12.8. AC Characteristics

(Unless otherwise specified,  $T_a = -40$  to  $85$  °C, Input:  $t_r = t_f = 6$  ns)

Characteristics	Symbol	Test Condition	$C_L$ (pF)	$V_{CC}$ (V)	Min	Max	Unit
Output transition time	$t_{TLH}, t_{THL}$	—	50	2.0	—	75	ns
				4.5	—	15	
				6.0	—	13	
Propagation delay time (CK-Q)	$t_{PLH}, t_{PHL}$	—	50	2.0	—	190	ns
				4.5	—	38	
				6.0	—	33	
			150	2.0	—	240	
				4.5	—	48	
				6.0	—	41	
Output enable time	$t_{PZL}, t_{PZH}$	$R_L = 1\text{ k}\Omega$	50	2.0	—	155	ns
				4.5	—	31	
				6.0	—	26	
			150	2.0	—	205	
				4.5	—	41	
				6.0	—	35	
Output disable time	$t_{PLZ}, t_{PHZ}$	$R_L = 1\text{ k}\Omega$	50	2.0	—	155	ns
				4.5	—	31	
				6.0	—	26	
Maximum clock frequency	$f_{MAX}$	—	50	2.0	5	—	MHz
				4.5	24	—	
				6.0	28	—	
Input capacitance	$C_{IN}$	—	—	—	—	10	pF

Not Recommended for New Design

### 12.9. AC Characteristics (Note)

(Unless otherwise specified,  $T_a = -40$  to  $125$  °C, Input:  $t_r = t_f = 6$  ns)

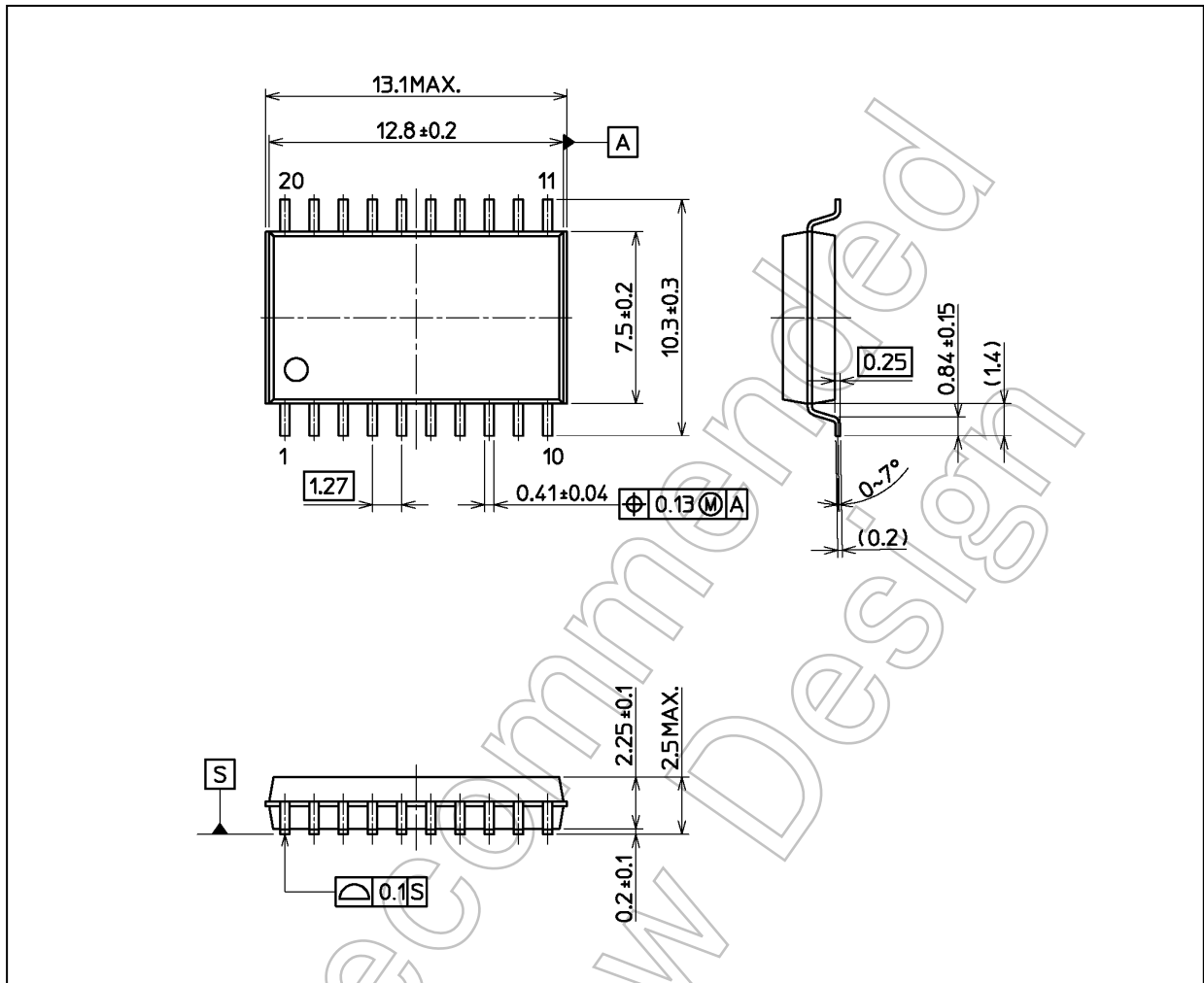
Characteristics	Symbol	Test Condition	$V_{CC}$ (V)	$C_L$ (pF)	Min	Max	Unit
Output transition time	$t_{TLH}, t_{THL}$	—	2.0	50	—	85	ns
			4.5		—	17	
			6.0		—	15	
Propagation delay time (CK-Q)	$t_{PLH}, t_{PHL}$	—	2.0	50	—	217	ns
			4.5		—	43	
			6.0		—	38	
			2.0	150	—	273	
			4.5		—	55	
			6.0		—	46	
Output enable time	$t_{PZL}, t_{PZH}$	$R_L = 1$ k $\Omega$	2.0	50	—	175	ns
			4.5		—	35	
			6.0		—	29	
			2.0	150	—	232	
			4.5		—	46	
			6.0		—	40	
Output disable time	$t_{PLZ}, t_{PHZ}$	$R_L = 1$ k $\Omega$	2.0	50	—	175	ns
			4.5		—	35	
			6.0		—	29	
Maximum clock frequency	$f_{MAX}$	—	2.0	50	4	—	MHz
			4.5		19	—	
			6.0		23	—	
Input capacitance	$C_{IN}$	—	—	—	—	10	pF

Note: Operating Range spec of  $T_{opr} = -40$  °C to  $125$  °C is applicable only for the products which manufactured after July 2020.

Not Recommended for New

## Package Dimensions

Unit: mm



Weight: 0.51 g (typ.)

Package Name(s)
Nickname: SOIC20

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