

# 74HC175D

## 1. Functional Description

- Quad D-Type Flip-Flop with Clear

## 2. General

The 74HC175D is a high speed CMOS D-TYPE FLIP FLOP fabricated with silicon gate C<sup>2</sup>MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

Information signals applied to D inputs are transferred to the Q and  $\bar{Q}$  outputs on the positive going edge of the clock pulse.

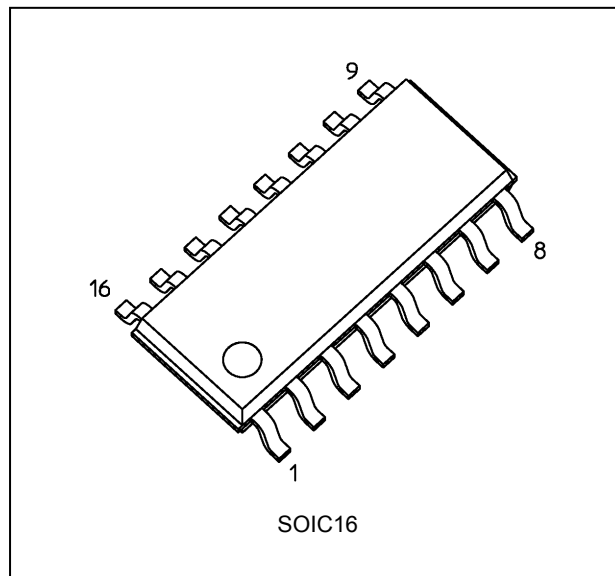
When the  $\overline{\text{CLR}}$  input is held low, the Q outputs are at the low logic level and the  $\bar{Q}$  outputs are at the high logic level independent of the other inputs.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

## 3. Features

- (1) High speed:  $f_{\text{MAX}} = 63 \text{ MHz}$  (typ.) at  $V_{\text{CC}} = 5 \text{ V}$
- (2) Low power dissipation:  $I_{\text{CC}} = 4.0 \mu\text{A}$  (max) at  $T_a = 25 \text{ }^\circ\text{C}$
- (3) Balanced propagation delays:  $t_{\text{PLH}} \approx t_{\text{PHL}}$
- (4) Wide operating voltage range:  $V_{\text{CC(opr)}} = 2.0 \text{ V to } 6.0 \text{ V}$

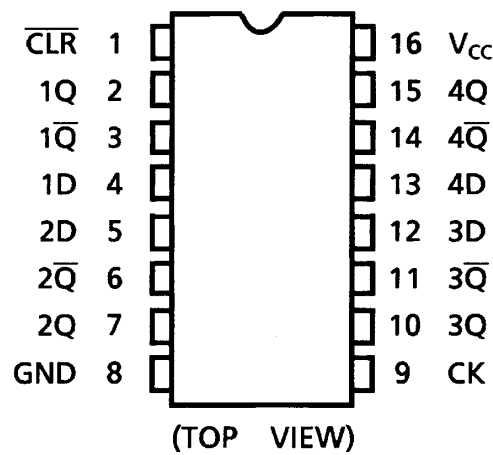
## 4. Packaging



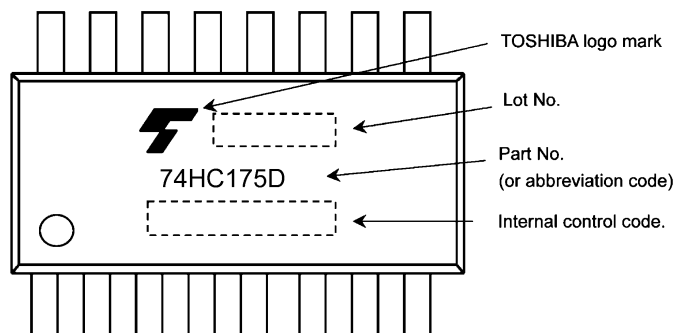
Start of commercial production

2016-05

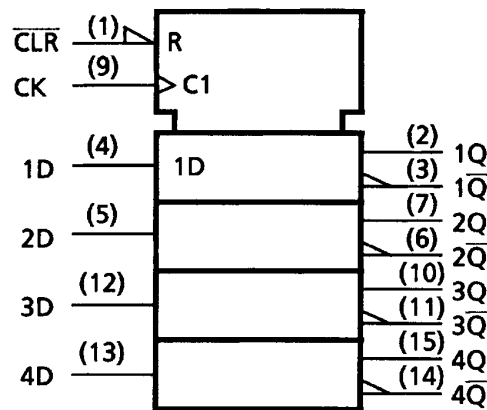
**5. Pin Assignment**



**6. Marking**



**7. IEC Logic Symbol**

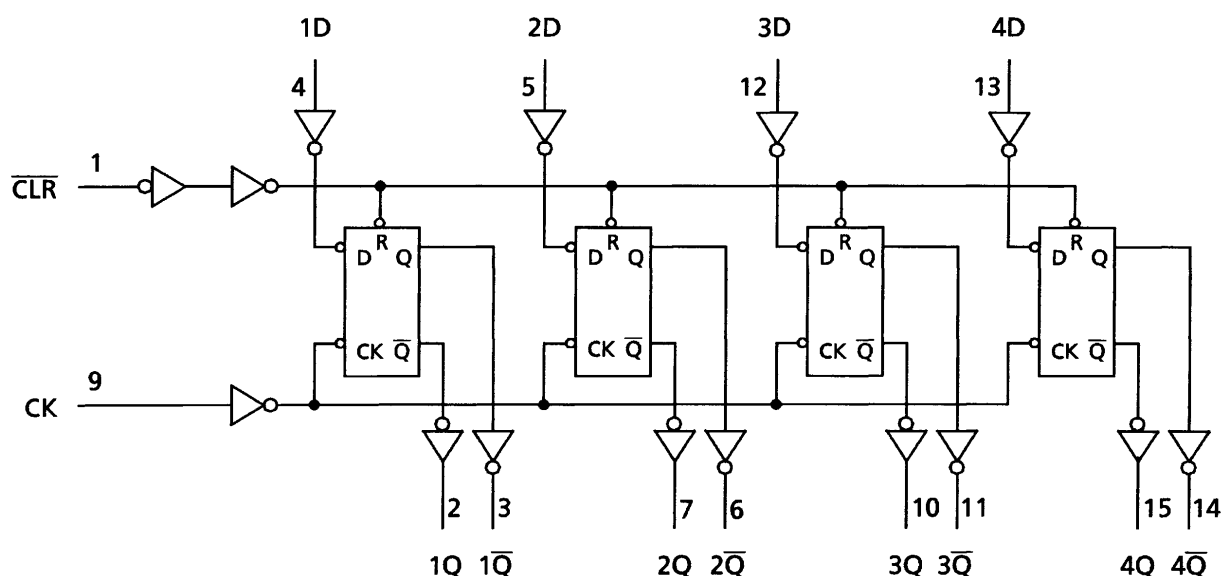


**8. Truth Table**

Inputs			Outputs		Function
CLR	D	CK	Q	Q̄	
L	X	X	L	H	Clear
H	L	↑	L	H	—
H	H	↑	H	L	—
H	X	↓	Q <sub>n</sub>	Q̄ <sub>n</sub>	No Change

X: Don't care

**9. System Diagram**



**10. Absolute Maximum Ratings (Note)**

Characteristics	Symbol	Note	Rating	Unit
Supply voltage	$V_{CC}$		-0.5 to 7.0	V
Input voltage	$V_{IN}$		-0.5 to $V_{CC} + 0.5$	V
Output voltage	$V_{OUT}$		-0.5 to $V_{CC} + 0.5$	V
Input diode current	$I_{IK}$		$\pm 20$	mA
Output diode current	$I_{OK}$		$\pm 20$	mA
Output current	$I_{OUT}$		$\pm 25$	mA
$V_{CC}$ /ground current	$I_{CC}$		$\pm 50$	mA
Power dissipation	$P_D$	(Note 1)	500	mW
Storage temperature	$T_{stg}$		-65 to 150	$^{\circ}C$

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1:  $P_D$  derates linearly with -8 mW/ $^{\circ}C$  above 85  $^{\circ}C$

**11. Operating Ranges (Note)**

Characteristics	Symbol	Test Condition	Rating	Unit
Supply voltage	$V_{CC}$	—	2.0 to 6.0	V
Input voltage	$V_{IN}$	—	0 to $V_{CC}$	V
Output voltage	$V_{OUT}$	—	0 to $V_{CC}$	V
Operating temperature	$T_{opr}$	—	-40 to 125	$^{\circ}C$
Input rise and fall times	$t_r, t_f$	—	0 to 50	$\mu s$

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either  $V_{CC}$  or GND.

**12. Electrical Characteristics**

**12.1. DC Characteristics (Unless otherwise specified,  $T_a = 25\text{ }^\circ\text{C}$ )**

Characteristics	Symbol	Test Condition		$V_{CC}$ (V)	Min	Typ.	Max	Unit
High-level input voltage	$V_{IH}$	—		2.0	1.50	—	—	V
				4.5	3.15	—	—	
				6.0	4.20	—	—	
Low-level input voltage	$V_{IL}$	—		2.0	—	—	0.50	V
				4.5	—	—	1.35	
				6.0	—	—	1.80	
High-level output voltage	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -20\text{ }\mu\text{A}$	2.0	1.9	2.0	—	V
				4.5	4.4	4.5	—	
			6.0	5.9	6.0	—		
			$I_{OH} = -4\text{ mA}$	4.5	4.18	4.31	—	
			$I_{OH} = -5.2\text{ mA}$	6.0	5.68	5.80	—	
Low-level output voltage	$V_{OL}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 20\text{ }\mu\text{A}$	2.0	—	0.0	0.1	V
				4.5	—	0.0	0.1	
				6.0	—	0.0	0.1	
			$I_{OL} = 4\text{ mA}$	4.5	—	0.17	0.26	
			$I_{OL} = 5.2\text{ mA}$	6.0	—	0.18	0.26	
Input leakage current	$I_{IN}$	$V_{IN} = V_{CC}$ or GND		6.0	—	—	$\pm 0.1$	$\mu\text{A}$
Quiescent supply current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND		6.0	—	—	4.0	$\mu\text{A}$

**12.2. DC Characteristics (Unless otherwise specified,  $T_a = -40$  to  $85\text{ }^\circ\text{C}$ )**

Characteristics	Symbol	Test Condition		$V_{CC}$ (V)	Min	Max	Unit
High-level input voltage	$V_{IH}$	—		2.0	1.50	—	V
				4.5	3.15	—	
				6.0	4.20	—	
Low-level input voltage	$V_{IL}$	—		2.0	—	0.50	V
				4.5	—	1.35	
				6.0	—	1.80	
High-level output voltage	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -20\text{ }\mu\text{A}$	2.0	1.9	—	V
				4.5	4.4	—	
			6.0	5.9	—		
			$I_{OH} = -4\text{ mA}$	4.5	4.13	—	
			$I_{OH} = -5.2\text{ mA}$	6.0	5.63	—	
Low-level output voltage	$V_{OL}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 20\text{ }\mu\text{A}$	2.0	—	0.1	V
				4.5	—	0.1	
				6.0	—	0.1	
			$I_{OL} = 4\text{ mA}$	4.5	—	0.33	
			$I_{OL} = 5.2\text{ mA}$	6.0	—	0.33	
Input leakage current	$I_{IN}$	$V_{IN} = V_{CC}$ or GND		6.0	—	$\pm 1.0$	$\mu\text{A}$
Quiescent supply current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND		6.0	—	40.0	$\mu\text{A}$

**12.3. DC Characteristics (Unless otherwise specified,  $T_a = -40$  to  $125$  °C)**

Characteristics	Symbol	Test Condition		$V_{CC}$ (V)	Min	Max	Unit
High-level input voltage	$V_{IH}$	—		2.0	1.50	—	V
				4.5	3.15	—	
				6.0	4.20	—	
Low-level input voltage	$V_{IL}$	—		2.0	—	0.50	V
				4.5	—	1.35	
				6.0	—	1.80	
High-level output voltage	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -20 \mu A$	2.0	1.9	—	V
				4.5	4.4	—	
				6.0	5.9	—	
			$I_{OH} = -4$ mA	4.5	3.7	—	
			$I_{OH} = -5.2$ mA	6.0	5.2	—	
Low-level output voltage	$V_{OL}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 20 \mu A$	2.0	—	0.1	V
				4.5	—	0.1	
				6.0	—	0.1	
			$I_{OL} = 4$ mA	4.5	—	0.4	
				6.0	—	0.4	
Input leakage current	$I_{IN}$	$V_{IN} = V_{CC}$ or GND		6.0	—	$\pm 1.0$	$\mu A$
Quiescent supply current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND		6.0	—	160.0	$\mu A$

**12.4. Timing Requirements (Unless otherwise specified,  $T_a = 25\text{ }^\circ\text{C}$ , Input:  $t_r = t_f = 6\text{ ns}$ )**

Characteristics	Symbol	Test Condition	$V_{CC}$ (V)	Typ.	Limit	Unit
Minimum pulse width (CK)	$t_{w(L)}, t_{w(H)}$	—	2.0	—	75	ns
			4.5	—	15	
			6.0	—	13	
Minimum pulse width (CLR)	$t_{w(L)}$	—	2.0	—	75	ns
			4.5	—	15	
			6.0	—	13	
Minimum setup time	$t_S$	—	2.0	—	75	ns
			4.5	—	15	
			6.0	—	13	
Minimum hold time	$t_h$	—	2.0	—	0	ns
			4.5	—	0	
			6.0	—	0	
Minimum removal time	$t_{rem}$	—	2.0	—	75	ns
			4.5	—	15	
			6.0	—	13	
Clock frequency	f	—	2.0	—	6	MHz
			4.5	—	31	
			6.0	—	36	

**12.5. Timing Requirements (Unless otherwise specified,  $T_a = -40\text{ to }85\text{ }^\circ\text{C}$ , Input:  $t_r = t_f = 6\text{ ns}$ )**

Characteristics	Symbol	Test Condition	$V_{CC}$ (V)	Limit	Unit
Minimum pulse width (CK)	$t_{w(L)}, t_{w(H)}$	—	2.0	95	ns
			4.5	19	
			6.0	16	
Minimum pulse width (CLR)	$t_{w(L)}$	—	2.0	95	ns
			4.5	19	
			6.0	16	
Minimum setup time	$t_S$	—	2.0	95	ns
			4.5	19	
			6.0	16	
Minimum hold time	$t_h$	—	2.0	0	ns
			4.5	0	
			6.0	0	
Minimum removal time	$t_{rem}$	—	2.0	95	ns
			4.5	19	
			6.0	16	
Clock frequency	f	—	2.0	5	MHz
			4.5	25	
			6.0	29	

**12.6. Timing Requirements**  
 (Unless otherwise specified,  $T_a = -40$  to  $125\text{ }^\circ\text{C}$ , Input:  $t_r = t_f = 6\text{ ns}$ )

Characteristics	Symbol	Test Condition	$V_{CC}$ (V)	Limit	Unit
Minimum pulse width (CK)	$t_{w(L)}, t_{w(H)}$	—	2.0	110	ns
			4.5	22	
			6.0	19	
Minimum pulse width (CLR)	$t_{w(L)}$	—	2.0	110	ns
			4.5	22	
			6.0	19	
Minimum setup time	$t_s$	—	2.0	110	ns
			4.5	22	
			6.0	19	
Minimum hold time	$t_h$	—	2.0	0	ns
			4.5	0	
			6.0	0	
Minimum removal time	$t_{rem}$	—	2.0	110	ns
			4.5	22	
			6.0	19	
Clock frequency	f	—	2.0	4	MHz
			4.5	20	
			6.0	24	

**12.7. AC Characteristics**  
 (Unless otherwise specified,  $C_L = 15\text{ pF}$ ,  $V_{CC} = 5\text{ V}$ ,  $T_a = 25\text{ }^\circ\text{C}$ , Input:  $t_r = t_f = 6\text{ ns}$ )

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Output transition time	$t_{TLH}, t_{THL}$	—	—	4	8	ns
Propagation delay time (CK-Q, Q)	$t_{PLH}, t_{PHL}$	—	—	16	24	ns
Propagation delay time (CLR-Q, Q)	$t_{PLH}, t_{PHL}$	—	—	13	21	ns
Maximum clock frequency	$f_{MAX}$	—	36	63	—	MHz

**12.8. AC Characteristics (Unless otherwise specified,  $C_L = 50 \text{ pF}$ ,  $T_a = 25 \text{ }^\circ\text{C}$ , Input:  $t_r = t_f = 6 \text{ ns}$ )**

Characteristics	Symbol	Note	Test Condition	$V_{CC}$ (V)	Min	Typ.	Max	Unit
Output transition time	$t_{TLH}, t_{THL}$		—	2.0	—	30	75	ns
				4.5	—	8	15	
				6.0	—	7	13	
Propagation delay time (CK-Q, $\bar{Q}$ )	$t_{PLH}, t_{PHL}$		—	2.0	—	70	140	ns
				4.5	—	19	28	
				6.0	—	16	24	
Propagation delay time (CLR-Q, $\bar{Q}$ )	$t_{PLH}, t_{PHL}$		—	2.0	—	50	125	ns
				4.5	—	16	25	
				6.0	—	12	22	
Maximum clock frequency	$f_{MAX}$		—	2.0	6	14	—	MHz
				4.5	31	53	—	
				6.0	36	63	—	
Input capacitance	$C_{IN}$		—	—	3	—	pF	
Power dissipation capacitance	$C_{PD}$	(Note 1)	—	—	5	—	pF	

Note 1:  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation.

$$I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/4 \text{ (per F/F)}$$

And the total  $C_{PD}$  when n pcs of latch operate can be gained by the following equation.

$$C_{PD} \text{ (total)} = 32 + 21 \times n$$

**12.9. AC Characteristics (Unless otherwise specified,  $C_L = 50 \text{ pF}$ ,  $T_a = -40 \text{ to } 85 \text{ }^\circ\text{C}$ , Input:  $t_r = t_f = 6 \text{ ns}$ )**

Characteristics	Symbol	Test Condition	$V_{CC}$ (V)	Min	Max	Unit
Output transition time	$t_{TLH}, t_{THL}$	—	2.0	—	95	ns
			4.5	—	19	
			6.0	—	16	
Propagation delay time (CK-Q, $\bar{Q}$ )	$t_{PLH}, t_{PHL}$	—	2.0	—	175	ns
			4.5	—	35	
			6.0	—	30	
Propagation delay time (CLR-Q, $\bar{Q}$ )	$t_{PLH}, t_{PHL}$	—	2.0	—	160	ns
			4.5	—	32	
			6.0	—	27	
Maximum clock frequency	$f_{MAX}$	—	2.0	5	—	MHz
			4.5	25	—	
			6.0	29	—	



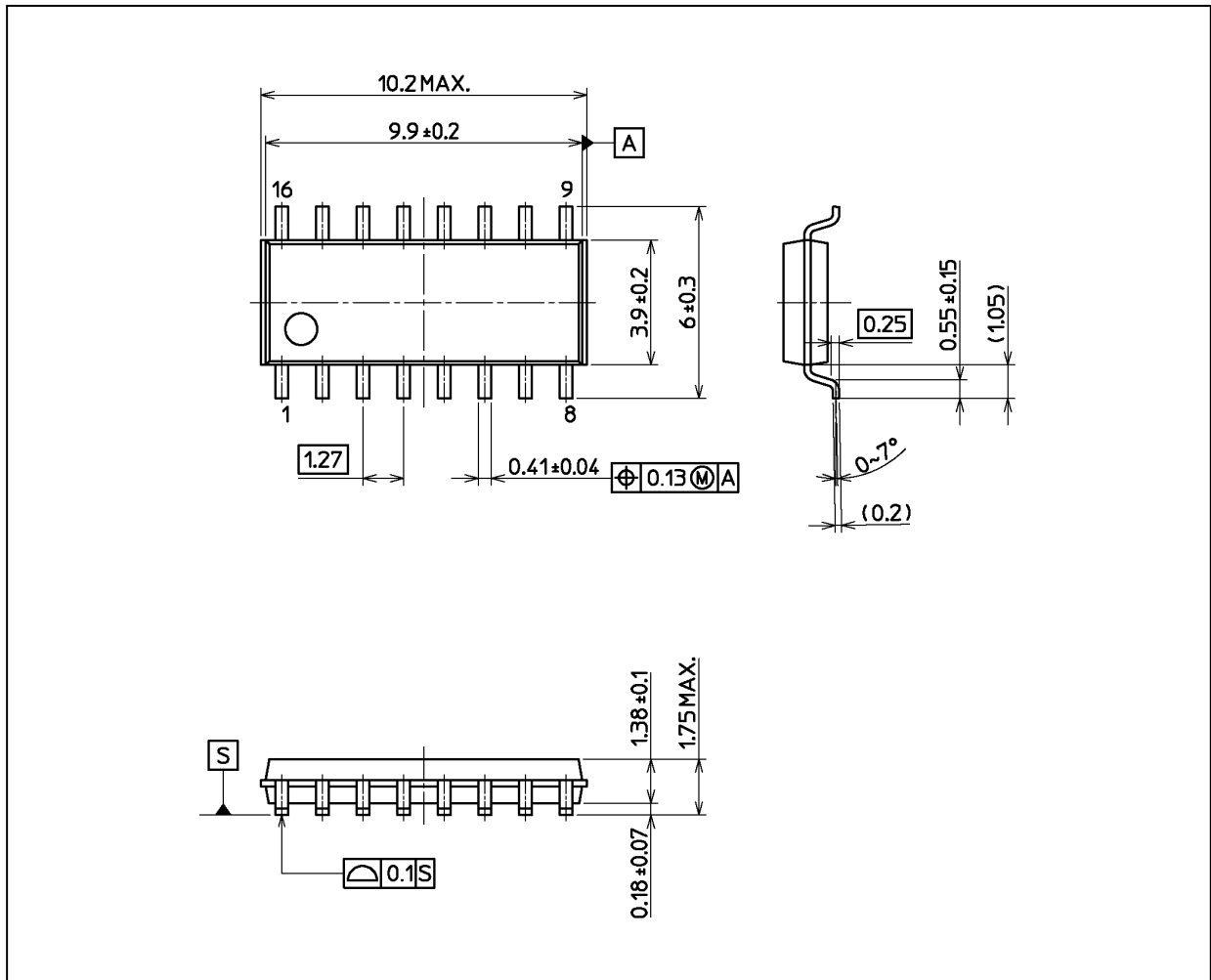
**12.10. AC Characteristics**

(Unless otherwise specified,  $C_L = 50 \text{ pF}$ ,  $T_a = -40 \text{ to } 125 \text{ }^\circ\text{C}$ , Input:  $t_r = t_f = 6 \text{ ns}$ )

Characteristics	Symbol	Test Condition	$V_{CC}$ (V)	Min	Max	Unit
Output transition time	$t_{TLH}, t_{THL}$	—	2.0	—	110	ns
			4.5	—	22	
			6.0	—	19	
Propagation delay time (CK-Q, $\bar{Q}$ )	$t_{PLH}, t_{PHL}$	—	2.0	—	210	ns
			4.5	—	42	
			6.0	—	36	
Propagation delay time (CLR-Q, $\bar{Q}$ )	$t_{PLH}, t_{PHL}$	—	2.0	—	190	ns
			4.5	—	38	
			6.0	—	32	
Maximum clock frequency	$f_{MAX}$	—	2.0	4	—	MHz
			4.5	20	—	
			6.0	24	—	

Package Dimensions

Unit: mm



Weight: 0.15 g (typ.)

Package Name(s)
Nickname: SOIC16

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