

TPCP8405

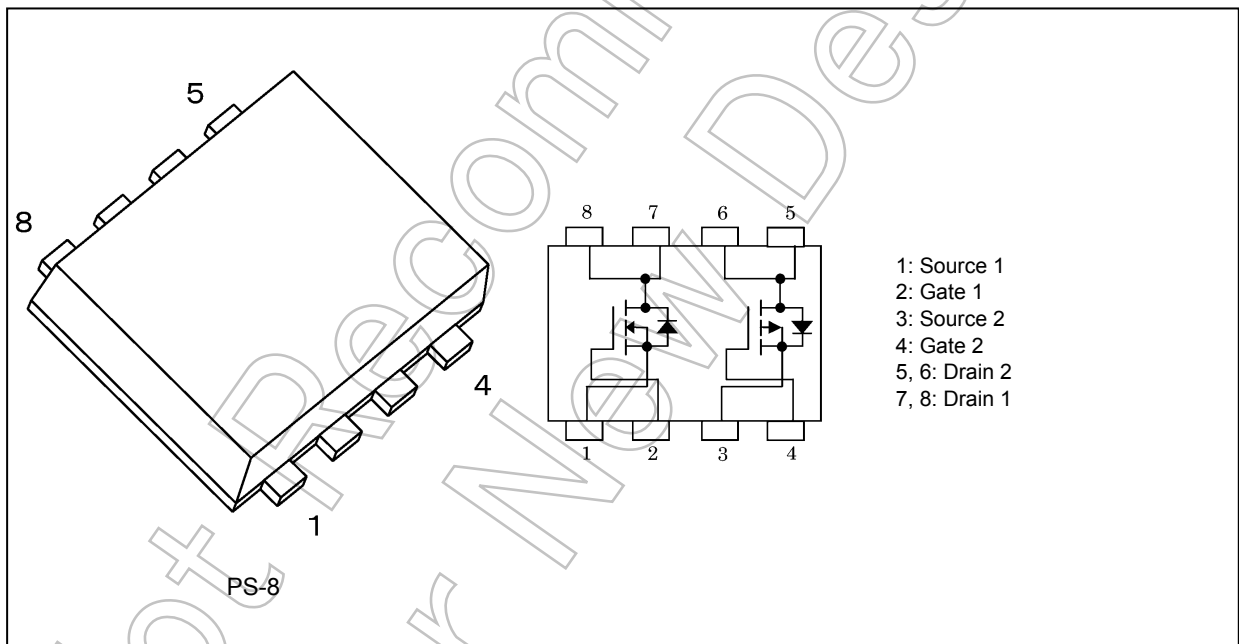
1. Applications

- Cell Phones
- Motor Drivers

2. Features

- (1) Low drain-source on-resistance
 P-channel $R_{DS(ON)} = 24 \text{ m}\Omega$ (typ.) ($V_{GS} = -10 \text{ V}$),
 N-channel $R_{DS(ON)} = 20 \text{ m}\Omega$ (typ.) ($V_{GS} = 10 \text{ V}$)
- (2) Low leakage current
 P-channel $I_{DSS} = -10 \text{ }\mu\text{A}$ ($V_{DS} = -30 \text{ V}$),
 N-channel $I_{DSS} = 10 \text{ }\mu\text{A}$ ($V_{DS} = 30 \text{ V}$)
- (3) Enhancement mode
 P-channel $V_{th} = -0.8$ to -2.0 V ($V_{DS} = -10 \text{ V}$, $I_D = -0.1 \text{ mA}$),
 N-channel $V_{th} = 1.3$ to 2.3 V ($V_{DS} = 10 \text{ V}$, $I_D = 0.1 \text{ mA}$)

3. Packaging and Internal Circuit



Start of commercial production
2009-11

4. Absolute Maximum Ratings (Note) ($T_a = 25^\circ\text{C}$ unless otherwise specified)

Characteristics	P/N	Symbol	Rating	Unit
Drain-source voltage	P-ch	V_{DSS}	-30	V
	N-ch		30	
Drain-gate voltage ($R_{GS} = 20\text{ k}\Omega$)	P-ch	V_{DGR}	-30	V
	N-ch		30	
Gate-source voltage	P-ch	V_{GSS}	± 20	V
	N-ch		± 20	
Drain current (DC) (Note 1)	P-ch	I_D	-6	A
	N-ch		6.5	
Drain current (pulsed) (Note 1)	P-ch	I_{DP}	-24	A
	N-ch		26	
Power dissipation (single operation) ($t = 5\text{ s}$) (Note 2), (Note 4)	P-ch	$P_{D(1)}$	1.48	W
	N-ch		1.48	
Power dissipation (per device for dual operation) ($t = 5\text{ s}$) (Note 2), (Note 5)	P-ch	$P_{D(2)}$	1.23	W
	N-ch		1.23	
Power dissipation (single operation) ($t = 5\text{ s}$) (Note 3), (Note 4)	P-ch	$P_{D(1)}$	0.58	W
	N-ch		0.58	
Power dissipation (per device for dual operation) ($t = 5\text{ s}$) (Note 3), (Note 5)	P-ch	$P_{D(2)}$	0.36	W
	N-ch		0.36	
Single-pulse avalanche energy (Note 6)	P-ch	E_{AS}	9.36	mJ
	N-ch		10.9	
Avalanche current	P-ch	I_{AR}	-6	A
	N-ch		6.5	
Channel temperature	P-ch	T_{ch}	150	$^\circ\text{C}$
	N-ch		150	
Storage temperature	P-ch	T_{stg}	-55 to 150	$^\circ\text{C}$
	N-ch		-55 to 150	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

5. Thermal Characteristics

Characteristics	Symbol	Max	Unit
Channel-to-ambient thermal resistance (single operation) (t = 5 s) (Note 2), (Note 4)	$R_{th(ch-a)(1)}$	84.5	°C/W
Channel-to-ambient thermal resistance (per device for dual operation) (t = 5 s) (Note 2), (Note 5)	$R_{th(ch-a)(2)}$	101.6	
Channel-to-ambient thermal resistance (single operation) (t = 5 s) (Note 3), (Note 4)	$R_{th(ch-a)(1)}$	215.5	
Channel-to-ambient thermal resistance (per device for dual operation) (t = 5 s) (Note 3), (Note 5)	$R_{th(ch-a)(2)}$	347.2	

Note 1: Ensure that the channel temperature does not exceed 150°C.

Note 2: Device mounted on a glass-epoxy board (a), Figure 5.1

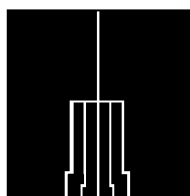
Note 3: Device mounted on a glass-epoxy board (b), Figure 5.2

Note 4: Power dissipation and thermal resistance values per device with the other device being off (During single operation, power is supplied to only one of the two devices.)

Note 5: Power dissipation and thermal resistance values per device for dual operation (During dual operation, power is evenly supplied to both devices.)

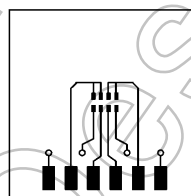
Note 6: P channel: $V_{DD} = -24\text{ V}$, $T_{ch} = 25^\circ\text{C}$ (initial), $L = 0.2\text{ mH}$, $R_G = 25\ \Omega$, $I_{AR} = -6\text{ A}$

N channel: $V_{DD} = 24\text{ V}$, $T_{ch} = 25^\circ\text{C}$ (initial), $L = 0.2\text{ mH}$, $R_G = 25\ \Omega$, $I_{AR} = 6.5\text{ A}$



FR-4
25.4 × 25.4 × 0.8
(Unit: mm)

Fig. 5.1 Device Mounted on a Glass-Epoxy Board (a)



FR-4
25.4 × 25.4 × 0.8
(Unit: mm)

Fig. 5.2 Device Mounted on a Glass-Epoxy Board (b)

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.

6. Electrical Characteristics

6.1. Static Characteristics (T_a = 25°C unless otherwise specified)

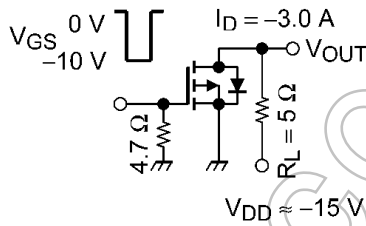
Characteristics	P/N	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	P-ch	I _{GSS}	V _{GS} = ±20 V, V _{DS} = 0 V	—	—	±0.1	μA
	N-ch		V _{GS} = ±20 V, V _{DS} = 0 V	—	—	±0.1	
Drain cut-off current	P-ch	I _{DSS}	V _{DS} = -30 V, V _{GS} = 0 V	—	—	-10	μA
	N-ch		V _{DS} = 30 V, V _{GS} = 0 V	—	—	10	
Drain-source breakdown voltage	P-ch	V _{(BR)DSS}	I _D = -10 mA, V _{GS} = 0 V	-30	—	—	V
	N-ch		I _D = 10 mA, V _{GS} = 0 V	30	—	—	
Drain-source breakdown voltage (Note 7)	P-ch	V _{(BR)DSX}	I _D = -10 mA, V _{GS} = 10 V	-21	—	—	V
	N-ch		I _D = 10 mA, V _{GS} = -20 V	15	—	—	
Gate threshold voltage	P-ch	V _{th}	V _{DS} = -10 V, I _D = -0.1 mA	-0.8	—	-2.0	V
	N-ch		V _{DS} = 10 V, I _D = 0.1 mA	1.3	—	2.3	
Drain-source on-resistance	P-ch	R _{DS(ON)}	V _{GS} = -4.5 V, I _D = -3 A	—	32	42	mΩ
			V _{GS} = -10 V, I _D = -3 A	—	24	31.3	
	N-ch		V _{GS} = 4.5 V, I _D = 3.3 A	—	22	29	
			V _{GS} = 10 V, I _D = 3.3 A	—	20	26	

Note 7: If a reverse bias is applied between gate and source, this device enters V_{(BR)DSX} mode. Note that the drain-source breakdown voltage is lowered in this mode.

Not Recommended for New Design

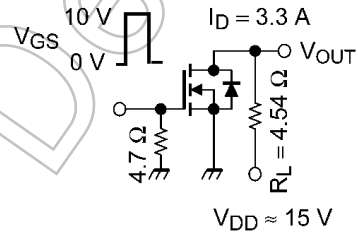
6.2. Dynamic Characteristics ($T_a = 25^\circ\text{C}$ unless otherwise specified)

Characteristics	P/N	Symbol	Test Condition	Min	Typ.	Max	Unit
Input capacitance	P-ch	C_{iss}	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V},$ $f = 1\text{ MHz}$	—	1075	—	pF
	N-ch		$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V},$ $f = 1\text{ MHz}$	—	830	—	
Reverse transfer capacitance	P-ch	C_{rss}	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V},$ $f = 1\text{ MHz}$	—	190	—	pF
	N-ch		$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V},$ $f = 1\text{ MHz}$	—	53	—	
Output capacitance	P-ch	C_{oss}	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V},$ $f = 1\text{ MHz}$	—	234	—	pF
	N-ch		$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V},$ $f = 1\text{ MHz}$	—	177	—	
Switching time (rise time)	P-ch	t_r	See Figure 6.2.1.	—	7.3	—	ns
	N-ch		See Figure 6.2.2.	—	4.1	—	
Switching time (turn-on time)	P-ch	t_{on}	See Figure 6.2.1.	—	13.6	—	ns
	N-ch		See Figure 6.2.2.	—	10.8	—	
Switching time (fall time)	P-ch	t_f	See Figure 6.2.1.	—	42	—	ns
	N-ch		See Figure 6.2.2.	—	11	—	
Switching time (turn-off time)	P-ch	t_{off}	See Figure 6.2.1.	—	136	—	ns
	N-ch		See Figure 6.2.2.	—	31	—	



Duty $\leq 1\%$, $t_w = 10\ \mu\text{s}$

Fig. 6.2.1 Switching Time Test Circuit (P-ch)



Duty $\leq 1\%$, $t_w = 10\ \mu\text{s}$

Fig. 6.2.2 Switching Time Test Circuit (N-ch)

6.3. Gate Charge Characteristics ($T_a = 25^\circ\text{C}$ unless otherwise specified)

Characteristics	P/N	Symbol	Test Condition	Min	Typ.	Max	Unit
Total gate charge (gate-source plus gate-drain)	P-ch	Q_g	$V_{DD} \approx -24\text{ V}, V_{GS} = -10\text{ V},$ $I_D = -6\text{ A}$	—	24.1	—	nC
	N-ch		$V_{DD} \approx 24\text{ V}, V_{GS} = 10\text{ V},$ $I_D = 6.5\text{ A}$	—	13.8	—	
Gate-source charge 1	P-ch	Q_{gs1}	$V_{DD} \approx -24\text{ V}, V_{GS} = -10\text{ V},$ $I_D = -6\text{ A}$	—	3.3	—	nC
	N-ch		$V_{DD} \approx 24\text{ V}, V_{GS} = 10\text{ V},$ $I_D = 6.5\text{ A}$	—	3.0	—	
Gate-drain charge	P-ch	Q_{gd}	$V_{DD} \approx -24\text{ V}, V_{GS} = -10\text{ V},$ $I_D = -6\text{ A}$	—	5.6	—	nC
	N-ch		$V_{DD} \approx 24\text{ V}, V_{GS} = 10\text{ V},$ $I_D = 6.5\text{ A}$	—	2.3	—	

6.4. Source-Drain Characteristics ($T_a = 25^\circ\text{C}$ unless otherwise specified)

Characteristics	P/N	Symbol	Test Condition	Min	Typ.	Max	Unit
Reverse drain current (pulsed) (Note 8)	P-ch	I_{DRP}	—	—	—	-24	A
	N-ch			—	—	26	
Diode forward voltage	P-ch	V_{DSF}	$I_{DR} = -6\text{ A}, V_{GS} = 0\text{ V}$	—	—	1.2	V
	N-ch		$I_{DR} = 6.5\text{ A}, V_{GS} = 0\text{ V}$	—	—	-1.2	

Note 8: Ensure that the channel temperature does not exceed 150°C .

7. Marking

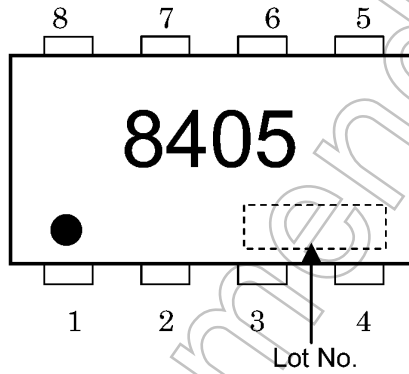


Fig. 7.1 Marking

Not Recommended for New Design

8. Characteristics Curves (Note)

8.1. P-Channel MOSFET

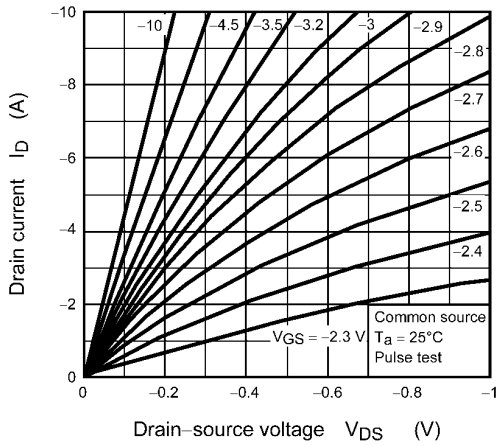


Fig. 8.1.1 ID - VDS

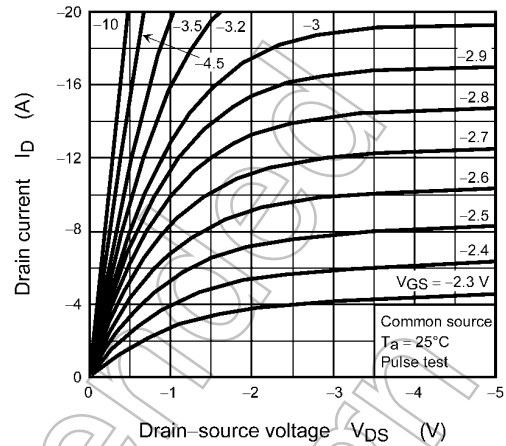


Fig. 8.1.2 ID - VDS

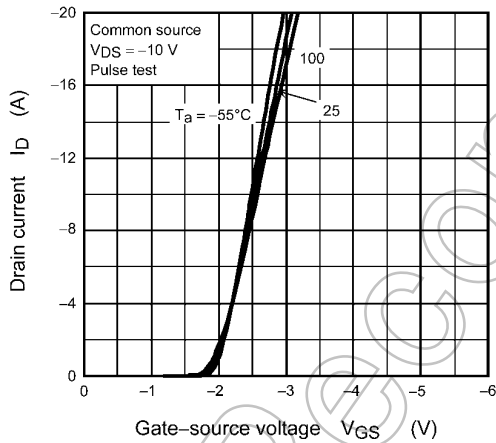


Fig. 8.1.3 ID - VGS

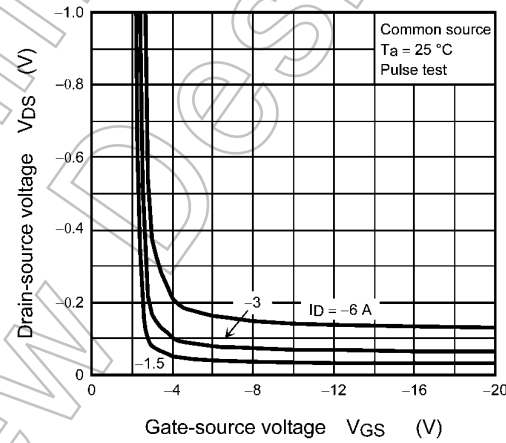


Fig. 8.1.4 VDS - VGS

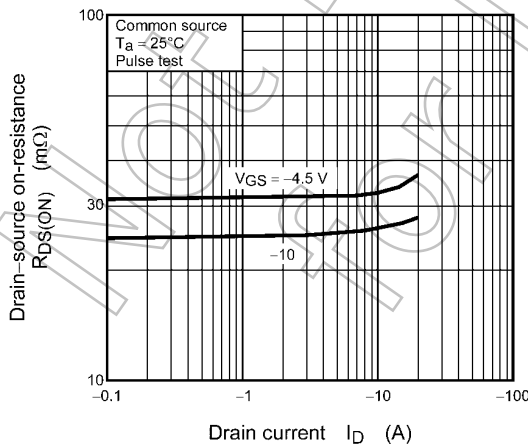


Fig. 8.1.5 RDS(ON) - ID

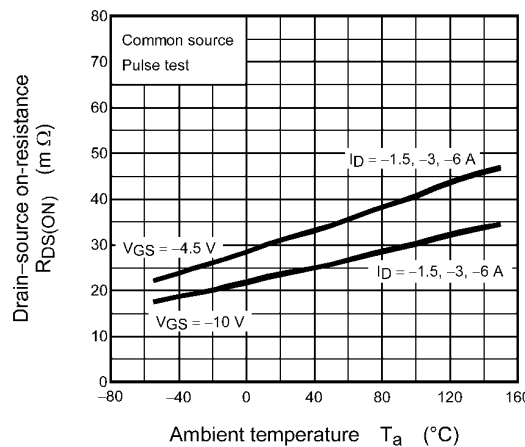


Fig. 8.1.6 RDS(ON) - Ta

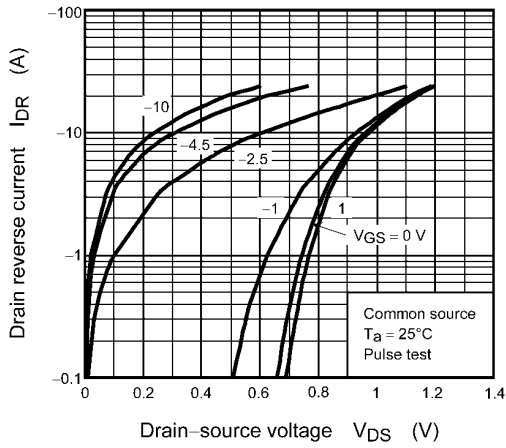


Fig. 8.1.7 $I_{DR} - V_{DS}$

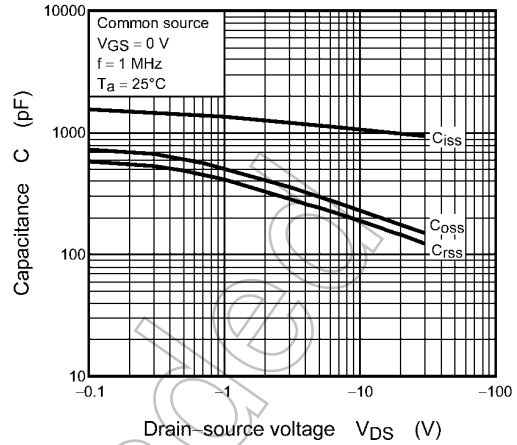


Fig. 8.1.8 Capacitance - V_{DS}

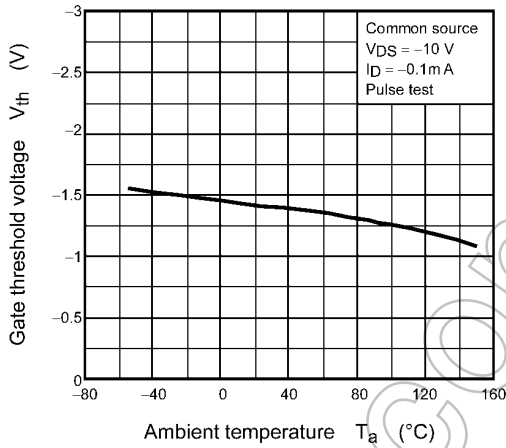


Fig. 8.1.9 $V_{th} - T_a$

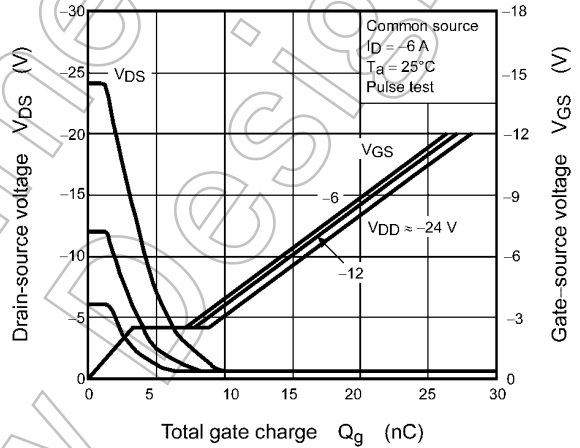


Fig. 8.1.10 Dynamic Input/Output Characteristics

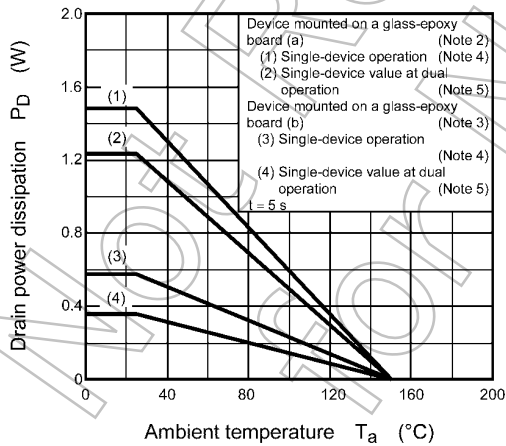


Fig. 8.1.11 $P_D - T_a$
 (Guaranteed Maximum)

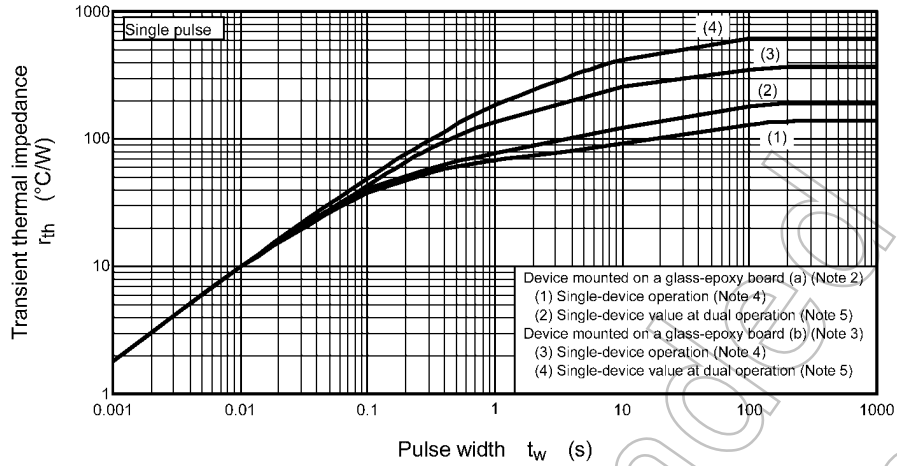


Fig. 8.1.12 $r_{th} - t_w$
(Guaranteed Maximum)

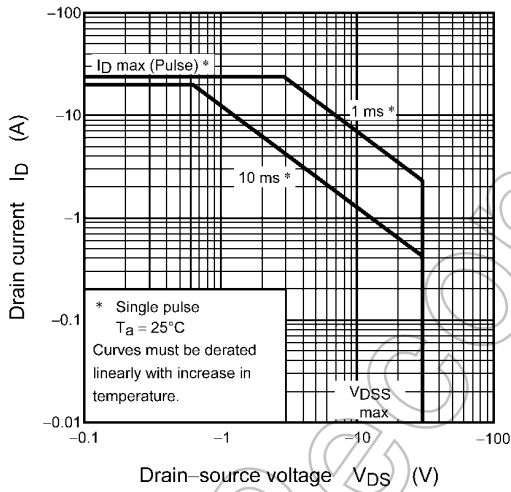


Fig. 8.1.13 Safe Operating Area
(Guaranteed Maximum)

8.2. N-Channel MOSFET

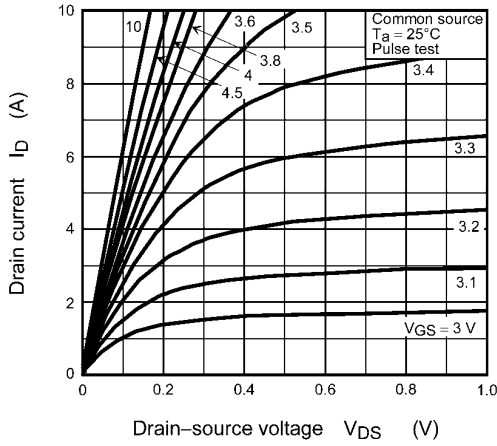


Fig. 8.2.1 $I_D - V_{DS}$

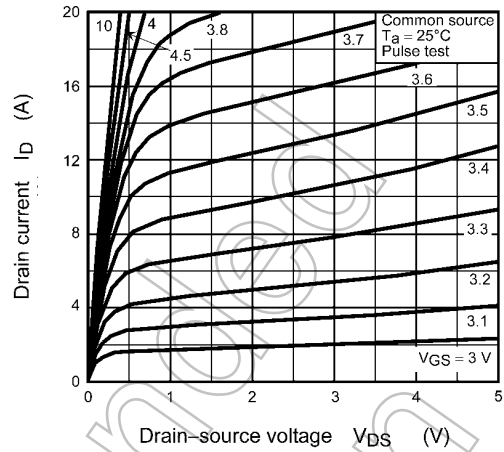


Fig. 8.2.2 $I_D - V_{DS}$

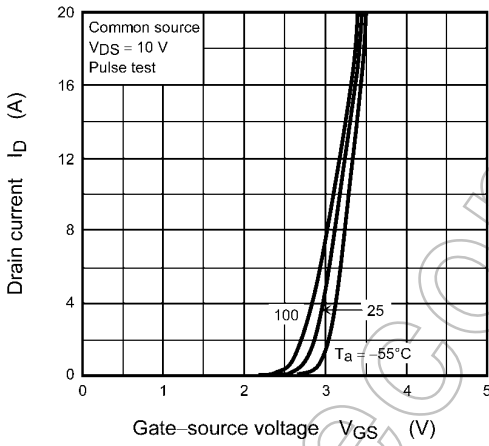


Fig. 8.2.3 $I_D - V_{GS}$

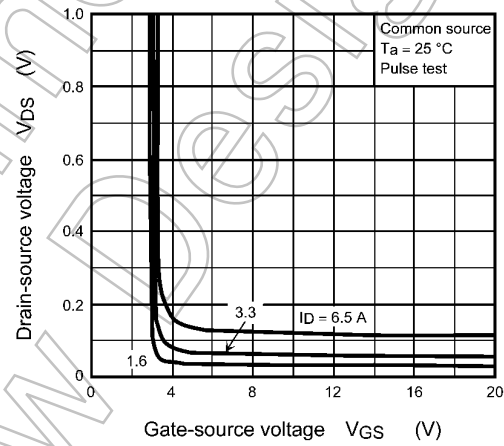


Fig. 8.2.4 $V_{DS} - V_{GS}$

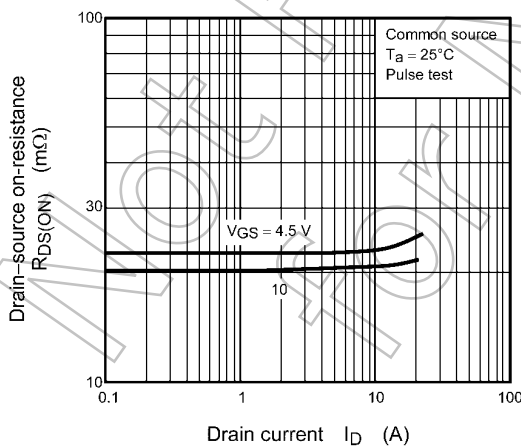


Fig. 8.2.5 $R_{DS(ON)} - I_D$

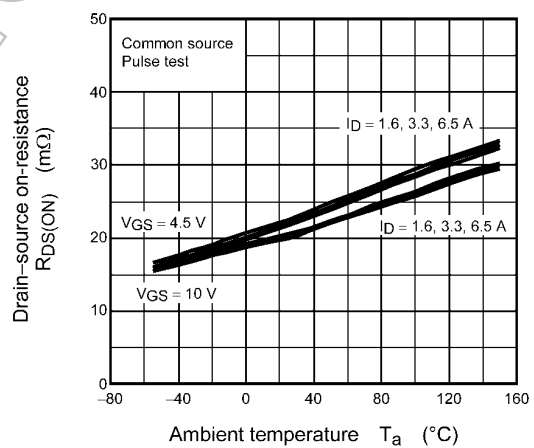


Fig. 8.2.6 $R_{DS(ON)} - T_a$

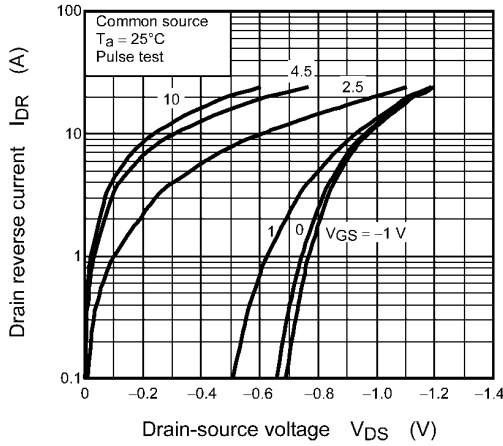


Fig. 8.2.7 $I_{DR} - V_{DS}$

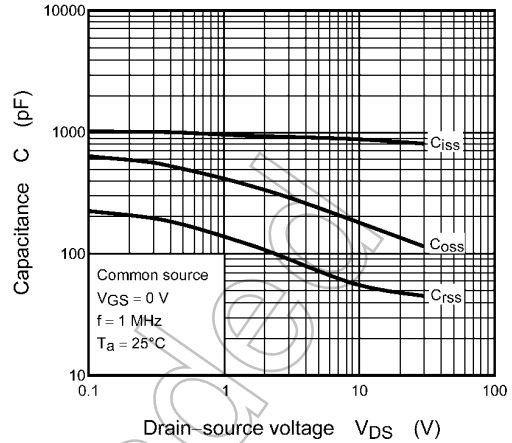


Fig. 8.2.8 Capacitance - V_{DS}

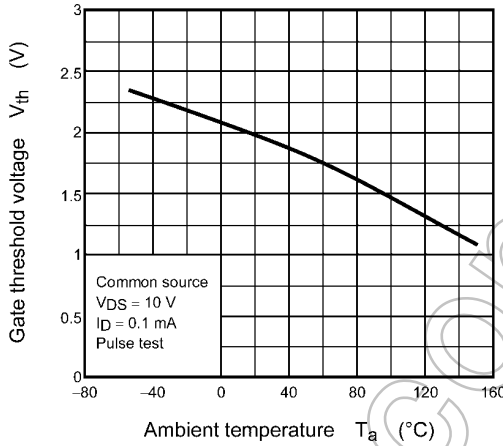


Fig. 8.2.9 $V_{th} - T_a$

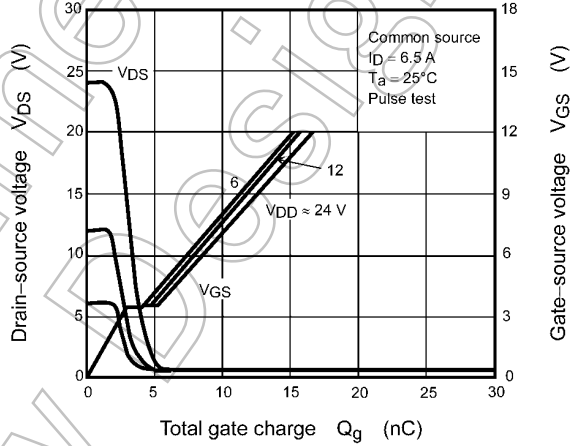


Fig. 8.2.10 Dynamic Input/Output Characteristics

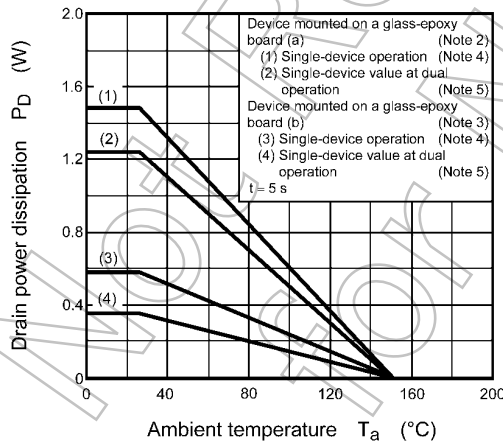


Fig. 8.2.11 $P_D - T_a$
 (Guaranteed Maximum)

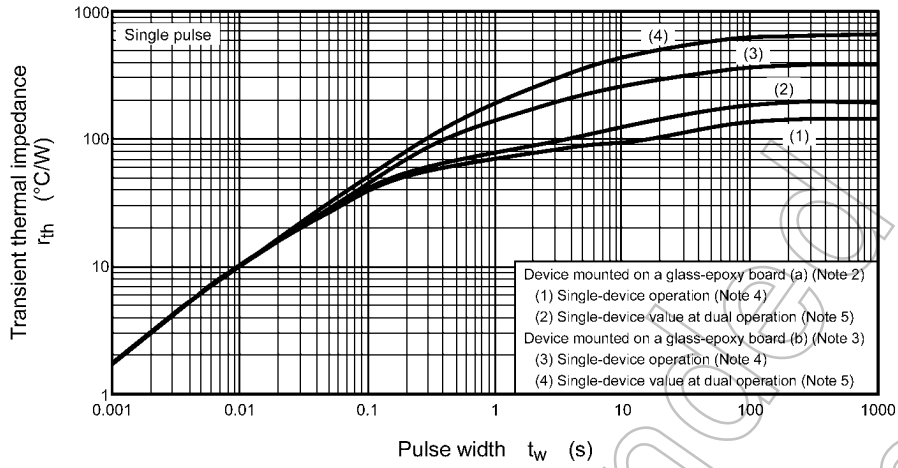


Fig. 8.2.12 $r_{th} - t_w$
(Guaranteed Maximum)

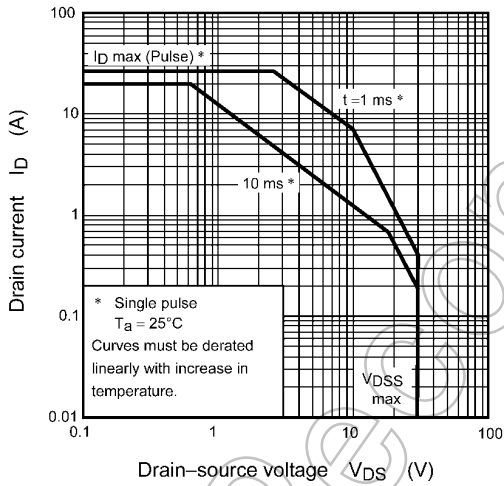
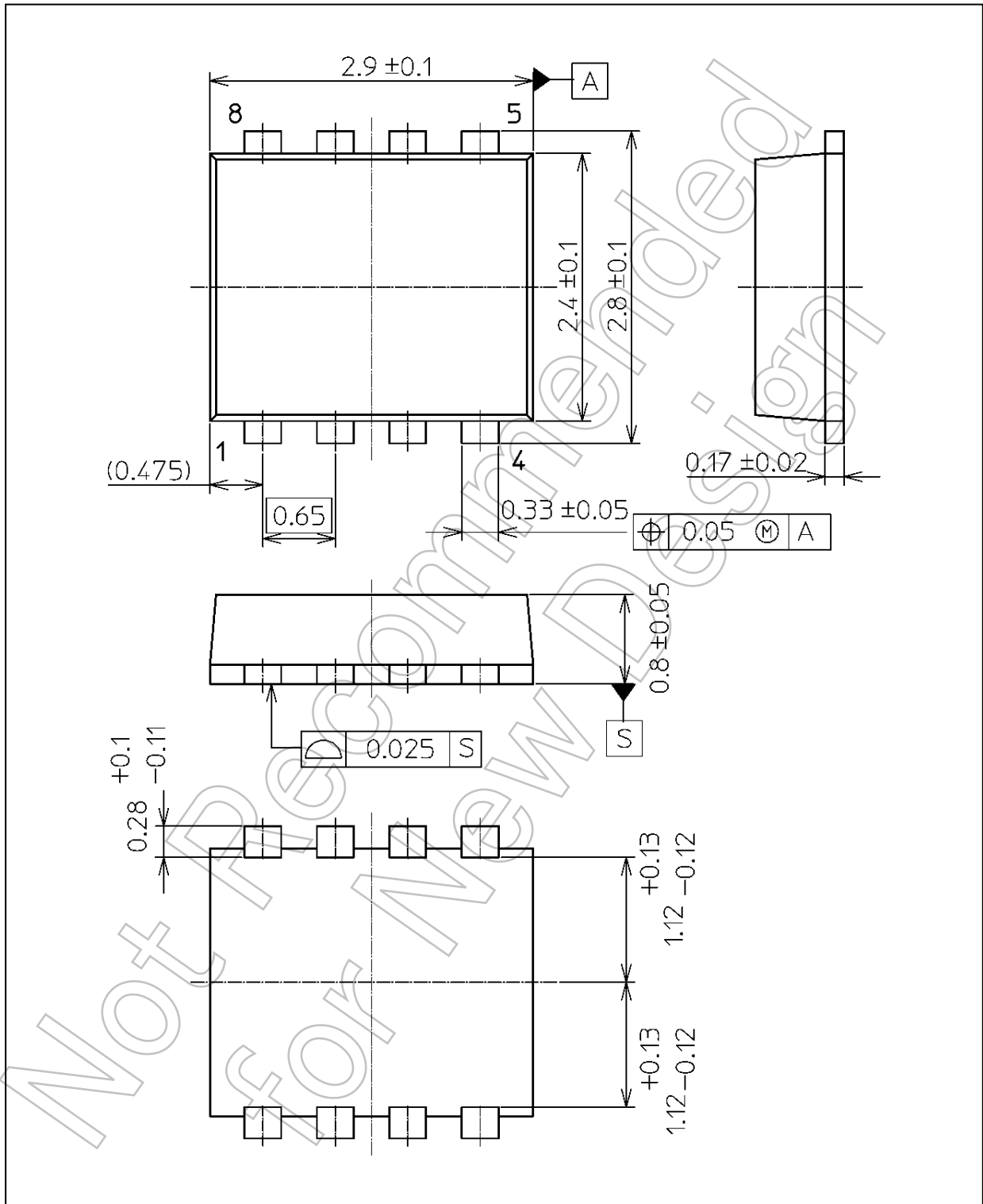


Fig. 8.2.13 Safe Operating Area
(Guaranteed Maximum)

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

Package Dimensions

Unit: mm



Weight: 0.017 g (typ.)

Package Name(s)
TOSHIBA: 2-3V1S
Nickname: PS-8

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