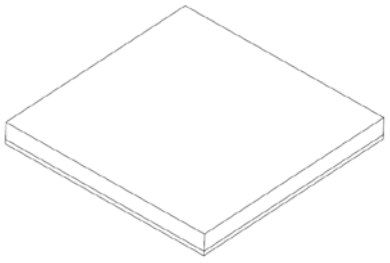
TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC90202XBG

Picture Quality Improver IC embedded the circuit for timing control signal generation

TC90202XBG has picture quality improver (Edge Enhancement, Color adjustment, Contrast adjustment, etc.) for input-digital-RGB-video-signal (6bit/8bit), and it outputs with digital-RGB-Video-signal (6bit/8bit). In addition, it supports output timing control signals for LCD panel.



P-FBGA121-1010-0.80A5

Weight : 0.23g (Typ.)

1. Features

1. Supports Panel
   WQVGA : 400x234,400x240,480x234,480x240,480x272
   WVGA : 800x480
2. System Clock frequency
   8MHz to 33.33MHz
3. Input / Output signal format
   Digital RGB signals (6bit / 8bit)
4. Picture Quality Improvement function
   <Y signal processing>
   -HVD Enhancer
   -Sharpness, LTI, Noise Canceler
   -Static Y-gamma correction
   -Dynamic Y-gamma correction
   -Contrast, Brightness
   <C signal process>
   -CTI, Noise Canceler
   -C gain correction with Y-gamma characteristic
   -Color management
   -Color saturation, Cb/Cr offset adjustment
   <RGB signal process>
   -Offset adjustment, Gain adjustment
   -RGB-gamma correction
   -Dither, FRC (Frame Rate Control)
5. Output the Timing Control Pulse for LCD panel
6. PWM signal output
7. I^2C-BUS Control
8. Package
   P-FBGA121-1010-0.80A5
9. Power Supply
   3.3V, 1.5V
10. Operating temperature
    -40°C to 85°C

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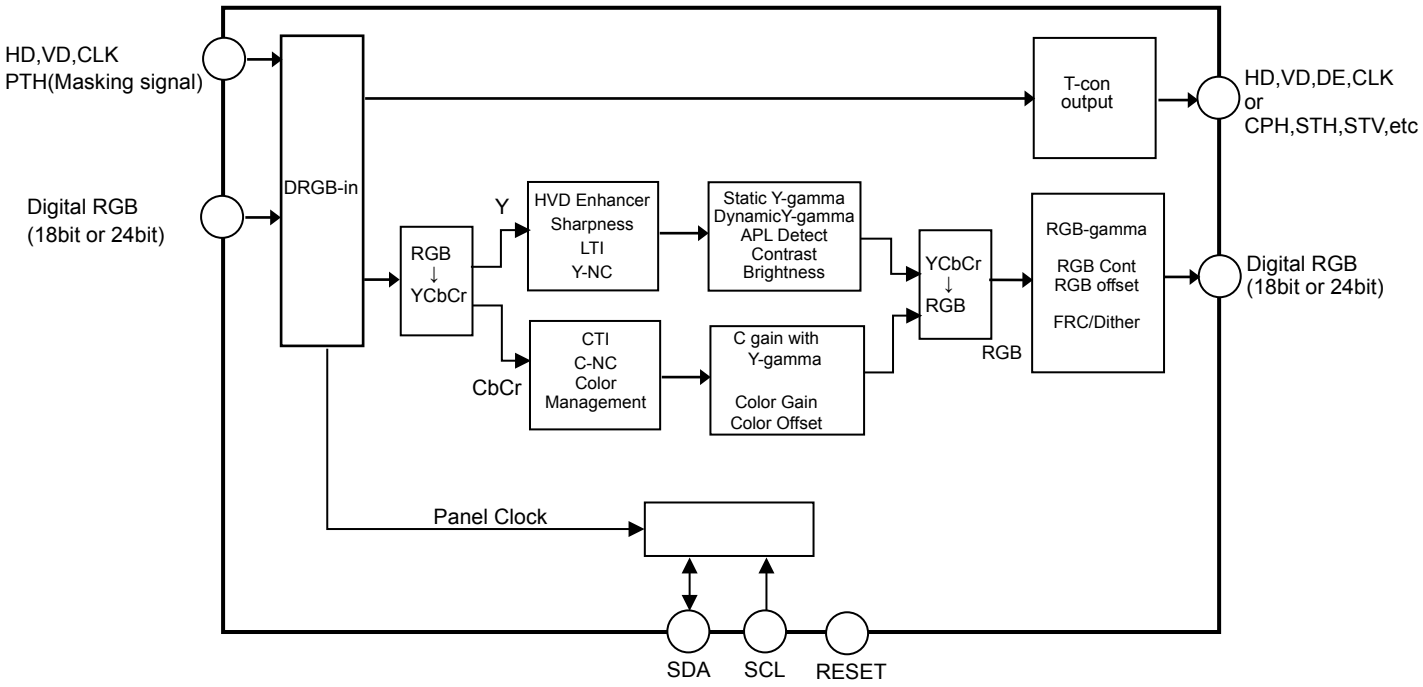
2. Block Diagram



3. Pin Assignment

Package TOP VIEW

	1	2	3	4	5	6	7	8	9	10	11	
A	A1 DGND	A2 R0OUT	A3 R2OUT	A4 VDDIO9	A5 R5OUT	A6 DVDD4	A7 G2OUT	A8 VDDIO8	A9 G7OUT	A10 B1OUT	A11 DGND	A
B	B1 R0IN	B2 DGND	B3 R1OUT	B4 R3OUT	B5 R6OUT	B6 G0OUT	B7 G3OUT	B8 G5OUT	B9 B0OUT	B10 DGND	B11 B2OUT	B
C	C1 R2IN	C2 R1IN	C3 DGND	C4 R4OUT	C5 R7OUT	C6 G1OUT	C7 G4OUT	C8 G6OUT	C9 DGND	C10 B3OUT	C11 VDDIO7	C
D	D1 VDDIO1	D2 R4IN	D3 R3IN	D4 DGND	D5 DGND	D6 DGND	D7 DGND	D8 DGND	D9 B5OUT	D10 B4OUT	D11 VDDIO6	D
E	E1 R7IN	E2 R6IN	E3 R5IN	E4 DGND	E5 DGND	E6 DGND	E7 DGND	E8 DGND	E9 B7OUT	E10 B6OUT	E11 CPHOUT	E
F	F1 DVDD1	F2 G1IN	F3 G0IN	F4 DGND	F5 DGND	F6 DGND	F7 DGND	F8 DGND	F9 STVOUT1	F10 DEOUT	F11 DVDD3	F
G	G1 G4IN	G2 G3IN	G3 G2IN	G4 DGND	G5 DGND	G6 DGND	G7 DGND	G8 DGND	G9 CPV	G10 LOAD	G11 STH	G
H	H1 VDDIO2	H2 G6IN	H3 G5IN	H4 DGND	H5 DGND	H6 DGND	H7 DGND	H8 DGND	H9 STVOUT2	H10 VLOAD	H11 VDDIO5	H
J	J1 B0IN	J2 G7IN	J3 B4IN	J4 B7IN	J5 VDIN	J6 TEST0	J7 RESET	J8 PANELSELECT	J9 DGND	J10 UD	J11 HCOM	J
K	K1 B1IN	K2 B2IN	K3 B5IN	K4 PTH	K5 HDIN	K6 TEST1	K7 SLAVESEL	K8 SDA	K9 DIMMER	K10 DGND	K11 VCOM1	K
L	L1 DGND	L2 B3IN	L3 B6IN	L4 VDDIO3	L5 CLKIN	L6 DVDD2	L7 SCL	L8 VDDIO4	L9 GOE	L10 VCOM2	L11 DGND	L
	1	2	3	4	5	6	7	8	9	10	11	

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4. Terminals Description

Pin No.	Pin Name	Pin Function	Pin Type	IO
A1	DGND	Digital GND	Power	GND
B1	R0IN	Digital RGB Input (R0) LSB	Digital IN	Input
C1	R2IN	Digital RGB Input (R2)	Digital IN	Input
D1	VDDIO1	3.3V Power Supply for I/O Block	Power	Power
E1	R7IN	Digital RGB Input (R7)	Digital IN	Input
F1	DVDD1	1.5V Power Supply for Internal Logic	Power	Power
G1	G4IN	Digital RGB Input (G4)	Digital IN	Input
H1	VDDIO2	3.3V Power Supply for I/O Block	Power	Power
J1	B0IN	Digital RGB Input (B0) LSB	Digital IN	Input
K1	B1IN	Digital RGB Input (B1)	Digital IN	Input
L1	DGND	Digital GND	Power	GND
A2	R0OUT	Digital RGB Output (R0) LSB	Digital OUT	Output
B2	DGND	Digital GND	Power	GND
C2	R1IN	Digital RGB Input (R1)	Digital IN	Input
D2	R4IN	Digital RGB Input (R4)	Digital IN	Input
E2	R6IN	Digital RGB Input (R6)	Digital IN	Input
F2	G1IN	Digital RGB Input (G1)	Digital IN	Input
G2	G3IN	Digital RGB Input (G3)	Digital IN	Input
H2	G6IN	Digital RGB Input (G6)	Digital IN	Input
J2	G7IN	Digital RGB Input (G7) MSB	Digital IN	Input
K2	B2IN	Digital RGB Input (B2)	Digital IN	Input
L2	B3IN	Digital RGB Input (B3)	Digital IN	Input
A3	R2OUT	Digital RGB Output (R2)	Digital OUT	Output
B3	R1OUT	Digital RGB Output (R1)	Digital OUT	Output
C3	DGND	Digital GND	Power	GND
D3	R3IN	Digital RGB Input (R3)	Digital IN	Input
E3	R5IN	Digital RGB Input (R5)	Digital IN	Input
F3	G0IN	Digital RGB Input (G0) LSB	Digital IN	Input
G3	G2IN	Digital RGB Input (G2)	Digital IN	Input
H3	G5IN	Digital RGB Input (G5)	Digital IN	Input
J3	B4IN	Digital RGB Input (B4)	Digital IN	Input
K3	B5IN	Digital RGB Input (B5)	Digital IN	Input
L3	B6IN	Digital RGB Input (B6)	Digital IN	Input
A4	VDDIO9	3.3V Power Supply for I/O Block	Power	Power
B4	R3OUT	Digital RGB Output (R3)	Digital OUT	Output
C4	R4OUT	Digital RGB Output (R4)	Digital OUT	Output
D4	DGND	Digital GND	Power	GND
E4	DGND			
F4	DGND			
G4	DGND			
H4	DGND			
J4	B7IN	Digital RGB Input (B7) MSB	Digital IN	Input
K4	PTH	Timing pulse for picture process through	Digital IN	Input
L4	VDDIO3	3.3V Power Supply for I/O Block	Power	Power
A5	R5OUT	Digital RGB Output (R5)	Digital OUT	Output
B5	R6OUT	Digital RGB Output (R6)	Digital OUT	Output
C5	R7OUT	Digital RGB Output (R7) MSB	Digital OUT	Output
D5	DGND	Digital GND	Power	GND
E5	DGND			
F5	DGND			
G5	DGND			
H5	DGND			
J5	VDIN	V Sync Input	Digital IN	Input
K5	HDIN	H Sync Input	Digital IN	Input

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Pin No	Pin Name	Pin Function	Pin Type	IO
L5	CLKIN	System Clock Input	Digital IN	Input
A6	DVDD4	1.5V Power Supply for Internal Logic	Power	Power
B6	G0OUT	Digital RGB Output (G0) LSB	Digital OUT	Output
C6	G1OUT	Digital RGB Output (G1)	Digital OUT	Output
D6	DGND	Digital GND	Power	GND
E6	DGND			
F6	DGND			
G6	DGND			
H6	DGND			
J6	TEST0	Test Input 0 (connect to GND)	TEST	Input
K6	TEST1	Test Input 1 (connect to GND)	TEST	Input
L6	DVDD2	1.5V Power Supply for Internal Logic	Power	Power
A7	G2OUT	Digital RGB Output (G2)	Digital OUT	Output
B7	G3OUT	Digital RGB Output (G3)	Digital OUT	Output
C7	G4OUT	Digital RGB Output (G4)	Digital OUT	Output
D7	DGND	Digital GND	Power	GND
E7	DGND			
F7	DGND			
G7	DGND			
H7	DGND			
J7	RESET	Reset signal Input (Low : Reset, High: Normal)	RESET	Input
K7	SLAVESEL	Set up I^2C-BUS Slave Address	I^2C	Input
L7	SCL	SCL Input for I^2C-BUS	I^2C	Input
A8	VDDIO8	3.3V Power Supply for I/O Block	Power	Power
B8	G5OUT	Digital RGB Output (G5)	Digital OUT	Output
C8	G6OUT	Digital RGB Output (G6)	Digital OUT	Output
D8	DGND	Digital GND	Power	GND
E8	DGND			
F8	DGND			
G8	DGND			
H8	DGND			
J8	PANEL SELECT	Setup polarity of GOE (GOE:LCD Control signal)	LCD control	Input
K8	SDA	SDA signal for I^2C-BUS	I^2C	I/O
L8	VDDIO4	3.3V Power Supply for I/O Block	Power	Power
A9	G7OUT	Digital RGB Output (G7) MSB	Digital OUT	Output
B9	B0OUT	Digital RGB Output (B0) LSB	Digital OUT	Output
C9	DGND	Digital GND	Power	GND
D9	B5OUT	Digital RGB Output (B5)	Digital OUT	Output
E9	B7OUT	Digital RGB Output (B7) MSB	Digital OUT	Output
F9	STVOUT1	Control signal for LCD (Vertical start pulse 1)	LCD control	Output
G9	CPV	Control signal for LCD (Gate clock signal)	LCD control	Output
H9	STVOUT2	Control signal for LCD (Vertical start pulse 2)	LCD control	Output
J9	DGND	Digital GND	Power	GND
K9	DIMMER	PWM signal Output	PWM	Output
L9	GOE	Control signal for LCD (Reset signal output for LCD panel)	LCD control	Output
A10	B1OUT	Digital RGB Output (B1)	Digital OUT	Output
B10	DGND	Digital GND	Power	GND
C10	B3OUT	Digital RGB Output (B3)	Digital OUT	Output
D10	B4OUT	Digital RGB Output (B4)	Digital OUT	Output
E10	B6OUT	Digital RGB Output (B6)	Digital OUT	Output
F10	DEOUT	Control signal for LCD (Data enable signal)	LCD control	Output
G10	LOAD	Control signal for LCD (Latch(writing) pulse for the H direction for source)	Control signal	Output
H10	VLOAD	Control signal for LCD (Latch(writing) signal for Gate)	LCD control	Output
J10	UD	Control signal for LCD (Vertical panel control)	LCD control	Output
K10	DGND	Digital GND	Power	GND

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Pin No	Pin Name	Pin Function	Pin Type	IO
L10	VCOM2	Control signal for LCD (Common Electrode output)	LCD control	Output
A11	DGND	Digital GND	Power	GND
B11	B2OUT	Digital RGB Output (B2)	Digital OUT	Output
C11	VDDIO7	3.3V Power Supply for I/O Block	Power	Power
D11	VDDIO6	3.3V Power Supply for I/O Block	Power	Power
E11	CPHOUT	Control signal for LCD (Source clock signal)	LCD control	Output
F11	DVDD3	1.5V Power Supply for Internal Logic	Power	Power
G11	STH	Control signal for LCD (Start pulse signal for source)	LCD control	Output
H11	VDDIO5	3.3V Power Supply for I/O Block	Power	Power
J11	HCOM	Control signal for LCD (Data invert signal)	LCD control	Output
K11	VCOM1	Control signal for LCD (Common Electrode output)	LCD control	Output
L11	DGND	Digital GND	Power	GND

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5. Functional Description

5.1 Input video signal

Input video signal : RGB (6bit/8bit)
Timing signal : HD(Horizontal sync), VD(Vertical sync), CLK
Support resolution : WQVGA (400x234, 400x240. 480x234, 480x240, 480x272), WVGA (800x480)

Notice
1) The polarity of HD input and VD input signal must be same. (Selectable Negative / Positive)
It is setup via the register SYNCIN at Sub Address 0x05 of Segment Address 0x00.
2) The period of front porch (between the end of active picture and start edge of sync signal) must keep the following specification.
Horizontal : it must be bigger than 4 clocks.
Vertical : it must be bigger than 2 lines.
2) The system clock of this LSI, it must be provided by external front block with RGB signal due to not include clock generation circuit in TC90202XBG..

5.2 Control signals for LCD panel

The Control signals for LCD use the leading edge of output's active area as a reference phase.
It has some limitations by the phase of leading edge of inputted sync signal.

< Horizontal >
The horizontal start phase for panel control signals is limited to width of horizontal back porch for input signal.
Maximum Output horizontal back porch = input back porch -1 [ck]

< Vertical >
The vertical start phase for panel control signals is limited to width of horizontal back-porch for input signal.
Maximum Output vertical back porch = input back porch +2 [line]

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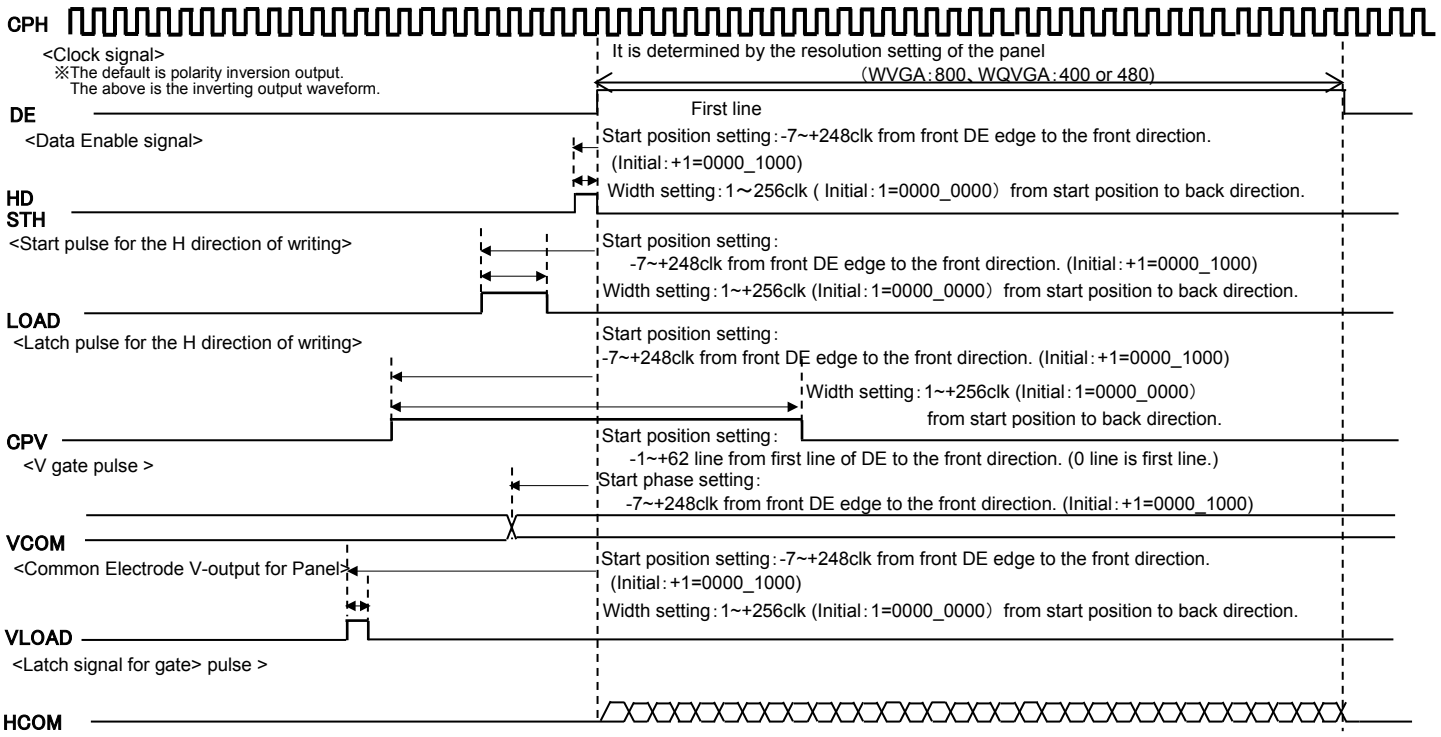
<Horizontal>



Polarity of HCOM inverts at every dots, only on active video period.
In addition, polarity of HCOM at first dot of line inverts at every lines.
Polarity of HCOM at first dot of first line of the vertical inverts at every the vertical.
At high output, Data output is inverted. (ex. HCOM=L:0011_1001,HCOM=H:1100_0110)

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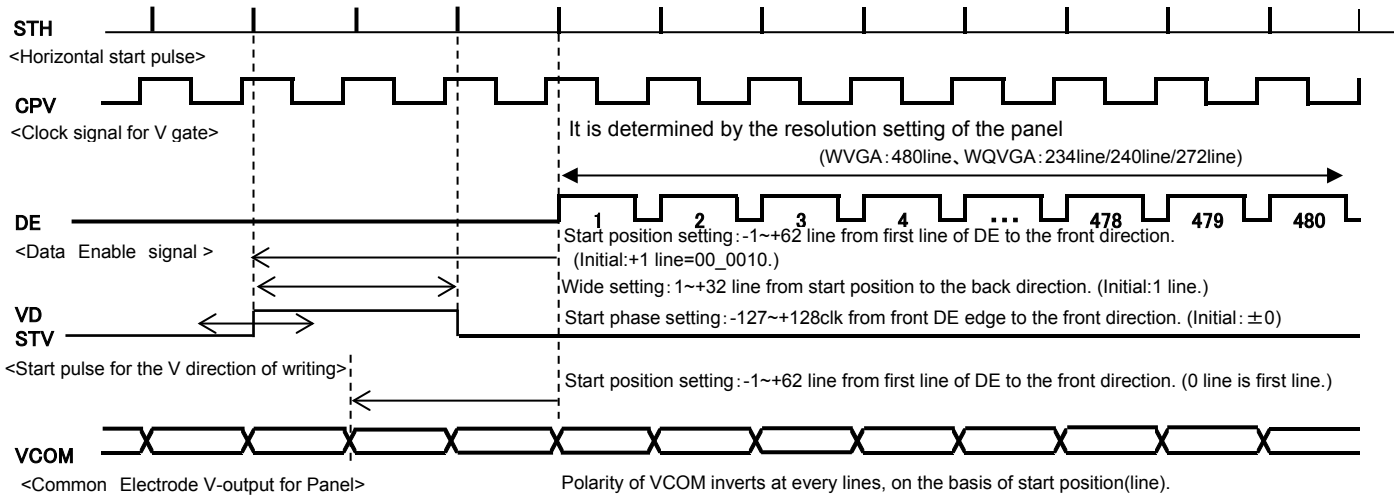
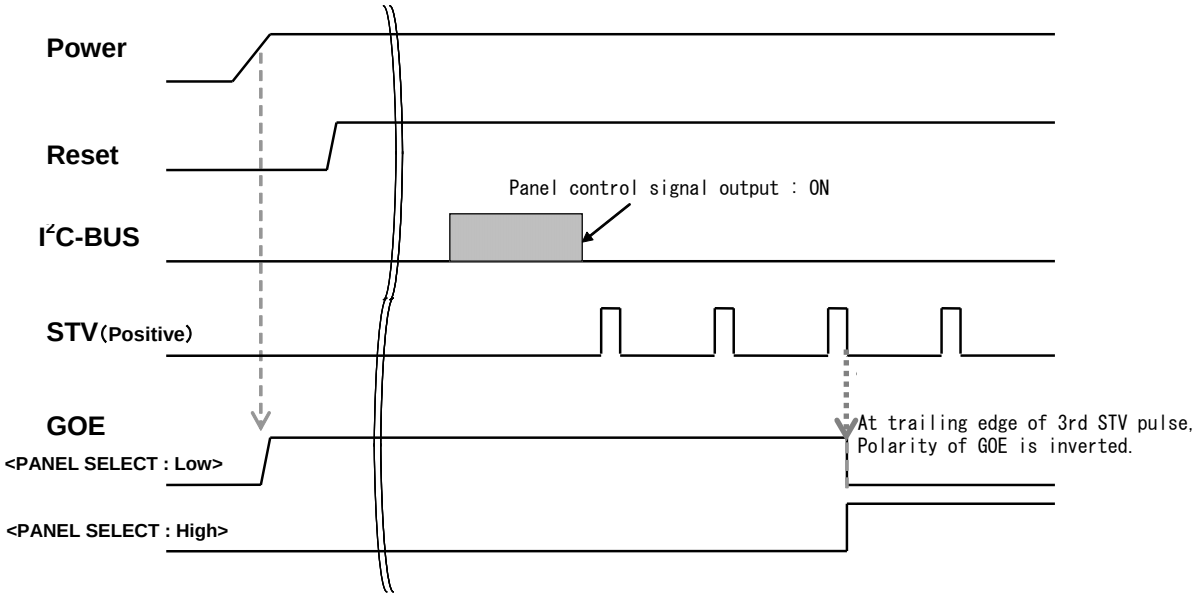
<Vertical>



<Power on and start sequence>



5.3 Picture Quality Improver

The RGB signal is converted to YCbCr format to process of picture quality improvement.

5.3.1 Masking function for Picture processing

It can through the picture quality improvement function for specific area such as OSD portion.
The area of mask-in is set by external timing pulse “PTH” or register setting.
The case of using I^2C, it has limitation to setup area up to 4.

The relative picture quality improvement functions are as follows.

- HVD enhancer
- Horizontal Y enhancer (Sharpness, LTI, Y-NC)
- APL detection
- Static Y-gamma correction
- Dynamic Y-gamma correction
- Contrast
- Brightness
- Horizontal C enhancer (CTI, C-NC)
- Color management
- Color Gain
- Cb/Cr offset
- Picture RGB offset / gain correction

5.3.2 Y signal process

5.3.2.1. HVD enhancer

This function accentuates edge of luminance of horizontal, vertical and diagonal.
Additionally, it makes small edge unemphatic by coring-setting, as noise canceller function.
It also can increase effect of NC as picture is darker.

Register setting : tap of filter (horizontal, vertical and diagonal), gain, coring level, N.C. gain, limit level, coring level increased by dark

5.3.2.2. Sharpness

This function accentuates the horizontal edge of luminance.
Register setting : f0, coring level, gain

5.3.2.3. LTI

This function accentuates the horizontal slope of luminance
Register setting : f0, coring level, gain

5.3.2.4. Y-NC

This function makes small the horizontal edge of luminance unemphatic.
Register setting : f0, coring level, gain

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5.3.2.5. APL detection

This function detects the luminance level of input picture.
The detection point, It can be selected the before stage or after stage of picture process block.
The detection area for input picture, It can be set with box area via I^2C.
The detection value can be read via I^2C. It is available to use as a reference value of the PWM output function.

5.3.2.6. Static Y-gamma control

This function adjusts luminance static gamma curve.
The luminance slope gain can be selected in range of 0LSB to 127LSB, 128LSB to 255LSB, 256LSB to 511LSB, 512LSB to 767LSB, 768LSB to 895LSB and 896LSB to 1023LSB respectively. (The luminance signal is processed with 10bit resolution in this function, then "1023LSB" means top level of D-range.)
The slope gain can be set plus direction only but not minus. If slope gain is set much higher in lower luminance range, it needs to reduce the slope gain in upper range to avoid overflow. Please care about white out in light portion of picture caused by the overflow.

5.3.2.7. Dynamic Y-gamma correction

This function controls luminance gamma characteristic and offset automatically by detecting the input picture dark portion and light portion.
The limitation of detection area of input picture can be set with box area as the same as the APL detection function.

5.3.2.8. Brightness control

This function controls the setup level of picture.
Control level : -256LSB to +252LSB (default: 0LSB)
Please care about white out in light portion of picture caused by setting much higher level.

5.3.2.9. Contrast control

This function controls the gain of luminance level.
Control gain range : ×0 to ×1.992 (default : ×1.0)
Please care about white out in light portion of picture caused by setting much higher gain.

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5.3.3 C signal process

5.3.3.1. CTI

This function accentuates the horizontal edge slope of chroma.
Register setting : f0, coring level, gain

5.3.3.2. C-NC

This function makes the small horizontal edge of chroma unemphatic
Register setting : f0, coring level, gain

5.3.3.3. Color Management

This function can manage color signal of the specific color phase. It is available at selected 3 of specific color phase independently.
Register setting : center color phase, coverage of phase width, color gain
.

5.3.3.4. Skin Color Correction (fresh color)

The function accentuates skin color/
Register setting : width of color phase, width of chromaticness, gain, color phase of skin color

5.3.3.5. C gain correction with Dynamic Y-gamma correction

This function controls the color gain synchronizing with Dynamic Y-gamma correction.
The gain can be selected to control the color amplitude synchronizing with Dynamic Y-gamma
In addition, a gain decreasing function can be selected when the Dynamic Y-gamma gain get minus direction.

5.3.3.6. Color Saturation

This function sets the gain each of Cb and Cr.
Control range : ×0 to ×3.992

5.3.3.7. Cb/Cr offset adjustment

This function sets the offset level each of Cb and Cr.
Control level : -256LSB to +252LSB

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5.3.4 RGB Signal Processing

5.3.4.1. Fine-tuning RGB Contrast and Brightness.

It can fine-tune RGB contrast and brightness except the picture process masking area.

5.3.4.2. Fine-tuning RGB Contrast and Brightness at before stage of RGB-gamma function

This function is contrast and brightness adjustment at before stage of RGB-gamma correction.
It is effective for all of area on screen which includes masking area.

5.3.4.3. RGB-gamma correction

It can fine-tune for RGB-gamma curve independently.
This function is effective for all of area on screen which includes masking area.
It can set 8 inflection points with I^2C.
Relative registers : Refer to registers at Sub Address 0x20 - 0x4F of Segment Address 0x01.
The unit of these registers is 2LSB/step.

5.3.4.4. RGB signal offset adjustment at after RGB-gamma correction

This function is brightness adjustment at after stage of RGB-gamma correction.
It is effective for all of area on screen which includes masking area.

5.3.4.5. Dither/FRC

There are Dither and FRC function at RGB output stage. These are effective to reduce random noise for 6bit output range mode.

5.3.5 PWM signal output

PWM signal output is available at PIN K9 DIMMER.
The duty of PWM is set by register from 0.02% to 100% with max.12bit resolution.
If duty should be set to 0%, it needs to turn to off of PWM output.
The output frequency is limited by the panel clock inputted this LSI.
Please refer the register manual for details.
Output ON/OFF and the output reversing control are available.
It is also available to control the duty automatically referring to the value output from the dynamic Y-gamma correction of light part, dark part or the APL detection function.

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6. Absolute maximum ratings

The maximum ratings are rated values which must not be exceeded during operation, even for an instant. Exceeding the maximum rating may result in destruction, degradation or other damage to the IC and other components.

When designing applications for this IC, be sure that none of the maximum rating values will ever be exceeded.

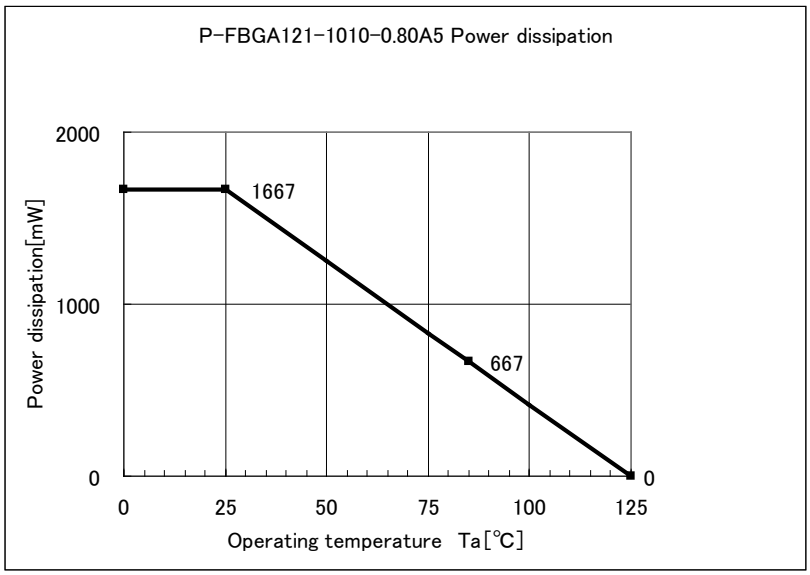
Item	Corresponding terminal	Symbol	Rating	Unit
Power voltage1 (1.5V system)	F1,A6,L6,F11	VDD1	-0.3 to VSS+2.0	V
Power voltage2 (3.3V system)	D1,H1,A4,L4,A8,L8, C11,D11,H11	VDD2	-0.3 to VSS+3.9	V
Input voltage (3.3V system)	B1,C1,E1,G1,J1,K1, C2,D2,E2,F2,G2,H2, J2,K2,L2,D3,E3,F3, G3,H3,J3,K3,L3,J4, K4,J5,K5,L5,J7,K7,J8	VIN2	-0.3 to VDD2+0.3	V
Input voltage (3.3V system, 5V withstand voltage)	L7,K8	VIN4 (Note1)	-0.3 to VSS+5.5	V
Potential difference between power pins (between 1.5V system power pins)	-	ΔVDG1 (Note2)	0.3	V
Potential difference between power pins (between 3.3V system power pins)	-	ΔVDG2 (Note3)	0.3	V
Power dissipation	-	PD (Note4)	1667	mW
Storage temperature	-	Tstg	-40 to 125	°C

Note1: The withstand voltage for pins (SDA, SCL) is 5V.

Note2: Make sure that the maximum potential difference between each 1.5V system V_{DD} pin (group) does not exceed the rating when connecting (shorting) a 1.5V system V_{DD} pin with a pin of the same group using the same potential difference. And, keep the maximum potential difference between all V_{SS} pins within 0.01 V.

Note3: Make sure that the maximum potential difference between each 3.3V system V_{DD} pin (group) does not exceed the rating when connecting (shorting) a 3.3V system V_{DD} pin with a pin of the same group using the same potential difference. And, keep the maximum potential difference between all V_{SS} pins within 0.01 V.

Note4: If using a temperature higher than Ta = 25°C, reduce by 16.67mW per 1°C increase (When Ta = 85°C, maximum power dissipation is 667mW.)



6.1 Thermal resistance of package

Symbol	Item	Condition	Min	Typ.	Max	Unit
θja	Thermal resistance	JEDEC 4 layer PCB	-	57.5	-	°C/W

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7. Operation Conditions

Cannot guarantee operation of TC90202XBG, when the recommendation power supply voltage range (1.4V to 1.6V, 3.0V to 3.6V) is exceeded. Please use within the specified operating conditions.
Once, when it returns from the over range, it differs from a previous condition.
Then, it must be turned off and power on again.

Item	Corresponding terminal	Symbol	Min	Typ.	Max	Unit
Power voltage of digital block	F1,A6,L6,F11	VDD-D	1.4	1.5	1.6	V
Power voltage of I/O block	D1,H1,A4,L4,A8,L8, C11,D11,H11	VDD-IO	3.0	3.3	3.6	V
Operating temperature	-	Topr	-40	-	85	°C

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8. Electrical characteristic

8.1 DC characteristic

(Ta=25°C, VDD1=1.50±0.1V, VDD2=3.30±0.3V)

Item	Corresponding terminal	Symbol	Min	Typ.	Max	Unit	Note
Power supply current	F1,A6,L6,F11	IDD1 (1.5V system)	-	-	60	mA	When operating in 33MHz
	D1,H1,A4,L4,A8,L8, C11,D11,H11	IDD2 (3.3V system)	-	-	70	mA	When operating in 33MHz
Input voltage	B1,C1,E1,G1,J1,K1, C2,D2,E2,F2,G2,H2, J2,K2,L2,D3,E3,F3, G3,H3,J3,K3,L3,J4, K4,J5,K5,L5,J7,K7, J8	VIH	VDD2x0.8	-	VDD	V	I/O input terminal of 3.3V system
	L7,K8						I/O input terminal of 5.0V system
	B1,C1,E1,G1,J1,K1, C2,D2,E2,F2,G2,H2, J2,K2,L2,D3,E3,F3, G3,H3,J3,K3,L3,J4, K4,J5,K5,L5,J7,K7, J8	VIL	VSS	-	VDDx0.2	V	I/O input terminal of 3.3V system
	L7,K8						I/O input terminal of 5.0V system
Input current	B1,C1,E1,G1,J1,K1, C2,D2,E2,F2,G2,H2, J2,K2,L2,D3,E3,F3, G3,H3,J3,K3,L3,J4, K4,J5,K5,L5,J7,K7, J8	IIH	-10	-	10	μA	I/O input terminal of 3.3V system
	L7,K8						I/O input terminal of 5.0V system
	B1,C1,E1,G1,J1,K1, C2,D2,E2,F2,G2,H2, J2,K2,L2,D3,E3,F3, G3,H3,J3,K3,L3,J4, K4,J5,K5,L5,J7,K7, J8	IIL	-10	-	10	μA	I/O input terminal of 3.3V system
	L7,K8						I/O input terminal of 5.0V system
Output voltage	A2,A3,B3,B4,C4,A5, B5,C5,B6,C6,A7,B7, C7,B8,C8,A9,B9,D9, E9,F9,G9,H9,K9,L9, A10,C10,D10,E10, F10,G10,H10,J10, L10,B11,E11,G11, J11,K11	V_{OH}	VDD2-0.6	-	VDD2	V	I/O input terminal of 3.3V system when load current 4mA
		V_{OL}	VSS	-	0.4	V	I/O input terminal of 3.3V system when load current 4mA

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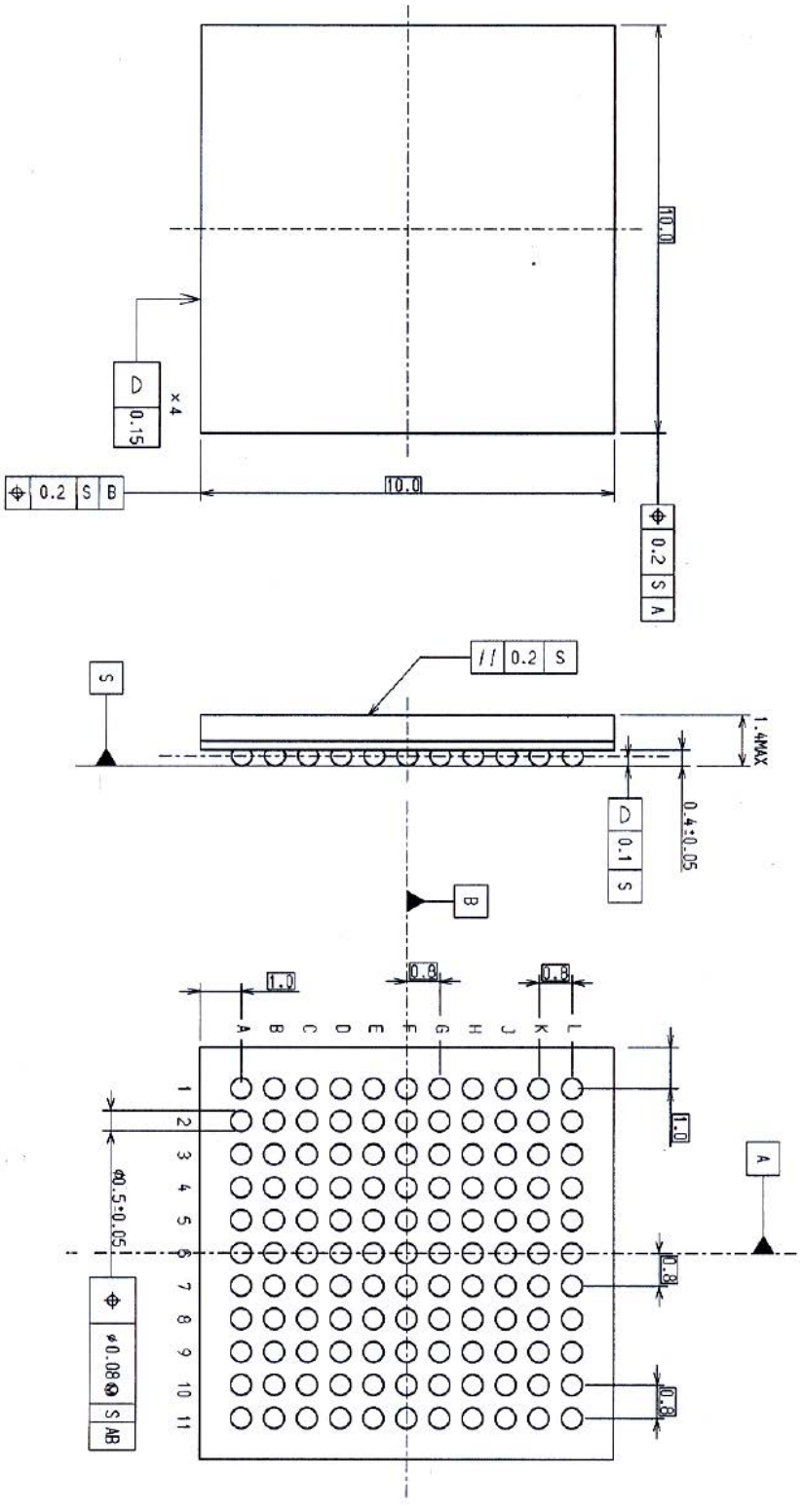
9. Package



Weight : 0.23 g (typ.)

10. Revision history

Date	Revision	Content
2016/04/11	1.00	First Edition
2016/07/05	2.00	2nd edition

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