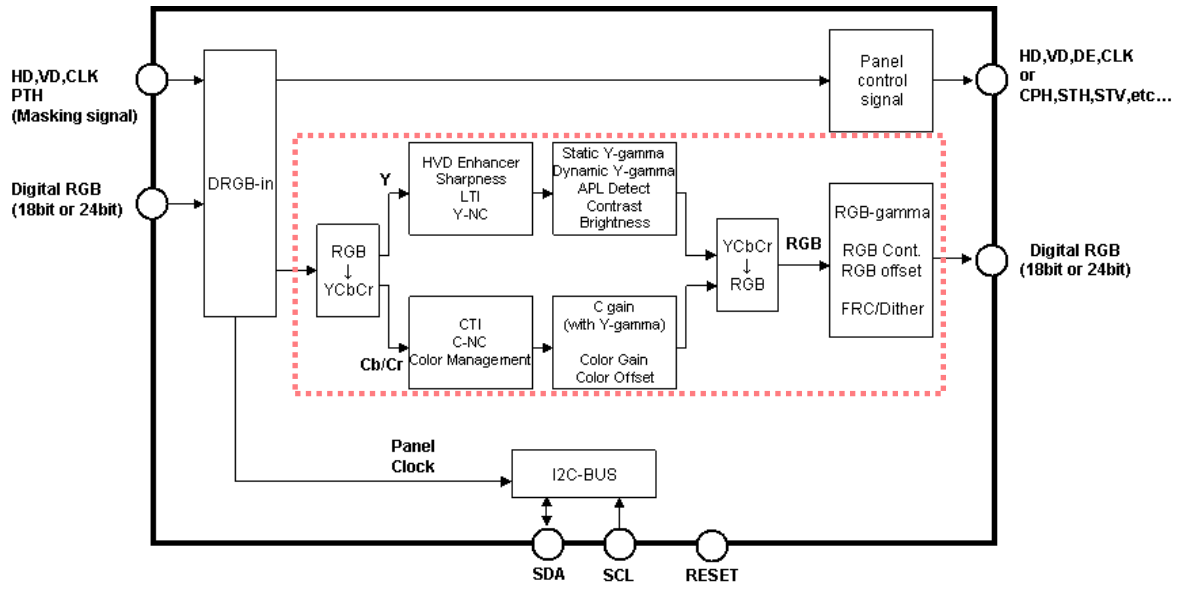
APPLICATION NOTE (Summary)
TC90202XBG

1. Overview

TC90202XBG has picture quality improver (Edge Enhancement, Color adjustment, Contrast adjustment, etc.) for input digital RGB video signal (6bit/8bit), and it outputs digital RGB video signal (6bit/8bit). In addition, it supports output timing control signals for LCD panel.

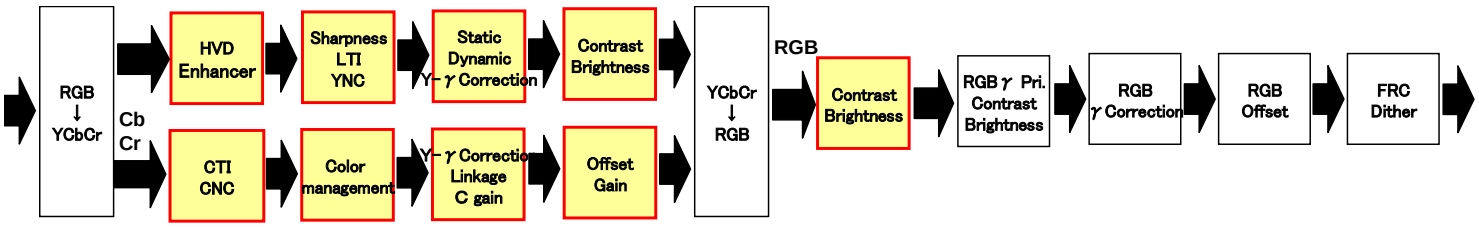
2. Block Diagram

2.1 Internal Block Diagram



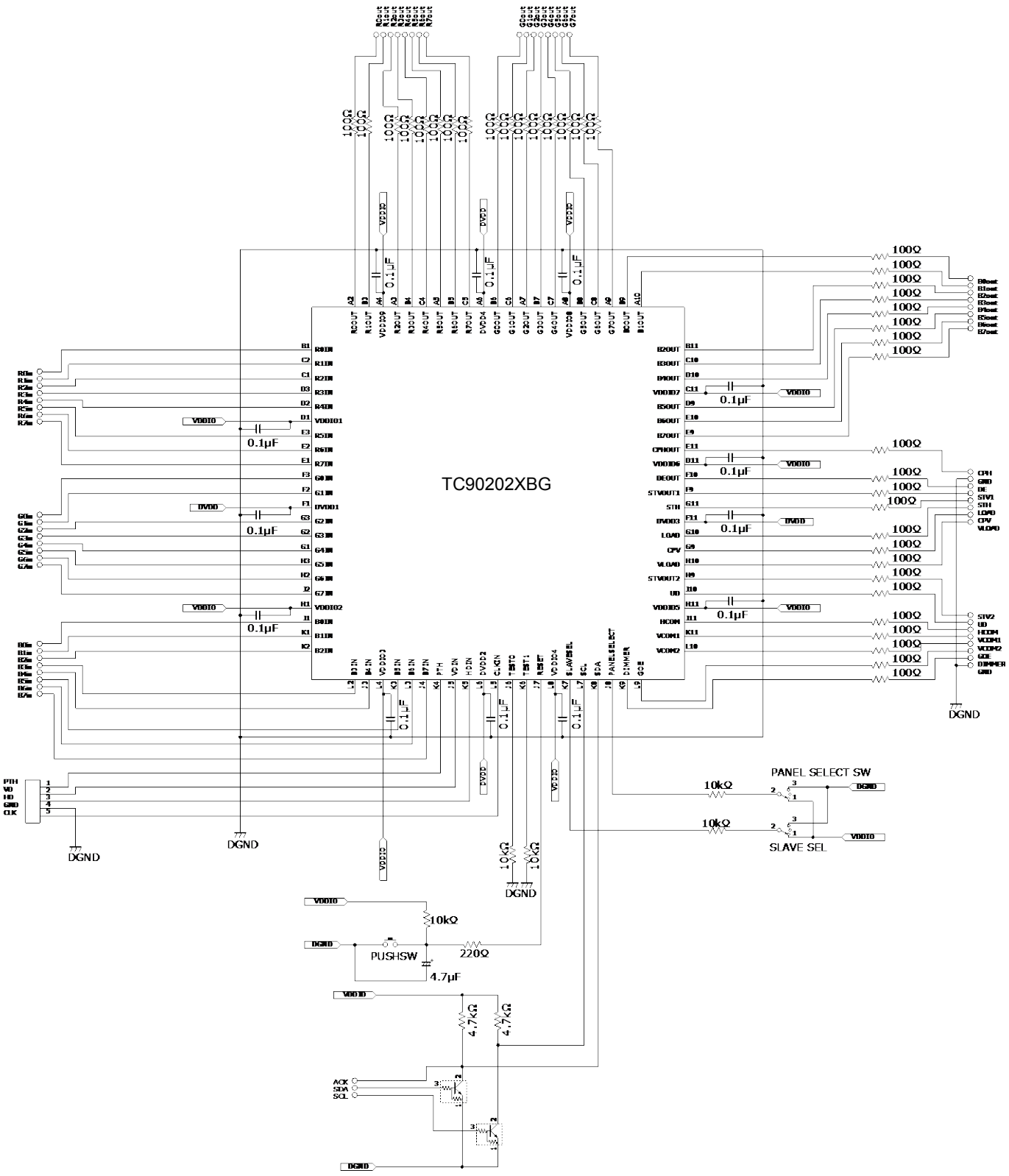
2.2 Picture quality improvement Block

The detail of ▭ block is shown as below.



▭ : These blocks respond to the Masking function of picture quality improver.

3. An example of Application Circuit



4. Pin Description

Pin No.	Pin Name	Pin Function	IO
A1	DGND	Digital GND	GND
B1	R0IN	Digital RGB Input (R0) LSB	Input
C1	R2IN	Digital RGB Input (R2)	Input
D1	VDDIO1	3.3V Power Supply for I/O Block	Power
E1	R7IN	Digital RGB Input (R7)	Input
F1	DVDD1	1.5V Power Supply for Logic circuit	Power
G1	G4IN	Digital RGB Input (G4)	Input
H1	VDDIO2	3.3V Power Supply for I/O Block	Power
J1	B0IN	Digital RGB Input (B0) LSB	Input
K1	B1IN	Digital RGB Input (B1)	Input
L1	DGND	Digital GND	GND
A2	R0OUT	Digital RGB Output (R0) LSB	Output
B2	DGND	Digital GND	GND
C2	R1IN	Digital RGB Input (R1)	Input
D2	R4IN	Digital RGB Input (R4)	Input
E2	R6IN	Digital RGB Input (R6)	Input
F2	G1IN	Digital RGB Input (G1)	Input
G2	G3IN	Digital RGB Input (G3)	Input
H2	G6IN	Digital RGB Input (G6)	Input
J2	G7IN	Digital RGB Input (G7) MSB	Input
K2	B2IN	Digital RGB Input (B2)	Input
L2	B3IN	Digital RGB Input (B3)	Input
A3	R2OUT	Digital RGB Output (R2)	Output
B3	R1OUT	Digital RGB Output (R1)	Output
C3	DGND	Digital GND	GND
D3	R3IN	Digital RGB Input (R3)	Input
E3	R5IN	Digital RGB Input (R5)	Input
F3	G0IN	Digital RGB Input (G0) LSB	Input
G3	G2IN	Digital RGB Input (G2)	Input
H3	G5IN	Digital RGB Input (G5)	Input
J3	B4IN	Digital RGB Input (B4)	Input
K3	B5IN	Digital RGB Input (B5)	Input
L3	B6IN	Digital RGB Input (B6)	Input
A4	VDDIO9	3.3V Power Supply for I/O Block	Power
B4	R3OUT	Digital RGB Output (R3)	Output
C4	R4OUT	Digital RGB Output (R4)	Output
D4	DGND	Digital GND	GND
E4	DGND		
F4	DGND		
G4	DGND		
H4	DGND		
J4	B7IN	Digital RGB Input (B7) MSB	Input
K4	PTH	Timing pulse for picture process masking	Input
L4	VDDIO3	3.3V Power Supply for I/O Block	Power
A5	R5OUT	Digital RGB Output (R5)	Output
B5	R6OUT	Digital RGB Output (R6)	Output
C5	R7OUT	Digital RGB Output (R7) MSB	Output
D5	DGND	Digital GND	GND
E5	DGND		
F5	DGND		
G5	DGND		
H5	DGND		
J5	VDIN	V Sync pulse Input	Input
K5	HDIN	H Sync pulse Input	Input

Pin No	Pin Name	Pin Function	IO
L5	CLKIN	System Clock Input	Input
A6	DVDD4	1.5V Power Supply for Logic circuit	Power
B6	G0OUT	Digital RGB Output (G0) LSB	Output
C6	G1OUT	Digital RGB Output (G1)	Output
D6	DGND	Digital GND	GND
E6	DGND		
F6	DGND		
G6	DGND		
H6	DGND		
J6	TEST0	Test Input 0 (Connect to GND)	Input
K6	TEST1	Test Input 1 (Connect to GND)	Input
L6	DVDD2	1.5V Power Supply for Logic circuit	Power
A7	G2OUT	Digital RGB Output (G2)	Output
B7	G3OUT	Digital RGB Output (G3)	Output
C7	G4OUT	Digital RGB Output (G4)	Output
D7	DGND	Digital GND	GND
E7	DGND		
F7	DGND		
G7	DGND		
H7	DGND		
J7	RESET	Reset signal (Low : Reset, High: Normal)	Input
K7	SLAVESEL	Set up I^2C-BUS Slave Address	Input
L7	SCL	SCL Input for I^2C-BUS	Input
A8	VDDIO8	3.3V Power Supply for I/O Block	Power
B8	G5OUT	Digital RGB Output (G5)	Output
C8	G6OUT	Digital RGB Output (G6)	Output
D8	DGND	Digital GND	GND
E8	DGND		
F8	DGND		
G8	DGND		
H8	DGND		
J8	PANEL SELECT	LCD Control signal (polarity selection of GOE output)	Input
K8	SDA	SDA signal for I^2C-BUS	I/O
L8	VDDIO4	3.3V Power Supply for I/O Block	Power
A9	G7OUT	Digital RGB Output (G7) MSB	Output
B9	B0OUT	Digital RGB Output (B0) LSB	Output
C9	DGND	Digital GND	GND
D9	B5OUT	Digital RGB Output (B5)	Output
E9	B7OUT	Digital RGB Output (B7) MSB	Output
F9	STVOUT1	Control signal for LCD (Vertical start pulse 1)	Output
G9	CPV	Control signal for LCD (Gate clock signal)	Output
H9	STVOUT2	Control signal for LCD (Vertical start pulse 2)	Output
J9	DGND	Digital GND	GND
K9	DIMMER	PWM signal Output	Output
L9	GOE	Control signal for LCD (Reset signal output for LCD panel)	Output
A10	B1OUT	Digital RGB Output (B1)	Output
B10	DGND	Digital GND	GND
C10	B3OUT	Digital RGB Output (B3)	Output
D10	B4OUT	Digital RGB Output (B4)	Output
E10	B6OUT	Digital RGB Output (B6)	Output
F10	DEOUT	Control signal for LCD (Data enable signal for picture area)	Output
G10	LOAD	Control signal for LCD (Writing pulse for the Horizontal direction)	Output
H10	VLOAD	Control signal for LCD (Writing signal for Gate)	Output
J10	UD	Control signal for LCD (Control signal for Vertical writing)	Output
K10	DGND	Digital GND	GND

Pin No	Pin Name	Pin Function	IO
L10	VCOM2	Control signal for LCD (Output voltage for common Electrode 2)	Output
A11	DGND	Digital GND	GND
B11	B2OUT	Digital RGB Output (B2)	Output
C11	VDDIO7	3.3V Power Supply for I/O Block	Power
D11	VDDIO6	3.3V Power Supply for I/O Block	Power
E11	CPHOUT	Control signal for LCD (Source clock signal)	Output
F11	DVDD3	1.5V Power Supply for Logic circuit	Power
G11	STH	Control signal for LCD (Horizontal start pulse)	Output
H11	VDDIO5	3.3V Power Supply for I/O Block	Power
J11	HCOM	Control signal for LCD (Output voltage for Horizontal common Electrode)	Output
K11	VCOM1	Control signal for LCD (Output voltage for common Electrode 1)	Output
L11	DGND	Digital GND	GND

5. I²C Bus Control

1. Slave address

TC90202XBG can control up to 400kbit/s .
It has 2 slave address (0xBC or 0xBE).
Slave address is set by the terminal “SLAVESEL” (K7 pin).

SLAVESEL pin	Slave address	
	Write mode	Read mode
L	0xBC	0xBD
H	0xBE	0xBF

2. Segment address

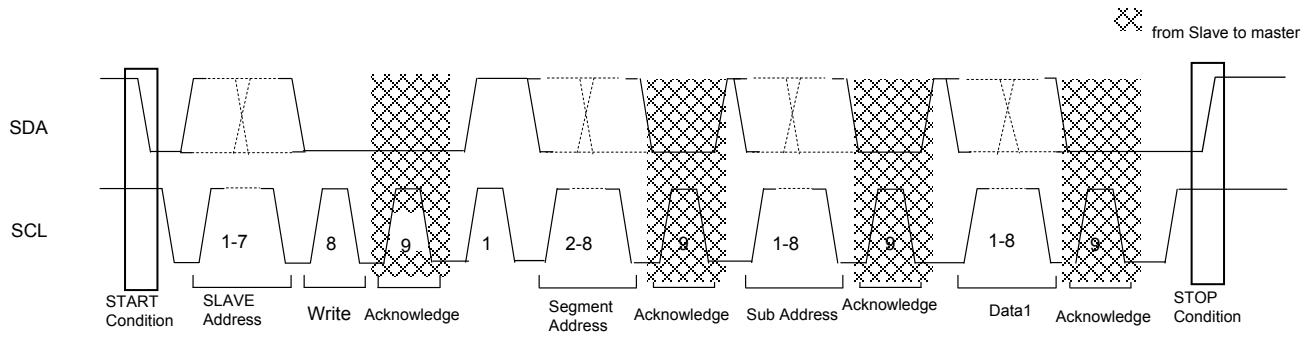
TC90202XBG has Segment Address, and applies to Sub Address below each Segment Address.

Segment address	Contents
0x00	Input signal setting Output signal setting for panel control Masking for Picture quality improver Picture quality improver (RGB gamma correction, HVD enhancer)
0x01	Picture quality improver (Horizontal enhancer, Color management, Dynamic gamma correction, etc…)

3. Data transmission format

5.1.1. Write mode format

When the LSB of the SLAVE Address is set to 0, it means the write mode.
The write mode format for one Sub-address data has the following sequence:
START Condition/ SLAVE Address (write mode)/ Segment Address/ Sub-address/ Data / STOP Condition.
Normally transmitted data order are SLAVE Address, Segment Address, Sub-address, and Data.

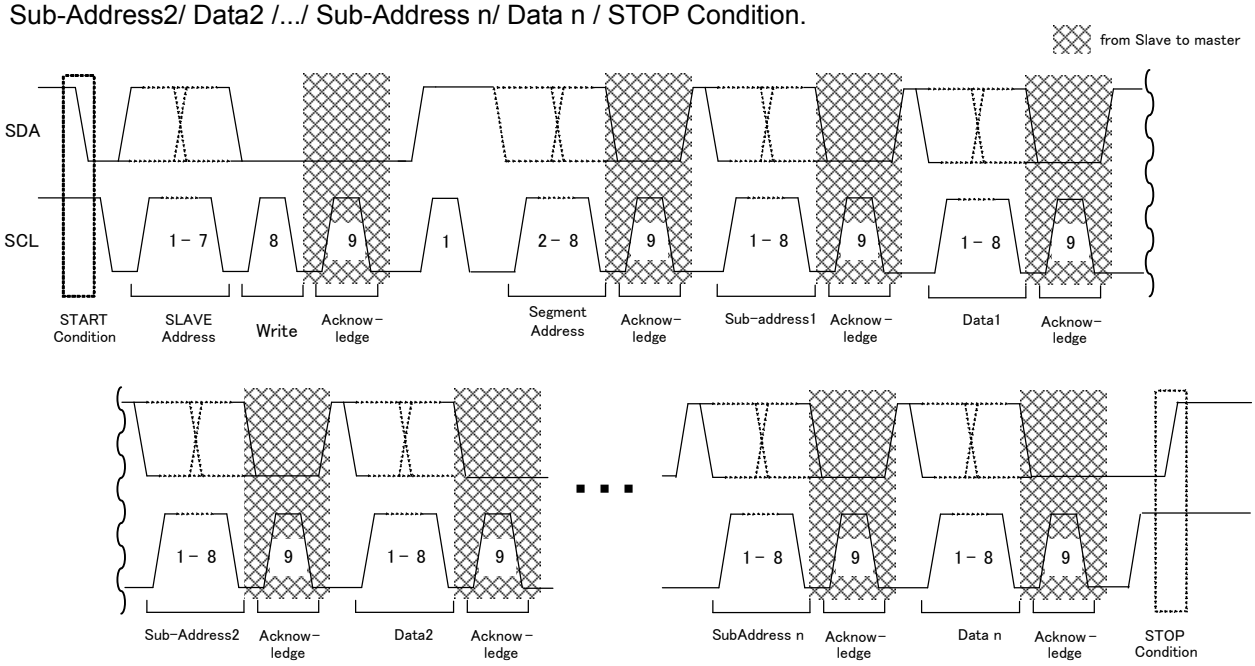


5.1.2. Write mode format (Multi sub address transmission)

When the MSB of the Segment Address is set to 1, it means the multi Sub-address write mode format as shown in following image.

It has the following sequence:

START Condition/ SLAVE Address (write mode)/ Segment Address (MSB=1)/ Sub-Address1/ Data1 / Sub-Address2/ Data2 /.../ Sub-Address n/ Data n / STOP Condition.

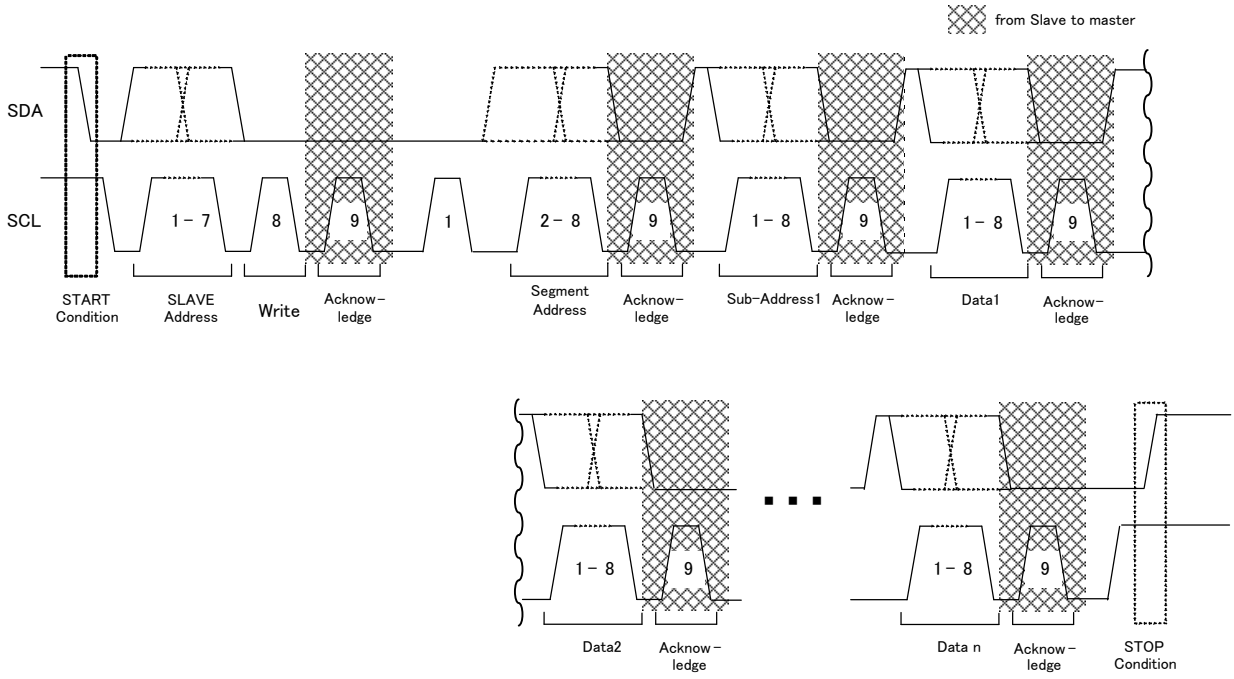


5.1.3. Write mode format (Auto increment mode)

When the MSB of the Segment Address is set to 0, it means the auto increment mode format as shown in following image.

It has the following sequence:

START Condition/ SLAVE Address (write mode)/ Segment Address (MSB=0)/ Sub-Address1/ Data1 / Data2 /.../ Data n / STOP Condition.



5.1.4. Read mode

When the LSB of the SLAVE Address is set to 1, it means the read mode as shown below.
The read mode has auto increment mode only.
The sequence of this mode is as follows:
START Condition/ SLAVE Address (write)/ Segment Address/ Sub-Address/ Repeated START Condition/ SLAVE Address (read)/ Data1 (read) / Data2 (read) /.../ Data n (read) / STOP Condition.

At the first, this mode needs to set Segment Address and Sub-Address with write mode, and then Repeated START Condition is also needed to start to read sequence.
And more, the master should output negative ACK (High) at the last read data before the STOP Condition.
If the STOP Condition is send without this negative ACK, this LSI does not recognize the end of read sequence and does not release SDA line to open condition until next START Condition or negative ACK.
If there is no negative ACK (High), then this LSI keeps outputting until the Sub-address 0xFF, and repeats the output of the data of the Sub-address 0xFF afterwards.
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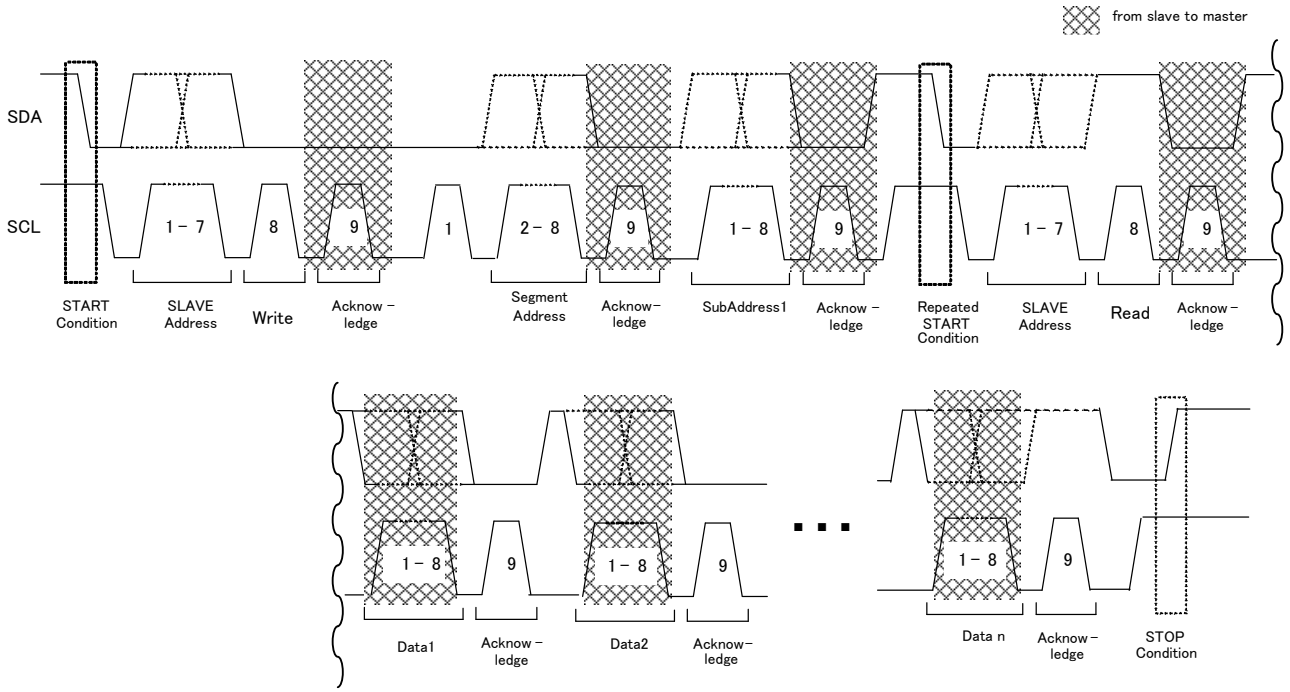


6. Register

● **Please not change the data value of the registers** which are colored to gray in this document, because these registers are defined as "Reserved".
If “Reserved” register bit exists on sub address to change data, **please write initial data value to the bit on the “Reserved” register and don’t change the value**.

● not VLT : Not concerned with vertical sync signal timing, it changes to new data.
● INIT: ** : Default setting.
● Underline portion are default setting.
● Please not change the data value of the registers, which are not described in this document.

● In this document, data value is described as follows.
Ex. 0x3F or 3Fh (hexadecimal) = 0011_1111 (binary) = 63 (decimal)

Segment Address 0x00

6.1. Sub Address 0x00 (Input / output terminal control)

Sub	D7	D6	D5	D4	D3	D2	D1	D0
0x00	Reserved	**IPIN_SEL[2:0]**			Reserved	**OPIN_SEL[2:0]**		
not VLT	Fix to 0	DRGB-in bit length	DRGB-in MSB-LSB	DRGB-in R/B	Fix to 0	DRGB-out 6bit shift	DRGB-out MSB-LSB	DRGB-out R/B
INIT: 0x00		0:8bit 1:6bit	0:Normal 1:MSB/LSB inversion	0:Normal 1:R-B swap		0:Normal 1:Shift	0:Normal 1:MSB/LSB inversion	0:Normal 1:R-B swap

IPIN_SEL[2] : Set up input Digital RGB signal bit length.
0：8bit length
1：6bit length (Top 6bits are functional for **IPIN_SEL[1:0]**)

IPIN_SEL[1] : Set up MSB - LSB inversion for input terminals of Digital RGB.
0：Normal
1：MSB/LSB inversion
（Note）：**IPIN_SEL[2]**＝1→ in case R input : R7IN～R2IN pins are object bits.

IPIN_SEL[0] : Swap R input and B input.
0：Normal
1：R⇔B （R7IN pin → B7 input signal, B7IN pin →R7input signal・・）

OIPIN_SEL[2] : Set up relative output Pins with **OPIN_SEL[1:0]** at 6bit output .
0：Normal
1：6bit shift It becomes active for high 6bit for **OPIN_SEL[1:0]**.
(Lower 2bit outputs low level.)

OPIN_SEL[1] : Set up MSB - LSB bit inversion for output terminals of Digital RGB.
0：Normal
1：MSB/LSB inversion
（Note）：**OPIN_SEL[2]**＝1 → in case R input : R7OUT～R2OUT pins are object bits.

OPIN_SEL[0] : Swap R output and B output.
0：Normal
1：R⇔B（R7OUT pin → B7 output signal, B7OUT pin → R7 output signal・・）

6.2. Sub Address 0x01 to 0x0F (T-con signal output)

Sub	D7	D6	D5	D4	D3	D2	D1	D0
0x01	**LCD_Out**	**LCD_Out _Mode**	**P_CPV**	**P_LOAD**	**P_STH**	**P_VLOAD**	**P_STV**	**P_CPH**
not VLT	T-con pulse output	Output mode	CPV pulse polarity	LOAD pulse polarity	STH pulse polarity	VLOAD pulse polarity	STV pulse polarity	CPH pulse polarity
INIT: 0x7F	0: OFF (ALL Low) 1:ON	0: Other 1: Standard (HD/VD/DE)	0: Nega 1: Posi	0: Nega 1: Posi	0: Nega 1: Posi	0: Nega 1: Posi	0: Nega 1: Posi	0: Nega 1: Posi
0x02	**P_VCOM2**	**UDOUT**	**STVSEL**	**P_DE**	**HCOM_ON**	Reserved	Reserved	**GOE_TGL**
not VLT	VCOM2 out	UD out	STV out	DE pulse polatiry	HCOM out	Fix to 0	Fix to 0	GOE out
INIT: 0x00	0: Nega 1: Posi	0: Low 1: High	0: STV1 1: STV2	0: Nega 1: Posi	0:OFF 1:ON			0:Normal 1:Reverse
0x03	**STH_START[7:0]**							
not VLT	Start phase of STH pulse							
INIT: 0x08	0000_0000:-7clk to 0000_1000:+1clk to 1111_1111:+248clk							
0x04	**STH_WIDTH[7:0]**							
not VLT	Width of STH pulse							
INIT: 0x00	0000_0000:1clk to 1111_1111:256clk							
0x05	Reserved	Reserved	**STV_VSTART[5:0]**					
not VLT	Fix to 0	Fix to 0	Width of STV pulse					
INIT: 0x02			00_0000:-1Line to 00_0010:+1Line to 11_1111:+62Line					
0x06	Reserved	Reserved	Reserved	**STV_VWIDTH[4:0]**				
not VLT	Fix to 0	Fix to 0	Fix to 0	Width of STV pulse				
INIT: 0x00				0_0000:1Line to 1_1111:32Line				
0x07	**STV_HSTART[7:0]**							
not VLT	Start phase of STV pulse (from front DE Edge to the front direction)							
INIT: 0x00	0000_0000:-7clk to 0000_1000:+1clk to 1111_1111:+248clk							
0x08	**LOAD_START[7:0]**							
not VLT	Start pulse of LOAD pulse (from front DE Edge to the front direction)							
INIT: 0x08	0000_0000:-7clk to 0000_1000:+1clk to 1111_1111:+248clk							
0x09	**LOAD_WIDTH[7:0]**							
not VLT	Width of LOAD pulse							
INIT: 0x00	0000_0000:1clk to 1111_1111:256clk							
0x0A	**CPV_START[7:0]**							
not VLT	Start phase of CPV pulse							
INIT: 0x08	0000_0000:-7clk to 0000_1000:+1clk to 1111_1111:+248clk							
0x0B	**CPV_WIDTH[7:0]**							
not VLT	Width of CPV pulse							
INIT: 0x00	0000_0000:1clk to 1111_1111:256clk							
0x0C	**VLOAD_START[7:0]**							
not VLT	Start phase of VLOAD pulse							
INIT: 0x08	0000_0000:-7clk to 0000_1000:+1clk to 1111_1111:+248clk							
0x0D	**VLOAD_WIDTH[7:0]**							
not VLT	Width of VLOAD pulse							
INIT: 0x00	0000_0000:1clk to 1111_1111:256clk							
0x0E	Reserved	Reserved	**VCOM_VSTART[5:0]**					
not VLT	Fix to 0	Fix to 0	Basing line of VCOM1/2 pulse					
INIT: 0x02			00_0000:-1Line to 00_0010:+1Line to 11_1111:+62Line					
0x0F	**VCOM_HSTART[7:0]**							
not VLT	Phase of VCOM1/2 pulse							
INIT: 0x08	0000_0000:-7clk to 0000_1000:+1clk to 1111_1111:+248clk							

LCD_OUT: T-con pulse output ON/OFF
0: OFF (All low out)
1: ON (Active)

LCD_OUT_MODE: T-con pulse output mode
0: Other
All signal output
1: Standard
Active pins: HD (STH), VD (STV), CLK (CPH), DEOUT

P_CPV: CPV signal polarity
0: Negative
1: Positive

P_LOAD: LOAD signal polarity
0: Negative
1: Positive

P_STH: STH (HD) signal polarity
0: Negative
1: Positive

P_VLOAD: VLOAD signal polarity
0: Negative
1: Positive

P_STV: STV (VD) signal polarity
0: Negative
1: Positive

P_CPH: CPH (CLK) signal polarity
0: Negative
1: Positive

P_VCOM2: VCOM2 signal polarity
0: Reverse polarity for VCOM1
1: Same polarity for VCOM1

UDOUT: UD signal output
0: Low out
1: High out

STVSEL: STV signal output
0: STV1 pin
1: STV2 pin

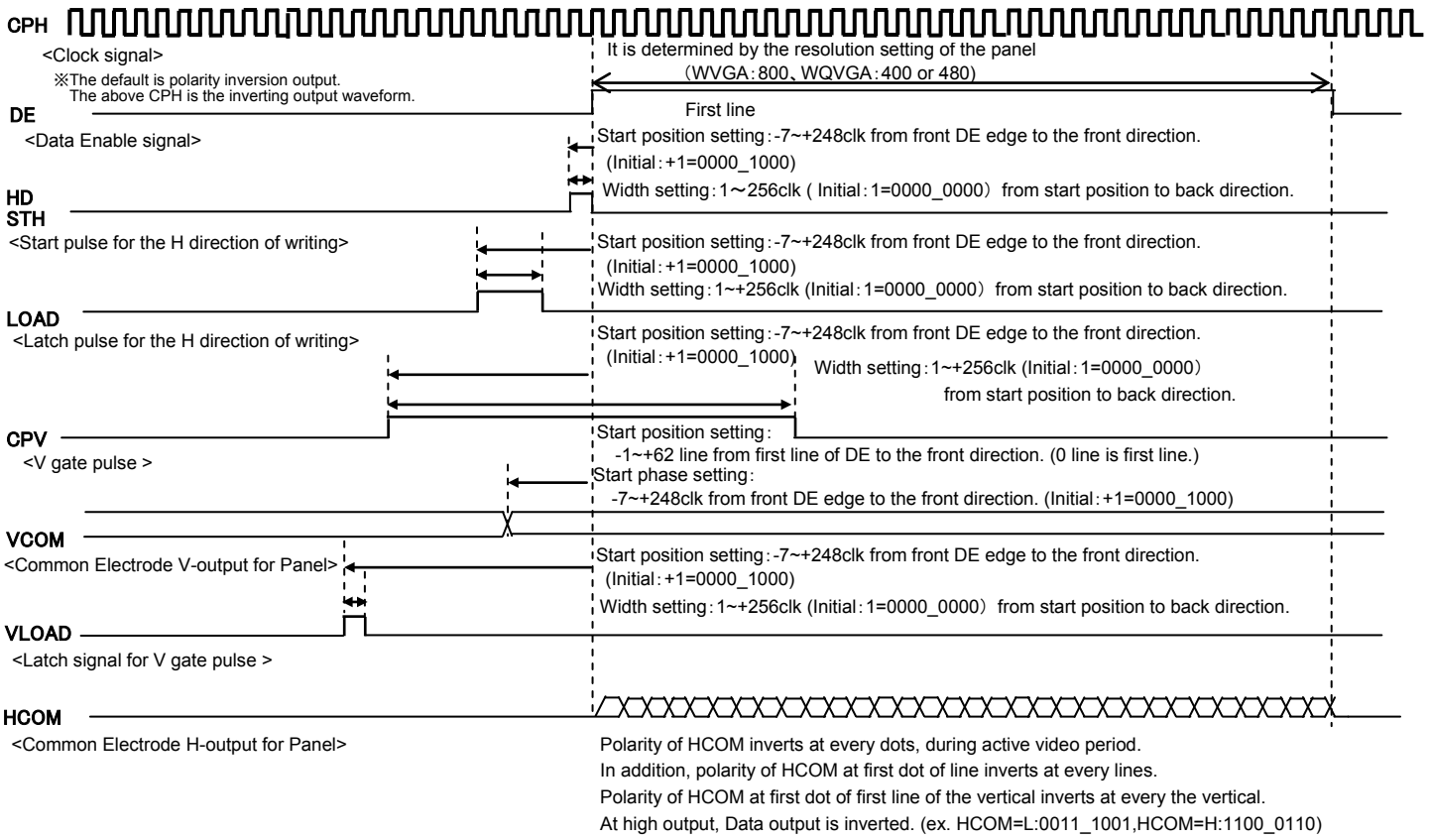
P_DE: DE signal polarity
0: Negative
1: Positive

P_HCOM: HCOM output ON/OFF
0: OFF
1: ON

GOE_TGL: GOE signal output
0: Normal
1: Reverse

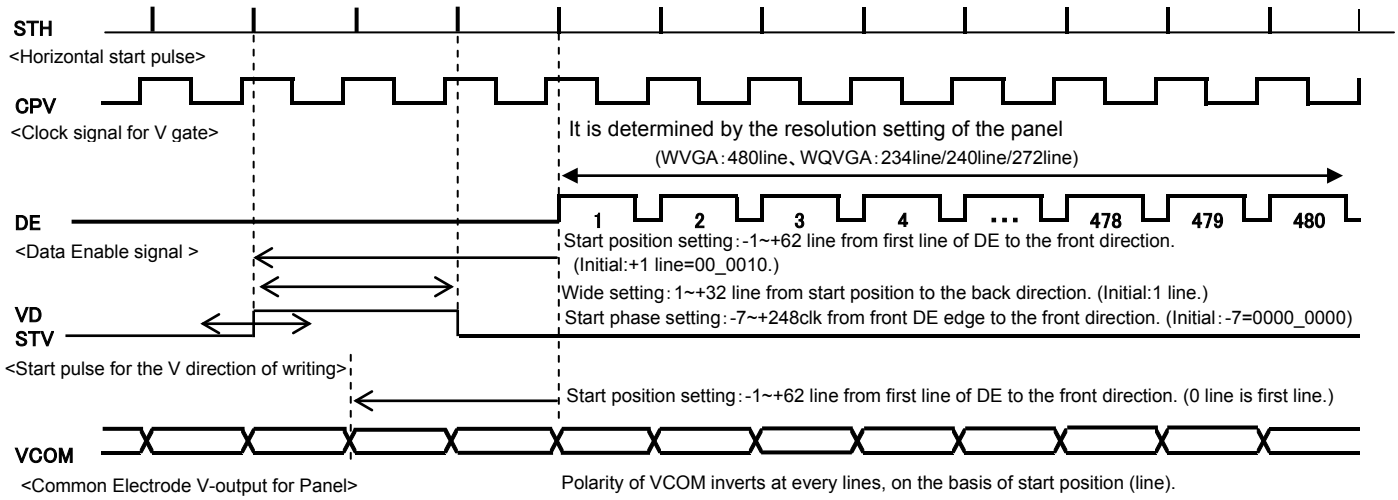
Control signals timing for LCD panel.

<Horizontal>

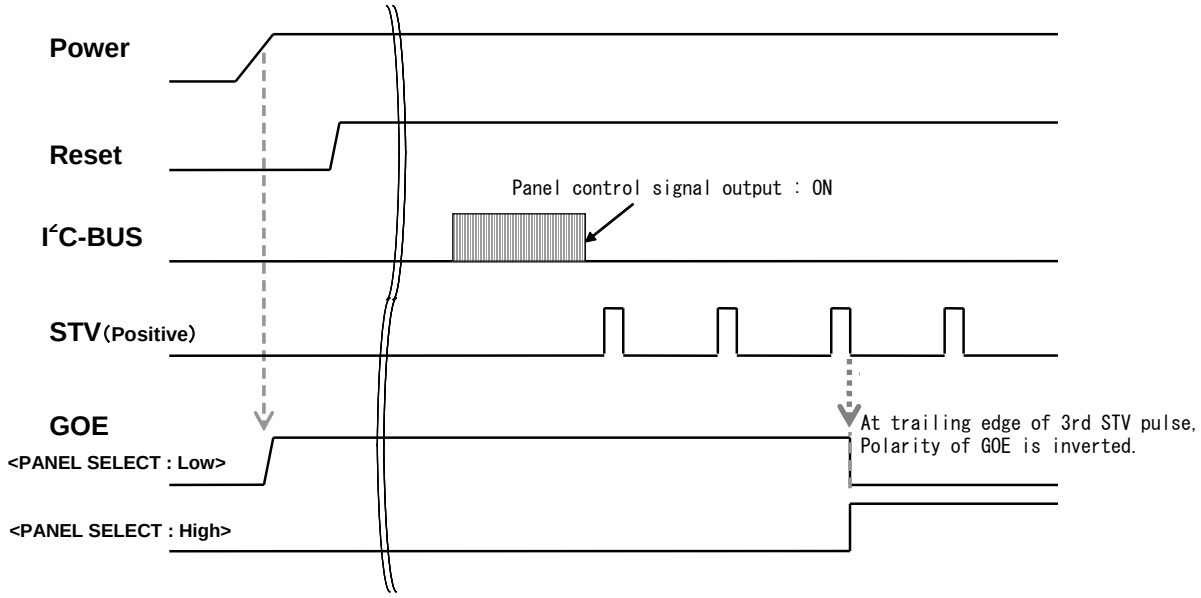


Control signals timing for LCD panel.

<Vertical>



<Power on and start sequence>



6.3. Sub Address 0x10 to 0x17 (HVD Enhancer)

Sub	D7	D6	D5	D4	D3	D2	D1	D0
0x10	**ENHON**	**CORE_MET**	Reserved	Reserved	Reserved	**HALFSEL**	Reserved	Reserved
	ENH ON/OFF	Noise canceller	Fix to 0	Fix to 0	Fix to 0	5tap Filter process	Fix to 0	Fix to 0
INIT: 0x00	0: OFF 1: ON	0:OFF (Coring) 1:ON (N.C.)				0:OFF 1:ON		
0x11	**V_35**	**V_OFF**	**H_SEL**	**H_35**	**H_OFF**	**D_SEL**	**D_35**	**D_OFF**
	Vertical tap		Horizontal tap			Diagonal tap		
	Tap number	ON/OFF	f0	Tap number	ON/OFF	f0	Tap number	ON/OFF
INIT: 0x00	0:3tap 1:5tap	0:ON 1:OFF	0:Narrow 1:Wide	0:3tap 1:5tap	0:ON 1:OFF	0:Narrow 1:Wide	0:3tap 1:5tap	0:ON 1:OFF
0x12	**ENHLV[3:0]**				**ENHLV_CORE[3:0]**			
	Enhancer gain				Noise canceller gain			
INIT: 0x00	0000:min to 1111:max				0000:min to 1111:max			
0x13	**CORE_LV[7:0]**							
	Coring level							
INIT: 0x00	0000_0000:Coring OFF 0000_0001:min to 1111_1111:max							
0x14	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
INIT: 0x00	Fix to 0	Fix to 0	Fix to 0	Fix to 0	Fix to 0	Fix to 0	Fix to 0	Fix to 0
0x15	**YCO1_ON**	**YCO1_COLV**	Reserved	Reserved	**YCO1_YLV[3:0]**			
	Coring up with low Y	Coring up with low Y Gain	Fix to 0	Fix to 0	Coring up with low Y Start Y level			
INIT: 0x00	0:OFF 1:ON	0:Y/16 1:Y/8			0000: 0LSB to 1111: 480LSB <10bit, 32LSB step>			
0x16	**YCO2_ON**	**YCO2_COLV**	Reserved	Reserved	**YCO2_YLV[3:0]**			
	Coring up with low Y	Coring up with low Y Gain	Fix to 0	Fix to 0	Coring up with low Y Start Y level			
INIT: 0x00	0:OFF 1:ON	0:Y/8 1:Y/4			0000: 0LSB to 1111: 480LSB <10bit, 32LSB step>			
0x17	**LIMIT_ON**	**LIMIT_MET**	**LIMIT_LV[5:0]**					
	Enhancer Limit	Limit mode	Limit level					
INIT: 0x00	0:OFF 1:ON	0:Keep 1:Pairing	00_0000: 0LSB to 11_1111: 252LSB <10bit, 8LSB step>					

< HVD Enhance function for Y signal >
The processing depends on the comparison the value of difference level around the target pixel and Coring level.

The value of difference level around the target pixel > coring level
⇨ Active Enhance function.

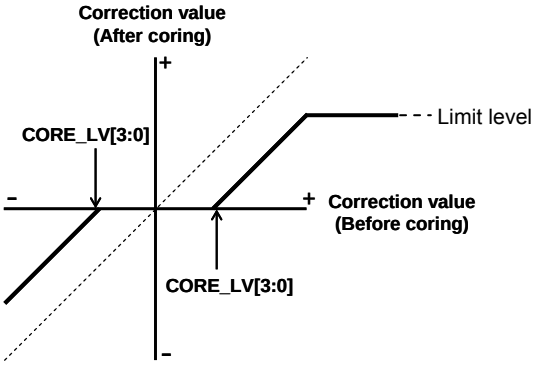
The value of difference level around the target pixel < coring level
⇨ Select non-enhance or noise cancel process via **CORE_MET**.

ENHON: Set up HVD Enhancer function.
0: OFF
1: ON

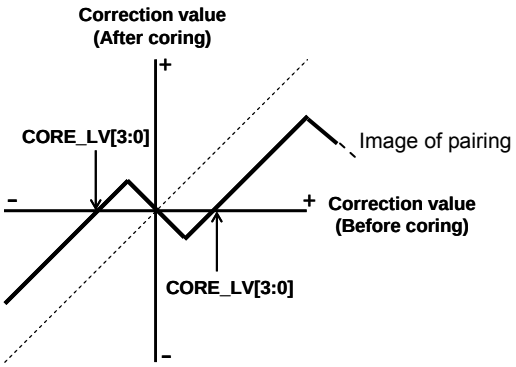
ENHLV [3:0]: Set up Enhancer Gain.
The correction value of enhance is increased by increasing enhance gain.

CORE_LV[7:0]：Set up the Coring level.
0x00: it means Coring function OFF.
The enhance function becomes effective for smaller uneven component when decrease coring level.

CORE_MET: Select the coring processing for HVD enhancer
0: Coring mode (The functional correction is not effective for under the coring level.)
1: Noise canceller mode (minus gain for coring area)



<When **CORE_MET** = 0>



<When **CORE_MET** = 1>

＜ Adaptive Coring function ＞

It can reduce noise at low brightness portion by the bigger coring level which responds to dark level.

YCO1_YLV[3:0]：Set up start Y level for Adaptive Coring function.
Under the YCO1_YLV[3:0], The Coring level increase than CORE_LV[7:0] with the brightness decreasing.

YCO1_COLV：Set up the Gain for Adaptive Coring level.
Set up the gain for the coring level at the under Y level for YCO_YLV [3:0].
It increases in order corresponding to Y/16、Y/8、Y/4.

＜ Limit process for HVD Enhance ＞

LIMIT_ON: Set up Limit process at the after stage of HVD enhance.
0: OFF
1: ON

LIMIT_LV [5:0]: Set up Limit level at the after stage of HVD enhance.

LIMIT_MET: Select the Limit process mode.
0: Keep mode (It keeps the Limit level which is set via **LIMIT_LV [5:0]**.)
1: Pairing mode (It reduce the enhanced component which is over **LIMIT_LV [5:0]**.)

HALFSEL：Set up Filter process at using 5tap
0：Filter OFF
1：Filter ON　(It is recommended when set up 5tap)

6.4. Sub Address 0x20 to 0x4F (RGB-gamma correction)

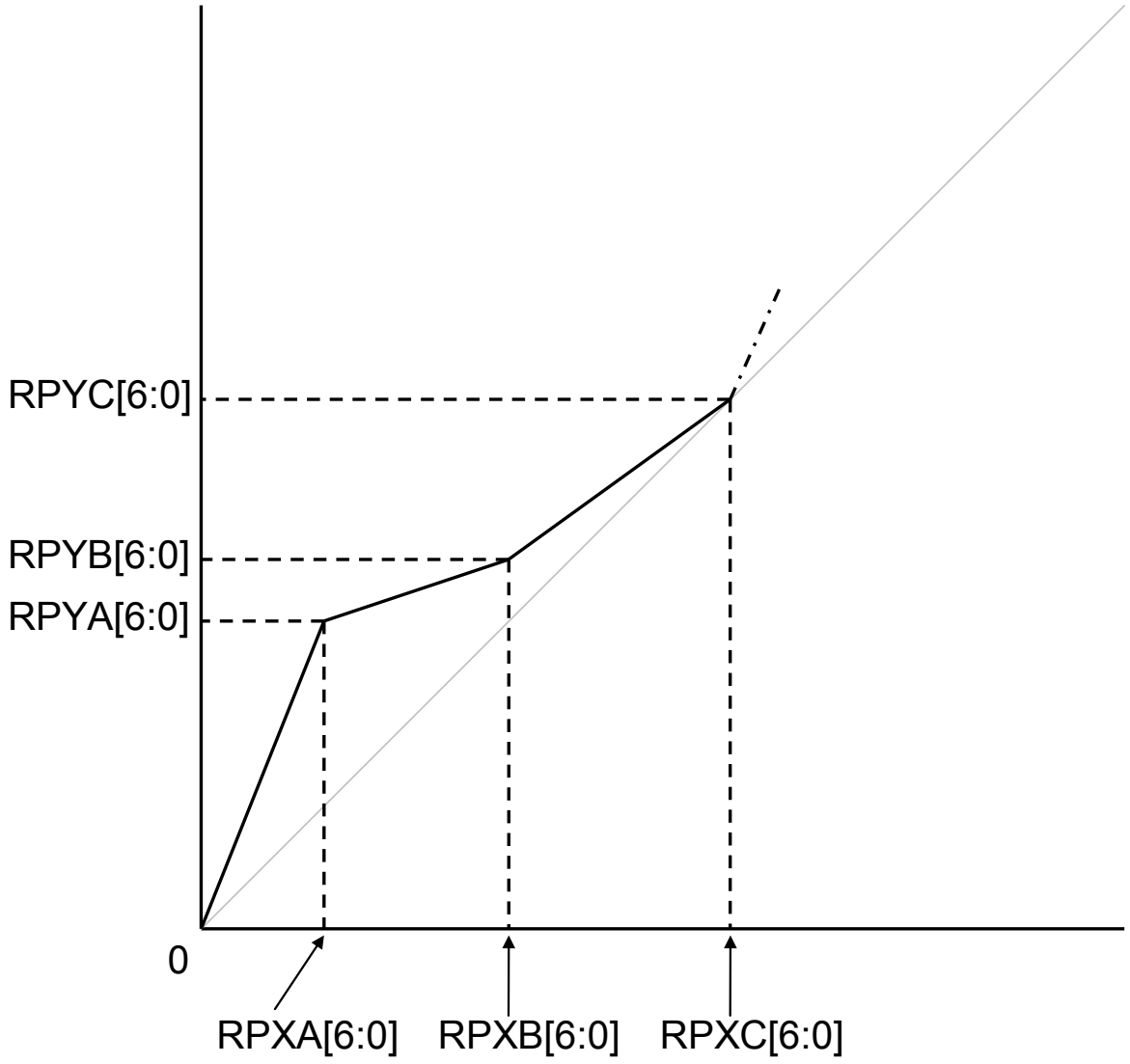
Sub	D7	D6	D5	D4	D3	D2	D1	D0
0x20	**RGB _GANMAON**	**RPXA[6:0]**						
	RGB gamma	R gamma A X axis						
INIT: 0x00	0:OFF 1:ON	000_0000:1LSB to 111_1111:255LSB						
0x21	**GANMA _RGBSAME**	**RPYA[6:0]**						
	RGB gamma setting mode	R gamma A Y axis						
INIT: 0x00	0:Each setting 1:RGB same setting	000_0000:1LSB to 111_1111:255LSB						
0x22	Reserved	**RPXB[6:0]**						
	Fix to 0	R gamma B X axis						
INIT: 0x00		000_0000:1LSB to 111_1111:255LSB						
0x23	Reserved	**RPYB[6:0]**						
	Fix to 0	R gamma B Y axis						
INIT: 0x00		000_0000:1LSB to 111_1111:255LSB						
0x24	Reserved	**RPXC[6:0]**						
	Fix to 0	R gamma C X axis						
INIT: 0x00		000_0000:1LSB to 111_1111:255LSB						
0x25	Reserved	**RPYC[6:0]**						
	Fix to 0	R gamma C Y axis						
INIT: 0x00		000_0000:1LSB to 111_1111:255LSB						
0x26	Reserved	**RPXD[6:0]**						
	Fix to 0	R gamma D X axis						
INIT: 0x00		000_0000:1LSB to 111_1111:255LSB						
0x27	Reserved	**RPYD[6:0]**						
	Fix to 0	R gamma D Y axis						
INIT: 0x00		000_0000:1LSB to 111_1111:255LSB						
0x28	Reserved	**RPXE[6:0]**						
	Fix to 0	R gamma E X axis						
INIT: 0x00		000_0000:1LSB to 111_1111:255LSB						
0x29	Reserved	**RPYE[6:0]**						
	Fix to 0	R gamma E Y axis						
INIT: 0x00		000_0000:1LSB to 111_1111:255LSB						
0x2A	Reserved	**RPXF[6:0]**						
	Fix to 0	R gamma F X axis						
INIT: 0x00		000_0000:1LSB to 111_1111:255LSB						
0x2B	Reserved	**RPYF[6:0]**						
	Fix to 0	R gamma F Y axis						
INIT: 0x00		000_0000:1LSB to 111_1111:255LSB						
0x2C	Reserved	**RPXG[6:0]**						
	Fix to 0	R gamma G X axis						
INIT: 0x00		000_0000:1LSB to 111_1111:255LSB						
0x2D	Reserved	**RPYG[6:0]**						
	Fix to 0	R gamma G Y axis						
INIT: 0x00		000_0000:1LSB to 111_1111:255LSB						
0x2E	Reserved	**RPXH[6:0]**						
	Fix to 0	R gamma H X axis						
INIT: 0x00		000_0000:1LSB to 111_1111:255LSB						
0x2F	Reserved	**RPYH[6:0]**						
	Fix to 0	R gamma H Y axis						
INIT: 0x00		000_0000:1LSB to 111_1111:255LSB						

Sub	D7	D6	D5	D4	D3	D2	D1	D0
0x30	Reserved	**GPXA[6:0]**						
	Fix to 0	G gamma A X axis						
INIT: 0x00		000_0000:1LSB to 111_1111:255LSB						
0x31	Reserved	**GPYA[6:0]**						
	Fix to 0	G gamma A Y axis						
INIT: 0x00		000_0000:1LSB to 111_1111:255LSB						
0x32	Reserved	**GPXB[6:0]**						
	Fix to 0	G gamma B X axis						
INIT: 0x00		000_0000:1LSB to 111_1111:255LSB						
0x33	Reserved	**GPYB[6:0]**						
	Fix to 0	G gamma B Y axis						
INIT: 0x00		000_0000:1LSB to 111_1111:255LSB						
0x34	Reserved	**GPXC[6:0]**						
	Fix to 0	G gamma C X axis						
INIT: 0x00		000_0000:1LSB to 111_1111:255LSB						
0x35	Reserved	**GPYC[6:0]**						
	Fix to 0	G gamma C Y axis						
INIT: 0x00		000_0000:1LSB to 111_1111:255LSB						
0x36	Reserved	**GPXD[6:0]**						
	Fix to 0	G gamma D X axis						
INIT: 0x00		000_0000:1LSB to 111_1111:255LSB						
0x37	Reserved	**GPYD[6:0]**						
	Fix to 0	G gamma D Y axis						
INIT: 0x00		000_0000:1LSB to 111_1111:255LSB						
0x38	Reserved	**GPXE[6:0]**						
	Fix to 0	G gamma E X axis						
INIT: 0x00		000_0000:1LSB to 111_1111:255LSB						
0x39	Reserved	**GPYE[6:0]**						
	Fix to 0	G gamma E Y axis						
INIT: 0x00		000_0000:1LSB to 111_1111:255LSB						
0x3A	Reserved	**GPXF[6:0]**						
	Fix to 0	G gamma F X axis						
INIT: 0x00		000_0000:1LSB to 111_1111:255LSB						
0x3B	Reserved	**RPYF[6:0]**						
	Fix to 0	G gamma F Y axis						
INIT: 0x00		000_0000:1LSB to 111_1111:255LSB						
0x3C	Reserved	**RPXG[6:0]**						
	Fix to 0	G gamma G X axis						
INIT: 0x00		000_0000:1LSB to 111_1111:255LSB						
0x3D	Reserved	**GPYG[6:0]**						
	Fix to 0	G gamma G Y axis						
INIT: 0x00		000_0000:1LSB to 111_1111:255LSB						
0x3E	Reserved	**GPXH[6:0]**						
	Fix to 0	G gamma H X axis						
INIT: 0x00		000_0000:1LSB to 111_1111:255LSB						
0x3F	Reserved	**GPYH[6:0]**						
	Fix to 0	G gamma H Y axis						
INIT: 0x00		000_0000:1LSB to 111_1111:255LSB						

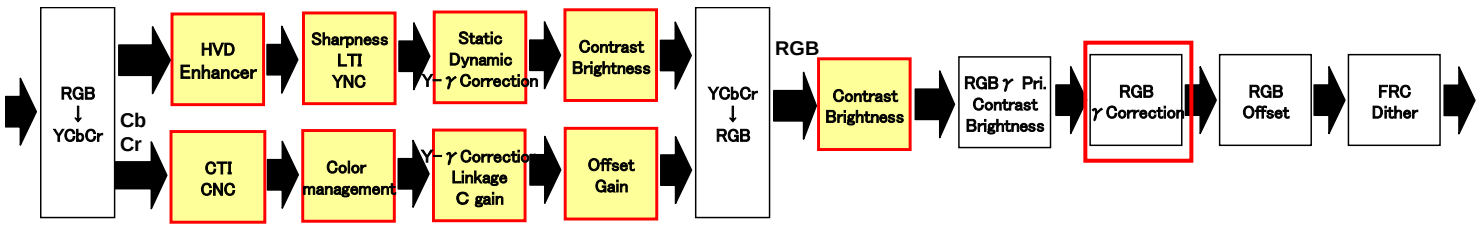
Sub	D7	D6	D5	D4	D3	D2	D1	D0
0x40	Reserved	**BPXA[6:0]**						
	Fix to 0	B gamma A X axis						
INIT: 0x00		000_0000:1LSB to 111_1111:255LSB						
0x41	Reserved	**BPYA[6:0]**						
	Fix to 0	B gamma A Y axis						
INIT: 0x00		000_0000:1LSB to 111_1111:255LSB						
0x42	Reserved	**BPXB[6:0]**						
	Fix to 0	B gamma B X axis						
INIT: 0x00		000_0000:1LSB to 111_1111:255LSB						
0x43	Reserved	**BPYB[6:0]**						
	Fix to 0	B gamma B Y axis						
INIT: 0x00		000_0000:1LSB to 111_1111:255LSB						
0x44	Reserved	**BPXC[6:0]**						
	Fix to 0	B gamma C X axis						
INIT: 0x00		000_0000:1LSB to 111_1111:255LSB						
0x45	Reserved	**BPYC[6:0]**						
	Fix to 0	B gamma C Y axis						
INIT: 0x00		000_0000:1LSB to 111_1111:255LSB						
0x46	Reserved	**BPXD[6:0]**						
	Fix to 0	B gamma D X axis						
INIT: 0x00		000_0000:1LSB to 111_1111:255LSB						
0x47	Reserved	**BPYD[6:0]**						
	Fix to 0	B gamma D Y axis						
INIT: 0x00		000_0000:1LSB to 111_1111:255LSB						
0x48	Reserved	**BPXE[6:0]**						
	Fix to 0	B gamma E X axis						
INIT: 0x00		000_0000:1LSB to 111_1111:255LSB						
0x49	Reserved	**BPYE[6:0]**						
	Fix to 0	B gamma E Y axis						
INIT: 0x00		000_0000:1LSB to 111_1111:255LSB						
0x4A	Reserved	**BPXF[6:0]**						
	Fix to 0	B gamma F X axis						
INIT: 0x00		000_0000:1LSB to 111_1111:255LSB						
0x4B	Reserved	**BPYF[6:0]**						
	Fix to 0	B gamma F Y axis						
INIT: 0x00		000_0000:1LSB to 111_1111:255LSB						
0x4C	Reserved	**BPXG[6:0]**						
	Fix to 0	B gamma G X axis						
INIT: 0x00		000_0000:1LSB to 111_1111:255LSB						
0x4D	Reserved	**BPYG[6:0]**						
	Fix to 0	B gamma G Y axis						
INIT: 0x00		000_0000:1LSB to 111_1111:255LSB						
0x4E	Reserved	**BPXH[6:0]**						
	Fix to 0	B gamma H X axis						
INIT: 0x00		000_0000:1LSB to 111_1111:255LSB						
0x4F	Reserved	**BPYH[6:0]**						
	Fix to 0	B gamma H Y axis						
INIT: 0x00		000_0000:1LSB to 111_1111:255LSB						

<RGB gamma correction>

This function is RGB gamma correction for each of signal.
The start point is input 0LSB and output 0LSB.
It can set 8 point of inflection. (See diagram as below.)
Input and output setting: 2LSB step.



(Note) The RGB gamma correction is placed at the back end. (See diagram as below.)



6.5. Sub Address 0x50 to 0x52 (Digital RGB Input)

Sub	D7	D6	D5	D4	D3	D2	D1	D0
0x50	**CLOCKIN**	**SYNCIN**	Reserved	**DE_END**	**LINE240**	**DMODE[2:0]**		
not VLT	DRGB CLK polarity	DRGB Sync polarity	Fix to 0	Internal Sync signal	WQVGA vertical line	Panel mode		
INIT: 0x06	0: Positive 1: Negative	0: Negative 1:Positive		0: HD/VD 1: Enable	0:234line 1:240line	001:WQVGA(400x234) 010:WQVGA(480x234) 011:WQVGA(480x272) 110:WVGA (800x480)		000,100, 101, 111 : Do not use
0x51	**H_STA[7:0]**							
INIT: 0x97	Start position adjustment of digital RGB input 0000_0000: 0clk to 1111_1111: 255clk							
0x52	**V_STA[7:0]**							
INIT: 0x26	Start line adjustment of digital RGB input 0000_0000: 0line to 1111_1111: 255line							

CLOKIN : Set up polarity for input clock.
0 : Positive (Falling edge reference)
1 : Negative(Raising edge reference)

SYNCIN : Set up polarity for input HD/VD.
0 : Negative
1 : Positive
It must be same polarity for HD/VD.

DE_END : Set up internal reference sync signal.
0 : HD/VD
It has some limitation due to the phase of front porch of input HD/VD.
1 : DE back porch
In this case, it has non limitation for the phase of front porch of input HD/VD.
But the width of input HD/VD blanking, it must be kept stable.

LINE240 : Set up for 240line
0 : 234 line
1 : 240 line
This function becomes active when **DMODE [2:0]** takes [001] or [010].

DMODE[2:0] : Set up panel resolution.
001 : WQVGA（400 x 234）
010 : WQVGA（480 x 234）
011 : WQVGA（480 x 272）
110 : WVGA（800 x 480）
000、100、101、111 : Do not use.

H_STA[7:0] : Effective horizontal start position of the video signal.
0000_0000 : 0clk ～ 1111_1111 : 255clk
Set the dot numbers which is the width from leading edge of HD.

V_STA[7:0] : Effective vertical start position of the video signal.
0000_0000 : 0line ～ 1111_1111 : 255line
Set the line numbers which is the width from leading edge of VD.

6.6. Sub Address 0x59 to 0x6E (Masking for Picture Quality Improver)

Sub	D7	D6	D5	D4	D3	D2	D1	D0
0x59	**PTH_ON**	**PTH_XOR**	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	PTH pin	PTH polarity	Fix to 0	Fix to 0	Fix to 0	Fix to 0	Fix to 0	Fix to 0
INIT: 0x00	0: Active 1: non active	0: Normal 1: Reverse						
0x5A	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
INIT: 0x00	Fix to 0	Fix to 0	Fix to 0	Fix to 0	Fix to 0	Fix to 0	Fix to 0	Fix to 0
0x5B	**MASK0_ON**	**MASK0_XOR**	**MASK0_HST[9:8]**		**MASK0_HWD[9:8]**		**MASK0_ VST[8]**	**MASK0_ VWD[8]**
	MASK0 ON	MASK0 Mask area reverse	MASK0 Horizontal start position		MASK0 Horizontal width		MASK0 Vertical start position	MASK0 Vertical width
INIT: 0x00	0: OFF 1: ON	0: Normal 1: Reverse	Setting of MSB		Setting of MSB		Setting of MSB	Setting of MSB
0x5C	**MASK0_HST[7:0]**							
	MASK0 Horizontal start position							
INIT: 0x00	00_0000_0000 to 11_1111_1111: (1023clk)							
0x5D	**MASK0_HWD[7:0]**							
	MASK0 Horizontal width							
INIT: 0x00	00_0000_0000: 0clk to 11_1111_1111: (1023clk)							
0x5E	**MASK0_VST[7:0]**							
	MASK0 Vertical start position							
INIT: 0x00	0_0000_0000 to 1_1111_1111: (512 Line)							
0x5F	**MASK0_VWD[7:0]**							
	MASK0 Vertical width							
INIT: 0x00	0_0000_0000 to 1_1111_1111: (512 Line)							

＜Masking for picture quality improver＞

It can be set via external timing pulse (PTH) or 4 areas that are set by registers.
The each of 4 areas are set via MASK0, MASK1, MASK2 and MASK3.

Sub	D7	D6	D5	D4	D3	D2	D1	D0
0x60	**MASK1_ON**	**MASK1_XOR**	**MASK1_HST[9:8]**		**MASK1_HWD[9:8]**		**MASK1_ VST[8]**	**MASK1_ VWD[8]**
	MASK1 ON	MASK1 Mask area reverse	MASK1 Horizontal start position		MASK1 Horizontal width		MASK1 Vertical start position	MASK1 Vertical width
INIT: 0x00	0: OFF 1: ON	0: Normal 1: Reverse	Setting of MSB		Setting of MSB		Setting of MSB	Setting of MSB
0x61	**MASK1_HST[7:0]**							
	MASK1 Horizontal start position							
INIT: 0x00	00_0000_0000: 1st clk (Extreme left pixel) to 11_1111_1111: (1023clk)							
0x62	**MASK1_HWD[7:0]**							
	MASK1 Horizontal width							
INIT: 0x00	00_0000_0000: 0clk to 11_1111_1111: (1023clk)							
0x63	**MASK1_VST[7:0]**							
	MASK1 Vertical start position							
INIT: 0x00	0_0000_0000: 1st line (Top line) to 1_1111_1111: (512 Line)							
0x64	**MASK1_VWD[7:0]**							
	MASK1 Vertical width							
INIT: 0x00	0_0000_0000: 0Line to 1_1111_1111: (512 Line)							
0x65	**MASK2_ON**	**MASK2_XOR**	**MASK2_HST[9:8]**		**MASK2_HWD[9:8]**		**MASK2 _VST[8]**	**MASK2 _VWD[8]**
	MASK2 ON	MASK2 Mask area reverse	MASK2 Horizontal start position		MASK2 Horizontal width		MASK2 Vertical start position	MASK2 Vertical width
INIT: 0x00	0: OFF 1: ON	0: Normal 1: Reverse	Setting of MSB		Setting of MSB		Setting of MSB	Setting of MSB
0x66	**MASK2_HST[7:0]**							
	MASK2 Horizontal start position							
INIT: 0x00	00_0000_0000: 1st clk (Extreme left pixel) to 11_1111_1111: (1023clk)							
0x67	**MASK2_HWD[7:0]**							
	MASK2 Horizontal width							
INIT: 0x00	00_0000_0000: 0clk to 11_1111_1111: (1023clk)							
0x68	**MASK2_VST[7:0]**							
	MASK2 Vertical start position							
INIT: 0x00	0_0000_0000: 1st Line (Top Line) to 1_1111_1111: (512 Line)							
0x69	**MASK2_VWD[7:0]**							
	MASK2 Vertical width							
INIT: 0x00	0_0000_0000: 0Line to 1_1111_1111: 512 Line)							
0x6A	**MASK3_ON**	**MASK3_XOR**	**MASK3_HST[9:8]**		**MASK3_HWD[9:8]**		**MASK3 _VST[8]**	**MASK3 _VWD[8]**
	MASK3 ON	MASK3 Mask area reverse	MASK3 Horizontal start position		MASK3 Horizontal width		MASK3 Vertical start position	MASK3 Vertical width
INIT: 0x00	0: OFF 1: ON	0: Normal 1: Reverse	Setting of MSB		Setting of MSB		Setting of MSB	Setting of MSB
0x6B	**MASK3_HST[7:0]**							
	MASK3 Horizontal start position							
INIT: 0x00	00_0000_0000: 1st clk (Extreme left pixel) to 11_1111_1111: (1023clk)							
0x6C	**MASK3_HWD[7:0]**							
	MASK3 Horizontal width							
INIT: 0x00	00_0000_0000: 0clk to 11_1111_1111: (1023clk)							
0x6D	**MASK3_VST[7:0]**							
	MASK3 Vertical start position							
INIT: 0x00	0_0000_0000: 1st Line (Top Line) to 1_1111_1111: (512 Line)							
0x6E	**MASK3_VWD[7:0]**							
	MASK3 Vertical width							
INIT: 0x00	0_0000_0000: 0Line to 1_1111_1111: (512 Line)							

MASK0_ON：Set up Masking function.
（**MASK1_ON**、**MASK2_ON**、**MASK3_ON**）
0：OFF 1：ON

MASK0_XOR：Set up inverting function for Masking function.
（**MASK1_XOR**、**MASK2_XOR**、**MASK3_XOR**）
0：Normal
1：Reverse
Masking function becomes active for outside of Masking area.
This function is available when uses picture quality improver only for setup Masking area.

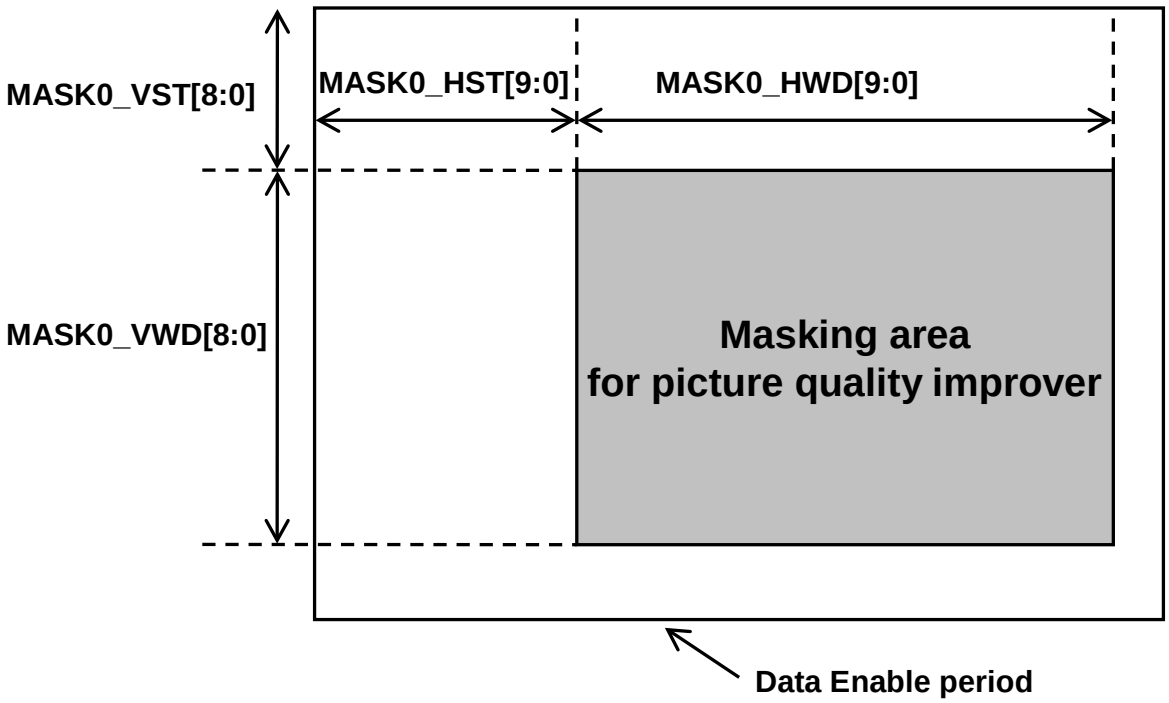
MASK0_HST[9:0]：Set up horizontal start phase for MASK0.
（**MASK1_HST[9:0]**、**MASK2_HST[9:0]**、**MASK3_HST[9:0]**）

MASK0_HWD[9:0]：Set up horizontal width for MASK0.
（**MASK1_HWD[9:0]**、**MASK2_HWD[9:0]**、**MASK3_HWD[9:0]**）

MASK0_VST[8:0]：Set up vertical start position for MASK0.
（**MASK1_VST[8:0]**、**MASK2_VST[8:0]**、**MASK3_VST[8:0]**）

MASK0_VWD[8:0]：Set up vertical width for MASK0.
（**MASK1_VWD[8:0]**、**MASK2_VWD[8:0]**、**MASK3_VWD[8:0]**）

< The image of masking function >



Segment Address 0x01

6.7. Sub Address 0x00 to 0x02 (ON-OFF of picture quality improver, Mute)

Sub	D7	D6	D5	D4	D3	D2	D1	D0
0x00	Reserved	**ENHOFF**	**CTIOFF**	**CNTBRTPS**	**CLVLPS**	**OUTBIT**	**YMUTE**	**CMUTE**
	Fix to 0	YENH	CTI	Contrast Brightness	Color level adjustment	Data output bit	Y Mute	C Mute
INIT: 0x00		0:Noraml 1:Forced OFF	0:Noraml 1:Forced OFF	0:Noraml 1:Forced OFF	0:Noraml 1:Forced OFF	0:8bit 1:6bit	0:Normal 1:YMUTE	0:Normal 1:CMUTE
0x01	**STGANPASS**	**YGANPASS**	**COMPPASS**	Reserved	Reserved	Reserved	**BBACK**	**RGB_MUTE**
	Static Y-gamma	Dynamic Y-gamma	YCCOMP	Fix to 0	Fix to 0	Fix to 0	Blue Back	RGB Mute
INIT: 0x03	0:Noraml 1:Forced OFF	0:Noraml 1:Forced OFF	0:Noraml 1:Forced OFF				0:Normal 1:Blue back	0:Normal 1:MUTE
0x02	**RGB_ CNTBRTPS**	**BMASKPS**	**CMPS**	Reserved	Reserved	Reserved	Reserved	Reserved
	PICT CNT/BRT	Back Mask	Color Management	Fix to 0	Fix to 0	Fix to 0	Fix to 0	Fix to 0
INIT: 0x00	0:Noraml 1:Forced OFF	0:Noraml 1:Forced OFF	0:Noraml 1:Forced OFF					

The register for forced-off function and the target picture process function

Register	Function
ENHOFF	Sharpness, LTI, YNC
CTIOFF	CTI, CNC
CNTBRITPS	Contrast, Brightness
CLVLPS	Cb/Cr gain, Cb/Cr offset
STGANPASS	Static Y-gamma correction
YGANPASS	Dynamic Y-gamma correction
COMPPASS	C gain compensated with Y-gamma
RGB_CNTBRTPS	Picture RGB contrast Picture RGB brightness
CMPS	Color management Skin color correction, Tint

OUTBIT：Set up bit range of RGB output signals.
0：RGB 8bit output
1：RGB 6bit output

YMUTE：Set up Mute function for Y signal.
(Note): this function is not available for masking area.

CMUTE：Set up Mute function for C signal.
(Note): this function is not available for masking area.

BBACK：Set up Blue back function.
This function can blue back for overall picture area.
The color of blue back is set via registers **BBACK_R[3:0]**、**BBACK_G[3:0]**、**BBACK_B[3:0]**（Seg.0x01 Sub.0x6D to 0x6F）. It can set other color in addition to blue.

RGB_MUTE：Set up Mute function for RGB signal.
This function works all of picture area.

6.8. Sub Address 0x04 to 0x07 (Sharpness, LTI, YNC)

Sub	D7	D6	D5	D4	D3	D2	D1	D0
0x04	Reserved	**ENHLIM[2:0]**			**ENHGA[2:0]**			**FENH**
	Fix to 0	Sharpness1 Coring level			Sharpness1 Gain			Sharpness1 f0
INIT: 0x00		000:0LSB to 111:7LSB (1LSB step @8bit)			000:OFF 001: x0.125% to 111: x0.875%			0:PANEL_CLK/4 1:PANEL_CLK/2
0x05	Reserved	**ENHLIM2[2:0]**			**ENHGA2[2:0]**			**FENH2**
	Fix to 0	Sharpness2 Coring level			Sharpness2 gain			Sharpness2 f0
INIT: 0x00		000:0LSB to 111:7LSB (1LSB step @8bit)			000:OFF 001: x0.125% to 111: x0.875%			0:PANEL_CLK/8 1:PANEL_CLK/6
0x06	Reserved	**LTILIM[2:0]**			**LTIGA[2:0]**			**FLTI**
	Fix to 0	LTI Coring			LTI Gain			LTI f0
INIT: 0x00		000:0LSB to 111:7LSB (1LSB step @8bit)			000:OFF 001: x0.125% to 111: x0.875%			0:PANEL_CLK/6 1:PANEL_CLK/4
0x07	Reserved	**NCLIM[2:0]**			**NCGA[1:0]**		**FNC[1:0]**	
	Fix to 0	YNC Coring			YNC gain		YNC f0	
INIT: 0x00		000:0LSB to 111:7LSB (1LSB step @8bit)			00:OFF 01:*0.125% to 11:*0.5%		00:PANEL_CLK/8 01:PANEL_CLK/6	10:PANEL_CLK/4 11:PANEL_CLK/2

＜Sharpness function＞ （04H、05H）
This function is horizontal Y edge enhancer. It adds shoot to enhance Y edge.

ENHLIM[2:0]：Set up Coring level for sharpness 1.
000：0LSB ～ 111：7LSB (8bit process)
When the value of horizontal Y edge is lower than setup level, Sharpness function will be masking.
ENHGA[2:0]：Set up sharpness 1 gain for horizontal edge portion of Y.
000：OFF 001：minimum gain ～ 111：maximum gain
FENH：Set up f0 for sharpness 1
0：PANEL_CLK/4 1：PANEL_CLK/2
ENHLIM2[2:0]：Set up Coring level for sharpness 2.
000：0LSB ～ 111：7LSB (8bit process)
When the value of horizontal Y edge is lower than setup level, Sharpness function will be masking.
ENHGA2[2:0]：Set up sharpness gain 2 for horizontal edge portion of Y.
000：OFF 001：minimum gain ～ 111：maximum gain
FENH2：Set up f0 for sharpness 2.
0：PANEL_CLK/8 1：PANEL_CLK/6

＜LTI function＞ （06H）
This function is horizontal Y edge enhancer.
LTI can enhance Y edge to make a steep slope for it without adding shoot.

LTILIM[1:0]：Set up Coring level for LTI.
000：0LSB ～ 111：7LSB (8bit process)
When the value of horizontal Y edge is lower than setup level, LTI function will be masking.

LTIGA[2:0]：Set up LTI gain.
000：OFF 001：minimum gain ～ 111：maximum gain

FLTI：Set up f0 for LTI.
0：PANEL_CLK/6 1：PANEL_CLK/4

＜YNC function＞ （07H）
This function suppresses horizontal Y edge.
It can noise cancel for small edge to make a minus gain in edge enhance processing.
(Note): when use strong gain, it becomes blurry picture at overall screen.

NCLIM[2:0]：Set up Coring level.
000：0LSB ～ 111：7LSB (8bit process)
It will make an opposite enhance processing for edge that smaller than setup level.
NCGA[1:0]：Set up gain for Coring function.
00：OFF 01：minimum gain ～ 11：maximum gain
FNC[1:0]：Set up f0 for Coring function.
00：wide band ～ 11：narrow band

6.9. Sub Address 0x08 to 0x09 (Brightness, Contrast)

Contrast adjustment and Brightness adjustment for Y signal.

Sub	D7	D6	D5	D4	D3	D2	D1	D0
0x08	Reserved	**ADJCONT[6:0]**						
	Fix to 0	Contrast of Y						
INIT: 0x40		000_0000: x0 to 100_0000: x1 to 111_1111: x1.98						
0x09	Reserved	**ADJBRIT[6:0]**						
	Fix to 0	Brightness of Y						
INIT: 0x00		100_0000:-64LSB to 000_0000:0LSB to 011_1111:+63LSB (@8bit, 1LSB step)						

6.10. Sub Address 0x0A to 0x0B (CTI, CNC)

Sub	D7	D6	D5	D4	D3	D2	D1	D0
0x0A	Reserved	**CTILIM[2:0]**			**CTIGA[2:0]**			**FCTI**
	Fix to 0	CTI Coring			CTI Gain			CTI f0
INIT: 0x00		000:0LSB to 111:7LSB (1LSB step @8bit)			000:OFF 001: x0.250% to 111: x1.750%			0:PANEL_CLK/6 1:PANEL_CLK/4
0x0B	Reserved	**CNCLIM**			**CNCGA**		**FCNC[1:0]**	
	Fix to 0	CNC Coring			CNC Gain		CNC f0	
INIT: 0x00		000:0LSB to 111:7LSB (1LSB step @8bit)			00:OFF 01: x0.125% to 11: x0.5%		00:PANEL_CLK/8 01:PANEL_CLK/6	10:PANEL_CLK/4 11:PANEL_CLK/2

＜CTI function＞
This function is horizontal C edge enhancer.
CTILIM[2:0]：Set up Coring level.
000：0LSB ～ 111：7LSB（8bit process）
When the value of C edge is lower than setup level, CTI function will be masking.

CTIGA[2:0]：Set up Coring level.
000：OFF 001：：minimum gain ～ 111：maximum gain
FCTI： Set up f0 for CTI.
0：PANEL_CLK/6 1：PANEL_CLK/4

＜Coring function for C＞
This function suppresses horizontal C edge.
It can noise cancel for small edge to make a minus gain processing.
000：0LSB ～ 111：7LSB (8bit process)
CNCGA[1:0]：Set up Coring gain.
00：OFF 01：minimum gain ～ 11：maximum gain
FCNC[1:0]： Set up f0 for Coring function.
00：Wide band ～ 11：Narrow band

6.11. Sub Address 0x0C to 0x0F (C gain, Cb/Cr offset, C gain compensation with Y-gamma)

Sub	D7	D6	D5	D4	D3	D2	D1	D0
0x0C	**CGAIN[7:0]**							
	C gain							
INIT: 0x40	0000_0000:*0 to 0100_0000:*1 to 1111_1111:*3.98							
0x0D	**COMPSW[1]**	**CBOFS[6:0]**						
	Coefficient for (-) correction	Cb offset						
INIT: 0x00		100_0000:-64LSB to 000_0000:0LSB to 011_1111:+63LSB (@8bit, 1LSB)						
0x0E	**COMPSW[0]**	**CROFS[6:0]**						
	Coefficient for (-) correction	Cr offset						
INIT: 0x00	00: 1/8 01: 1/4 10: 1/2 11: 1/1	100_0000:-64LSB to 000_0000:0LSB to 011_1111:+63LSB (@8bit, 1LSB)						
0x0F	**COMPDLYSEL**	**COMPGA[6:0]**						
	Reference source for C gain correction	YCCOMP Gain						
INIT: 0x00	0: static+ Dynamic-γ 1: Dynamic-γ	000_0000:*0 to 111_1111:*7.9375						

CGAIN[7:0] : Color gain.
CBPFS[6:0] : Offset adjustment for Cb.
CRPFS[6:0] : Offset adjustment for Cr.

< Correction C gain linked Y-gamma function >
This function is color level correction to link with the Y level that is corrected by Y-γ correction.

COMPGA[6:0] : Set up C gain for C gain correction linked Y-γ.
000_0000 : Off 000_0001 : minimum gain ～ 111_1111 : maximum gain

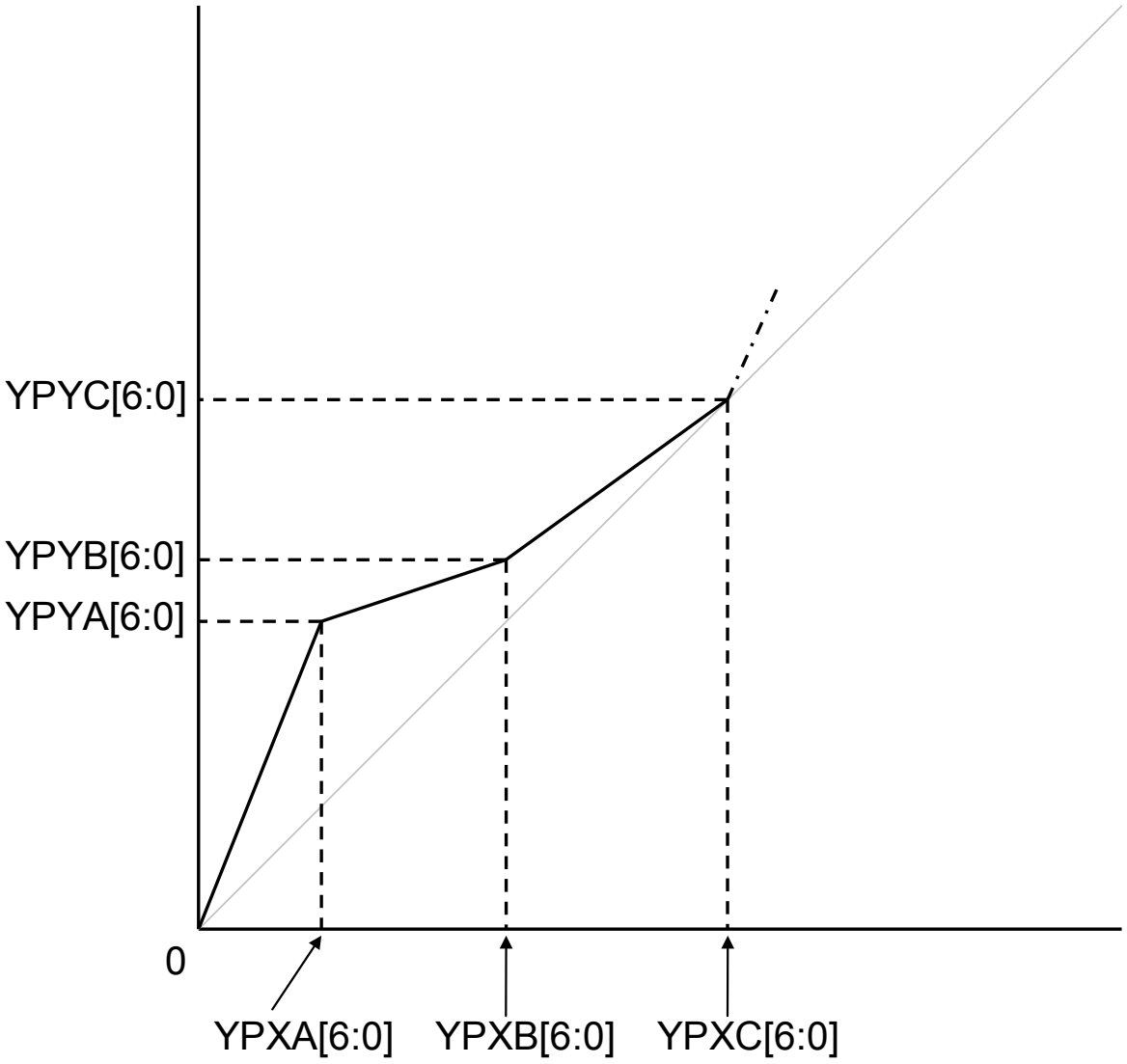
COMPSW[1:0] : Set up minus compensation for C gain correction linked Y-γ.
00 : x 1/8 01 : x 1/4 10 : x 1/2 11 : x 1
This function is to suppress fade in color at minus correction for Y-γ.
11→00 : The correction value for C gain, it takes half value step by step at minus correction linked Y-γ.

COMDLYSEL : Select Y-γ function for C gain correction as a reference
0 : Static gamma + Dynamic gamma correction 1 : Dynamic gamma

6.12. Sub Address 0x10 to 0x1F (Static Y-gamma correction)

Sub	D7	D6	D5	D4	D3	D2	D1	D0
0x10	Reserved	**YPXA[6:0]**						
		Static Y-gamma correction A X axis						
INIT: 0x0F	Fix to 0	000_0000: 1LSB to 000_1111: 31LSB to 111_1111: 255LSB (2LSB step)						
0x11	Reserved	**YPYA[6:0]**						
		Static Y-gamma correction A Y axis						
INIT: 0x0F	Fix to 0	000_0000: 1LSB to 000_1111: 31LSB to 111_1111: 255LSB (2LSB step)						
0x12	Reserved	**YPXB[6:0]**						
		Static Y-gamma correction B X axis						
INIT: 0x1F	Fix to 0	000_0000: 1LSB to 001_1111: 63LSB to 111_1111: 255LSB (2LSB step)						
0x13	Reserved	**YPYB[6:0]**						
		Static Y-gamma correction B Y axis						
INIT: 0x1F	Fix to 0	000_0000: 1LSB to 001_1111: 63LSB to 111_1111: 255LSB (2LSB step)						
0x14	Reserved	**YPXC[6:0]**						
		Static Y-gamma correction C X axis						
INIT: 0x2F	Fix to 0	000_0000: 1LSB to 010_1111: 95LSB to 111_1111: 255LSB (2LSB step)						
0x15	Reserved	**YPYC[6:0]**						
		Static Y-gamma correction C Y axis						
INIT: 0x2F	Fix to 0	000_0000: 1LSB to 010_1111: 95LSB to 111_1111: 255LSB (2LSB step)						
0x16	Reserved	**YPXD[6:0]**						
		Static Y-gamma correction D X axis						
INIT: 0x3F	Fix to 0	000_0000: 1LSB to 011_1111: 127LSB to 111_1111: 255LSB (2LSB step)						
0x17	Reserved	**YPYD[6:0]**						
		Static Y-gamma correction D Y axis						
INIT: 0x3F	Fix to 0	000_0000: 1LSB to 011_1111: 127LSB to 111_1111: 255LSB (2LSB step)						
0x18	Reserved	**YPXE[6:0]**						
		Static Y-gamma correction E X axis						
INIT: 0x4F	Fix to 0	000_000: 1LSB to 100_1111: 159LSB to 111_1111: 255LSB (2LSB step)						
0x19	Reserved	**YPYE[6:0]**						
		Static Y-gamma correction E Y axis						
INIT: 0x4F	Fix to 0	000_0000: 1LSB to 100_1111: 159LSB to 111_1111: 255LSB (2LSB step)						
0x1A	Reserved	**YPXF[6:0]**						
		Static Y-gamma correction F X axis						
INIT: 0x5F	Fix to 0	000_0000: 1LSB to 101_1111: 191LSB to 111_1111: 255LSB (2LSB step)						
0x1B	Reserved	**YPYF[6:0]**						
		Static Y-gamma correction F Y axis						
INIT: 0x5F	Fix to 0	000_0000: 1LSB to 101_1111: 191LSB to 111_1111: 255LSB (2LSB step)						
0x1C	Reserved	**YPXG[6:0]**						
		Static Y-gamma correction G X axis						
INIT: 0x6F	Fix to 0	000_0000: 1LSB to 110_1111: 223LSB to 111_1111: 255LSB (2LSB step)						
0x1D	Reserved	**YPYG[6:0]**						
		Static Y-gamma correction G Y axis						
INIT: 0x6F	Fix to 0	000_0000: 1LSB to 110_1111: 223LSB to 111_1111: 255LSB (2LSB step)						
0x1E	Reserved	**YPXH[6:0]**						
		Static Y-gamma correction H X axis						
INIT: 0x7F	Fix to 0	000_0000: 1LSB to 111_1111: 255LSB (2LSB step)						
0x1F	Reserved	**YPYH[6:0]**						
		Static Y-gamma correction H Y axis						
INIT: 0x7F	Fix to 0	000_0000: 1LSB to 111_1111: 255LSB (2LSB step)						

< Static Y-gamma correction >
The start point is input 0LSB and output 0LSB.
It can set 8 point of inflection. (See diagram below.)
Input and output setting: 2LSB step.



6.13. Sub Address 0x20 to 0x22, 0x32 to 0x3E (Dynamic Y-gamma correction)

Sub	D7	D6	D5	D4	D3	D2	D1	D0
0x20	Reserved	Reserved	Reserved	**DYGANMA1[4:0]**				
	Fix to 0	Fix to 0	Fix to 0	Dynamic Y-gamma (dark portion) gain 1_0000: x0 to 0_0000: x1 to 0_1111: x1.94 (1/16 step)				
INIT: 0x00								
0x21	Reserved	Reserved	Reserved	**DYGANMA2[4:0]**				
	Fix to 0	Fix to 0	Fix to 0	Dynamic Y-gamma (light portion) gain 1_0000: x0 to 0_0000: x1 to 0_1111: x1.94 (1/16 step)				
INIT: 0x00								
0x22	Reserved	Reserved	Reserved	**YGARANGE**	**DYGANSW[3:0]**			
	Fix to 0	Fix to 0	Fix to 0	Correction range 0: 0-1023 1: 64-944 (0-100IRE)	Light portion control 0*: Normal 10: gain up 11: gain down		Dark potion control 0*: Normal 10: gain down 11: gain up	
INIT: 0x00								

< Dynamic Y-gamma correction>

DYGANMA1[4:0]：Set up gain for Dynamic Y-gamma for dark portion.
Recommendation value：0x16

DYGANMA2[4:0]：Set up gain for Dynamic Y-gamma for light portion.
Recommendation value：0x16

DYGANSW[3:2]：Set up the direction for correction at light portion Dynamic Y-gamma.
Recommendation value：00
00 or 01：Both direction (level up / down Y)
10： Gain up（level up Y）
11： Gain down (level down Y)

DYGANSW [1:0]: Set up the direction for correction at dark portion Dynamic Y-gamma.
Recommendation value：00
00 or 01： Both direction (level up / down Y)
10： Gain down (level down Y)
11： Gain up (level up Y)

Sub	D7	D6	D5	D4	D3	D2	D1	D0
0x32	Reserved		Reserved	**DYGAINTG**	**DYGASW[3:0]**			
	Fix to 0		Fix to 0	Detection value integral	D-γ light / dark detection select	Correction mode		Gamma correction
INIT: 0x00				0: OFF 1: ON	0: Before D-γ 1: After D-γ	00: OFF 01:0-12.5-25%	10: 0-25-50% 11: 0-50-100%	0:continuous 1:divide
0x33	**DYG1DEG[2:0]**			**DYG1IRE[2:0]**			**DYG1SW[1:0]**	
	Dark portion detection range			Dark portion detection threshold			Dark portion D-γ	
INIT: 0x00	000: 3.63IRE to 111: 58.2IRE			000: 0IRE to 111: 25.5IRE			Fix to 0	0:OFF 1:ON
0x34	**DYG1GAN[2:0]**			**DYG1SFT[2:0]**			**DYG1SW[3:2]**	
	Dark portion gain range			Dark portion level range			Detect Dark portion D-γ	
INIT: 0x00	000: 3.125% to 111: 50%			000: 0% to 111: 21.88%			0: Input Y 1: After St-γ	Fix to 0
0x35	**DYG1SPU[7:0]**							
	Dark portion control rising time constant							
INIT: 0x00	0000_0000:Slow to 1111_1111: Fast							
0x36	**DYG1SPD[7:0]**							
	Dark portion control falling time constant							
INIT: 0x00	0000_0000: Slow to 1111_1111: Fast							
0x37	**DYG2DEG[2:0]**			**DYG2IRE[2:0]**			**DYG2SW[1:0]**	
	Light portion detection range			Light portion detection threshold			Light portion D-γ	
INIT: 0x00	000: -3.63IRE to 111: -58.2IRE			000: 100IRE to 111: 74.5IRE 3.57 IRE Step			Fix to 0	0:OFF 1:ON
0x38	**DYG2GAN[2:0]**			**DYG2SFT[2:0]**			**DYG2SW[3:2]**	
	Light portion gain range			Light portion level range			Detect Light portion D-γ	
INIT: 0x00	000: 3.125% to 111: 50%			000: 0% to 111: 21.88%			0: Input Y 1: After St-γ	Fix to 0
0x39	**DYG2SPU[7:0]**							
	Light portion control rising time constant							
INIT: 0x00	0000_0000:Slow to 1111_1111: Fast							
0x3A	**DYG2SPD[7:0]**							
	Light portion control falling time constant							
INIT: 0x00	0000_0000:Slow to 1111_1111: Fast							

0x3B	**DYGA_DISP[0]**	**DYGA_VST[6:0]**
	Detection area limit	Vertical start position of detection area for dynamic Y-gamma
INIT: 0x00	0: OFF 1: ON	000_0000: 1st line to 111_1111: 509th line (4Lines step)
0x3C	**DYGA_DISP[1]**	**DYGA_VWD[6:0]**
	Detection display (darker)	Vertical width of detection area for dynamic Y-gamma
INIT: 0x00	0: OFF 1: ON	000_0000: 0Line to 111_1111: 508Lines (4Lines step)
0x3D	**DYGA_DISP[2]**	**DYGA_HST[6:0]**
	Detection display (lighter)	Horizontal start position of detection area for dynamic Y-gamma
INIT: 0x00	0: OFF 1: ON	000_0000: 1st clk to 111_1111: 1017th clk (8clks step)
0x3E	Reserved	**DYGA_HWD[6:0]**
	Fix to 0	Horizontal width of detection area for dynamic Y-gamma
INIT: 0x00		000_0000: 0clk to 111_1111: 1016clks (8clks step)

6.13.1. A sample setting of dynamic gamma

Sub address 0x32 to 0x3A: These registers are to setup Luminance detection and time constant for Dynamic Y-γ. Please use the recommendation value for Dynamic Y-γ as shown below.

Sub Address	Recommended data	Functions	Remarks
0x32	0x10	Detection mode setting	DYGAINTG: Recommended value is 1.
0x33	0xE1	Dark portion dynamic gamma setting 1	It must be changed 0xE0 to set off the dark portion Dynamic Y-γ.
0x34	0xE0	Dark portion dynamic gamma setting 2	-
0x35	0x90	Dark portion control rising time constant	It must be used same value.
0x36	0x90	Dark portion control falling time constant	
0x37	0xF1	Light portion dynamic gamma setting 1	It must be changed 0xF0 to set off the light portion Dynamic Y-γ.
0x38	0xFC	Light portion dynamic gamma setting 2	-
0x39	0x88	Light portion control rising time constant	It must be used same value.
0x3A	0x88	Light portion control falling time constant	

6.13.2. Limit function for detection area of dynamic Y-gamma correction

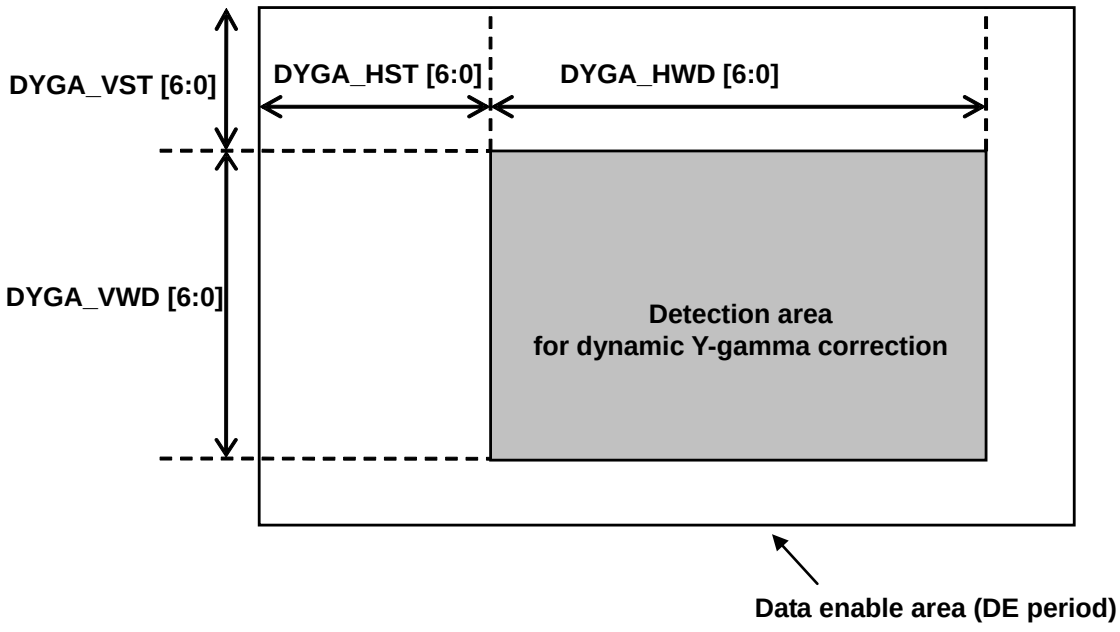
0x3C～0x3F：Set up limit function for detection area of light portion Dynamic Y-γ and dark portion Dynamic Y-γ.

DYGA_DISP[0]： ON/OFF selection for detection area setting function.
0：OFF 1：ON

DYGA_DISP[1]：Monitor for the detection area of dynamic Y gamma (Dark portion).
0：OFF
1：ON It becomes dark for the area which is set via DYGA_VST[6:0], DYGA_VWD [6:0, DYGA_HST [6:0], and DYGA_HWD [6:0].

DYGA_DISP[2]：Monitor for the detection area of dynamic Y gamma (Light portion).
0：OFF
1：ON It becomes light for the area which is set via, DYGA_VST[6:0], DYGA_VWD [6:0], DYGA_HST [6:0], DYGA_HWD [6:0].

DYGA_VST[6:0]、DYGA_VWD[6:0]、DYGA_HST[6:0]、DYGA_HWD[6:0]
Set up the detection area for Dynamic Y-γ.
(Refer to the figure as shown below.)



6.14. Sub Address 0x2C to 0x32 (APL detection)

Sub	D7	D6	D5	D4	D3	D2	D1	D0
0x2C	**APL_DISP[0]**	**APL_VST[6:0]**						
	Set Detection area	Vertical start line of APL detection area						
INIT: 0x00	0: OFF 1: ON	000_0000: 1st Line to 111_1111: 509th Line (4Line step)						
0x2D	**APL_DISP[1]**	**APL_VWD[6:0]**						
	Display detection area(dark)	Vertical width of APL detection area						
INIT: 0x00	0: OFF 1: ON	000_0000: 0Line to 111_1111: 508Line (4Lines step)						
0x2E	**APL_DISP[2]**	**APL_HST[6:0]**						
	Display detection area(light)	Horizontal start position of APL detection area						
INIT: 0x00	0: OFF 1: ON	000_0000: 1st clk (Extreme left pixel) to 111_1111: 1017th clk (8clks step)						
0x2F	Reserved	**APL_HWD[6:0]**						
	Fix to 0	Horizontal width of APL detection area						
INIT: 0x00		000_0000: 0clk to 111_1111: 1016clks (8clks step)						
0x30	**APL_SW[7:0]**							
	APL detection							
INIT: 0x00	Fix to 0	Fix to 0	Fix to 0	Fix to 0	Select Y signal 00: After HVD enhance 10:after Dynamic Y- γ 11:After Contrast/ Brightness	Fix to 0		0: OFF 1: ON
0x31	**APL_GAIN[7:0]**							
	APL Detection time constant							
INIT: 0x00	0000_0000: Slow to 1111_1111: Fast							

6.14.1. APL detection function setting

APL detection is set via sub address 0x2C to 0x31.

APL_SW [0]: APL detection function ON/OFF.
0: OFF (default) 1: ON
In regardless of ON/OFF of APL_SW [0], the value of APL detection is outputted at sub address 0x50 to 0x51 as read data.
In case using PWM function simultaneously with the value of APL detection, please set ON for APL_SW[0].

APL_SW [3:2]: Select Y signal for APL detection.
00: After HVD enhance
10: After Dynamic Y- γ
11: After Contrast/ Brightness

APL_GAIN [7:0]: Set up time constant for APL detection.
0000_0000: slow
1111_1111: fast
In case of using smaller APL detection area that is set via 0x2C to 0x30, the tracking of APL detection has tendency slow.
Therefore it is recommended to use big value for **APL_GAIN [7:0]**.

6.14.2. APL detection area setting function (Seg.0x04 Sub Address 0x2C to 0x2F)

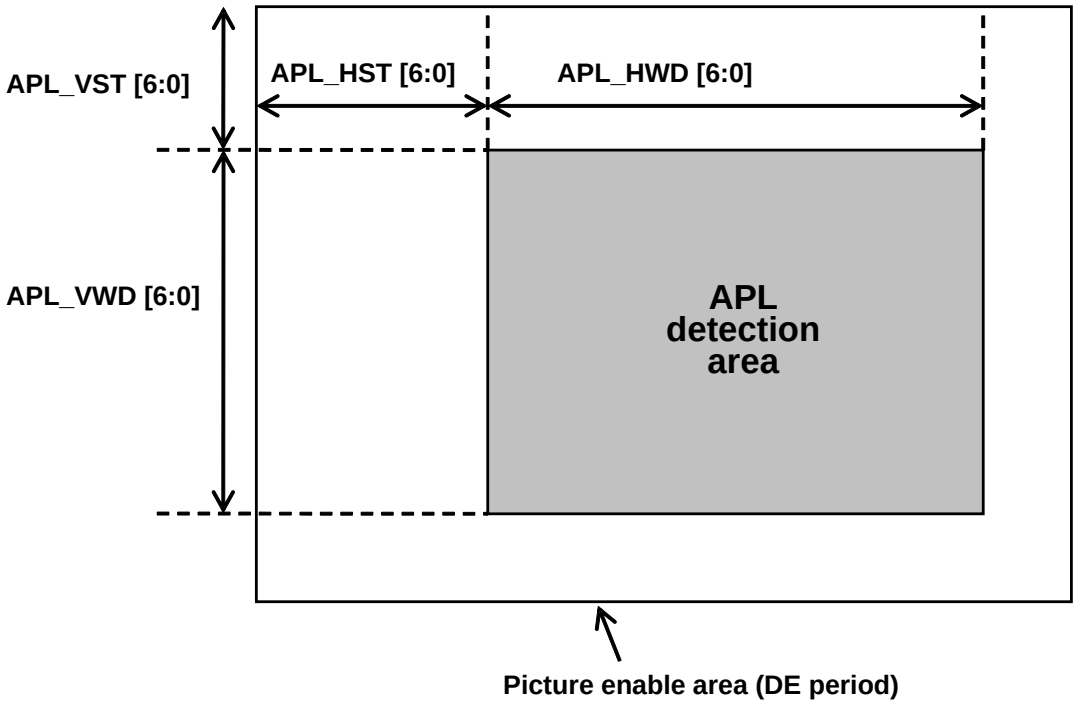
It can limit for APL detection area via sub address 0x2C to 0x2F.

APL_DISP [0]: APL detection function area setting function ON/OFF.
0: OFF (default)
1: ON (area setting by **APL_VST**, **DYGA_VWD**, **DYGA_HST**, **and DYGA_HWD**)

APL_DISP [1]: Display monitor the APL detection area (indicate dark).
0: OFF 1: ON

APL_DISP [1]: Display monitor the APL detection area (indicate light).
0: OFF 1: ON

APL_VST [6:0], **DYGA_VWD [6:0]**, **DYGA_HST [6:0]**, **DYGA_HWD [6:0]**
It can set the APL detection area via these registers.



6.15. Sub Address 0x50 to 0x55

(APL detection/ Dynamic Y-gamma detection of correction gain: Read only)

Sub	D7	D6	D5	D4	D3	D2	D1	D0
0x50 Read only	**RD_APLDET[9:2]**							
	APL detection value (read only)							
0x51 Read only	**RD_APLDET[1:0]**		Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	APL detection value (read only)		Fix to 0	Fix to 0	Fix to 0	Fix to 0	Fix to 0	Fix to 0
0x52 Read only	**RD_DYNAG1DET[8:1]**							
	Dark portion Y dynamic gamma gain detection value (read only)							
0x53 Read only	**RD_DYNAG1DET[0]**	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	Dark portion dynamic gamma gain detection value (read only)	Fix to 0	Fix to 0	Fix to 0	Fix to 0	Fix to 0	Fix to 0	Fix to 0
0x54 Read only	**RD_DYNAG2DET[8:1]**							
	Light portion Y dynamic gamma gain detection value (read only)							
0x55 Read only	**RD_DYNAG2DET[0]**	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	Light portion dynamic gamma gain detection value (read only)	Fix to 0	Fix to 0	Fix to 0	Fix to 0	Fix to 0	Fix to 0	Fix to 0

These registers (0x50 ~ 0x55) are read only.
Therefore do not write data to these registers.
So, these registers have the data of APL detection, dark portion dynamic Y-γ gain detection and Light portion dynamic Y-γ gain detection.
These data can be used for correction the PWM.

6.16. Sub Address 0x26 to 0x29 (PWM output setting of DIMMER terminal)

Sub	D7	D6	D5	D4	D3	D2	D1	D0
0x26	**PWM_SW[7:2]**						**PWM_NP**	**PWM_VLAT**
	PWM ON/OFF	interlock mode	Polarity correction	Configu ration	interlock mode signal select		Output Polarity	V latch
	0: OFF	0: OFF (normal)	0: +	0: STR (0)	00: APL	10: Dynamic gamma (light)	0: normal	0: OFF
INIT: 0x00	1: ON	1: ON	1: -	1: 2's	01: Dynamic gamma (dark)	11: not supported	1: reverse	1: ON
0x27	**PWM_GAIN[3:0]**				**PWM_DUTY[11:0]**			
	GAIN setting for interlock mode				DUTY setting (bit [11:8])			
INIT: 0x00	0000: x0.25 to 0011: x1.00 to 1111: x4.00				(refer to x28)			
0x28	**PWM_DUTY[11:0]**							
	DUTY setting (bit [7:0])							
INIT: 0x00	0000_0000_0000: 0.24% to 0111_1111_1111: 50% to 1111_1111_1111: 100.00%							
0x29	**PWM_SW[1:0]**		**PWM_DIV[5:0]**					
	PWM resolution		PWM divider setting					
	00: 1/2048	10: 1/8192	00_0000: x1 to 11_1111: x64					
INIT: 0x00	01: 1/4096	11: 1/16384						

PWM pulse at DIMMER terminal is set via sub address 0x25 to 0x29.
It can control not only static duty and also adaptive duty that is interlocked with APL detection, dark portion/light portion dynamic Y-γ gain detection.

PWM_SW [7]: Set up PWM output ON/OFF
0：OFF 1：PWM output

PWM_SW [6]: Set up interlock PWM with APL detection and dynamic Y-γ gain detection.
0：OFF 1：ON

PWM_SW [5]: Set up polarity of correction for interlocked PWM mode of PWM.
0：Adding correction (+) 1：Subtraction correction (-)

PWM_SW [4]: Set up configuration of the detection value
0：Strait binary 1：2's complement

PWM_SW [3:2]: Select the detection value to correct PWM.
00：APL detection
01：Dark portion Dynamic Y gamma gain detection value
10：Light portion Dynamic Y gamma gain detection value
11：do not use

PWM_NP: Set up polarity for PWM output
0：Normal (0%=Low., 100%=High) 1：Invert (0%=High, 100%=Low)

PWM_VLAT: Select V latch to capture the detection value for correction PWM.
Usually uses default.
0：V latch OFF(default) 1：V latch ON

PWM_GAIN [3:0]: Set up gain for detection value that corrects PWM.
0000：x 0.25, 0001:x 0.50, 0010:x 0.75, 0011: x1.00 ～ 1111: x4 (0.25 step)

PWM_DUTY [11:0]: Set up the duty of PWM output
0000_0000_0000(0.24%) - 0111_1111_1111 （50%） - 1111_1111_1111(100.00%)

PWM_DIV [5:0]: Set up the ratio of dividing panel clock to fine tune PWM output frequency.
PWM output frequency is determined by PWM_DIV [5:0] and PWM_SW [1:0].
00_0000: 1 ～ 11_1111: 64

PWM_SW[1:0]: Set up the base frequency for PWM output.
The value indicates the numbers of clock in 1 cycle of PWM output.
This register gives tradeoff for the PWM performance as shown below.
Set up bigger value => Output frequency: Low Accuracy of control: High
Set up smaller value => Output frequency: High Accuracy of control: Low
00: 2048 (11bit resolution)
01: 4096 (12bit resolution)
10: 8192 (13bit resolution)
11: 16384(14bit resolution)

（Note A）
PWM output frequency is defined by panel clock and register setting of **PWM_DIV[5:0]** and **PWM_SW [1:0]**.

When the panel clock frequency shows (A), the PWM output frequency (B) is shown the Calculation formula as indicated below.
(B) = (A) ÷ **PWM_SW** ÷ **PWM_DIV**

Ex) In the case of panel clock: 33.3MHz, the maximum and minimum frequency are calculated as follows.
max.: 33.3[MHz] ÷ 2048 ÷ 1 = 16.26[kHz] (11bit resolution)
min.: 33.3[MHz] ÷ 16384 ÷ 64 = 31.76[Hz] (14bit resolution)

（Note B）
・The DIMMER terminal initial condition is Low.
・The DIMMER terminal is not open drain. Then it cannot be used as pull up.
・The duty of PWM output, it cannot be set 0% at the register **PWM_DUTY [11:0].**
When use 0% setting, set the polarity Normal and out put OFF (**PWM_NP**=0, **PWM_SW [7]** =0).
・It cannot set up the time constant for the duty displacement at interlocked PWM mode.
The time constant is set up by the each of register APL detection or Dynamic Y-γ.

6.17. Sub Address 0x60 to 0x69 (Color management, Skin color correction, Tint)

Sub	D7	D6	D5	D4	D3	D2	D1	D0
0x60	**GAIN1[7:0]**							
	Color management1 (1st color phase) gain setting							
INIT: 0x00	1000_0000: gain max (color attenuation) to 0000_0000: OFF to 0111_1111: gain max (color amplitude)							
0x61	**GAIN2[7:0]**							
	Color management 2 (2nd color phase) gain setting							
INIT: 0x00	1000_0000: gain max (color attenuation) to 0000_0000: OFF to 0111_1111: gain max (color amplitude)							
0x62	**GAIN3[7:0]**							
	Color management3 (3rd color phase) gain setting							
INIT: 0x00	1000_0000: gain max (color attenuation) to 0000_0000: OFF to 0111_1111: gain max (color amplitude)							
0x63	**PH1[7:0]**							
	Color management1 (1st color phase) center color phase setting							
INIT: 0x00	0x00: Cb(+) axis to 0x40: Cr(+) axis to 0x80: Cb(-) axis to 0xC0: Cr(-) axis to 0x00: Cb(+) axis							
0x64	**PH2[7:0]**							
	Color management2 (2nd color phase) center color phase setting							
INIT: 0x00	0x00: Cb(+) axis to 0x40: Cr(+) axis to 0x80: Cb(-) axis to 0xC0: Cr(-) axis to 0x00: Cb(+) axis							
0x65	**PH3[7:0]**							
	Color management3 (3rd color phases) center color phase setting							
INIT: 0x00	0x00: Cb(+) axis to 0x40: Cr(+) axis to 0x80: Cb(-) axis to 0xC0: Cr(-) axis to 0x00: Cb(+) axis							
0x66	**COLMON**	Reserved	**WIN3[1:0]**		**WIN2[1:0]**		**WIN1[7:0]**	
	Color management	Fix to 0	surrounding color phase range for 3rd color phase		surrounding color phase range for 2nd color phase		surrounding color phase range for 1st color phase	
INIT: 0x00	0: OFF 1: ON		00: ±22.5° 1*: ±90° 01: ±45°		00: ±22.5° 1*: ±90° 01: ±45°		00: ±22.5° 1*: ±90° 01: ±45°	
0x67	**FRON**	**RNFROFF**	**LIM_FR[2:0]**			**GAIN_FR[2:0]**		
	Skin color correction	Skin color correction C mute	Skin color correction Correction range of Chroma level			Skin color correction Gain setting		
INIT: 0x00	0: OFF 1: ON	0: OFF 1: ON	000: OFF 001: min range to 111: max range			000: OFF 001: min to 111: max		
0x68	Reserved	**RN1OFF**	**RN2OFF**	**RN3OFF**	**WIN_FR**	**PH_FR[2:0]**		
	Fix to 0	1st axis C mute	2nd axis C Mute	3rd axis C Mute	Skin color correction Phase wide	Skin color Center phase adjustment		
INIT: 0x00		0: OFF 1: ON	0: OFF 1: ON	0: OFF 1: ON	0: ±22.5° 1: ±45°	100:for red to 000:Center to 011:for green 2.8° step		
0x69	**TINT[7:0]**							
	TINT adjustment							
INIT: 0x00	1111_1111: -44.8° to 1000_0000: -0.35° to 0000_0000: ±0° to 0111_1111: +44.45° 0.35° step							

＜Color management function＞

In this function, it can enhance color level at the specific color phase (axis) and surrounding color phase of it. It can set up 3 of specific color phase arbitrarily.

RN1OFF：Set up Color MUTE function to monitor the area of Color management1 (1st color phase)
0：OFF 1：MUTE ON
1：It can mute the color for Color management1 (1st color phase) only.

GAIN1[7:0]：Set up the gain of color level for Color management1 (1st color phase)
0x80：maximum attenuation color level ～ 0x00：gain off ～ 0x7F：maximum gain
Note: use of **GAIN1 [7] =1**, it means attenuation.

PH1[7:0]：Set up the center axis of Color management1 (1st color phase)
0x00：Cb(+) ～ 0x40：Cr(+) ～ 0x80：Cb(-) ～ 0xC0：Cr(-) ～ 0x00：Cb(+)
It can set 1.4° step.

WIN1[1:0]：Set up the phase area of correction for Color management1 (1st color phase)
00：±22.5° 01：±45° 1*：±90°
The color correction becomes effective for the area which is set Color management1 (1st color phase) as a center of the color phase.

＜Skin color correction＞
In addition to color management, it is available to use skin color correction.

FRON：Set up skin color correction function
0：OFF 1：ON

RNFROFF：Color Mute for the area of skin color correction
0：OFF 1：ON (the area of Cb/Cr becomes 128LSB(8bit range))

LIM_FR： Set up color saturation coverage for skin color correction
000：Non ～ 111：maximum

GAIN_FR：Set up the gain for skin color correction
000：Non ～ 111：maximum

WIN_FR：Set up the phase area for skin color correction
0：45° （±22.5°） ～ 1：90° （±45°）
Note: The center axis of skin color correction is I axis.
It corrects the area of ±22.5° or ±45° for I axis as a center color phase.

PH_FR：Set up the center axis for skin color correction
100：related red ～ 000：center (I axis) ～ 011：related green
Note: 2.8° step

TINT[7:0]：adjust color phase
1111_1111：-44.8° ～ 1000_0000：-0.35° ～ 0000_0000：±0° ～ 0111_1111：＋44.45°
+ Side: Blue color shift to side Green
- Side: Blue color shift to side Red

6.18. Sub Address 0x6A to 0x6F (Mute level)

Set the Video output at MUTE mode.
Regarding MUTE function (ON/OFF), Refer to sub address 0x00 of segment 0x01.

Sub	D7	D6	D5	D4	D3	D2	D1	D0
0x6A	Reserved	Reserved	Reserved	Reserved	**MUTE_Y[3:0]**			
INIT: 0x00	Fix to 0	Fix to 0	Fix to 0	Fix to 0	YMUTE Y level 0000: 0LSB to 1111: 255LSB (17LSB step)			
0x6B	Reserved	Reserved	Reserved	Reserved	**MUTE_CB[3:0]**			
INIT: 0x00	Fix to 0	Fix to 0	Fix to 0	Fix to 0	CMUTE Cb level 1000: -128LSB to 1111: -1LSB 0000: ±0LSB to 0111: +127LSB			
0x6C	Reserved	Reserved	Reserved	Reserved	**MUTE_CR[3:0]**			
INIT: 0x00	Fix to 0	Fix to 0	Fix to 0	Fix to 0	CMUTE Cr level 1000: -128LSB to 1111: -1LSB 0000: ±0LSB to 0111: +127LSB			
0x6D	Reserved	Reserved	Reserved	Reserved	**BBACK_R[3:0]**			
INIT: 0x00	Fix to 0	Fix to 0	Fix to 0	Fix to 0	Blue Back R level 0000: 0LSB to 1111: 255LSB (17LSB step)			
0x6E	Reserved	Reserved	Reserved	Reserved	Reserved			
INIT: 0x00	Fix to 0	Fix to 0	Fix to 0	Fix to 0	Blue Back G level 0000: 0LSB to 1111: 255LSB (17LSB step)			
0x6F	Reserved	Reserved	Reserved	Reserved	**BBACK_B[3:0]**			
INIT: 0x0C	Fix to 0	Fix to 0	Fix to 0	Fix to 0	Blue Back B level 0000: 0LSB to 1100: 204LSB to 1111: 255LSB (17LSB step)			

MUTE_Y[3:0]： Set up Y level at YMUTE
0000：0LSB ～ 1111：255LSB （17LSB step）

MUTE_CB[3:0]：Set up Cb level at CMUTE
1000：-128LSB ～ 1111：-1LSB、0000：0LSB ～ 0111：127LSB （127/7LSB step）

MUTE_CR[3:0]：Set up Cr level at CMUTE
1000：-128LSB ～ 1111：-1LSB、0000：0LSB ～ 0111：127LSB （127/7LSB step）

BBACK_R[3:0]：Set up R level at Blue back mode
0000：0LSB ～ 1111：255LSB （17LSB step）

BBACK_G[3:0]：Set up G level at Blue back mode
0000：0LSB ～ 1111：255LSB （17LSB step）

BBACK_B[3:0]：Set up B level at Blue back mode
0000：0LSB ～ 1100：204LSB ～ 1111：255LSB （17LSB step）

6.19. Sub Address 0x70 to 0x75 (RGB contrast/brightness)

Sub	D7	D6	D5	D4	D3	D2	D1	D0
0x70	**PICT_RCONT[7:0]**							
INIT: 0x80	Picture contrast (Red) 0000_0000 : x0 to 1000_0000 : x1 to 1111_1111 : x1.992							
0x71	**PICT_GCONT[7:0]**							
INIT: 0x80	Picture contrast (Green) 0000_0000 : x0 to 1000_0000 : x1 to 1111_1111 : x1.992							
0x72	**PICT_BCONT[7:0]**							
INIT: 0x80	Picture contrast (Blue) 0000_0000 : x0 to 1000_0000 : x1 to 1111_1111 : x1.992							
0x73	**PICT_ CONTON**	**PICT_ CONT_SAME**	**PICT_RBRT[5:0]**					
	Picture contrast	Picture contrast setting mode	Picture brightness (Red)					
INIT: 0x00	0: OFF 1: ON	0: Each Signal 1: RGB same setting	10_0000:-32LSB to 00_0000:±0LSB to 01_1111:+31LSB					
0x74	**PICT_ BRTON**	**PICT_ BRT_SAME**	**PICT_GBRT[5:0]**					
	Picture brightness	Picture brightness setting mode	Picture brightness (Green)					
INIT: 0x00	0: OFF 1: ON	0: Each Signal 1: RGB same setting	10_0000:-32LSB to 00_0000:±0LSB to 01_1111:+31LSB					
0x75	Reserved	Reserved	**PICT_BBRT[5:0]**					
	Fix to 0	Fix to 0	Picture brightness (Blue)					
INIT: 0x00			10_0000:-32LSB to 00_0000:±0LSB to 01_1111:+31LSB					

Contrast / Brightness control for RGB that is out of masking area

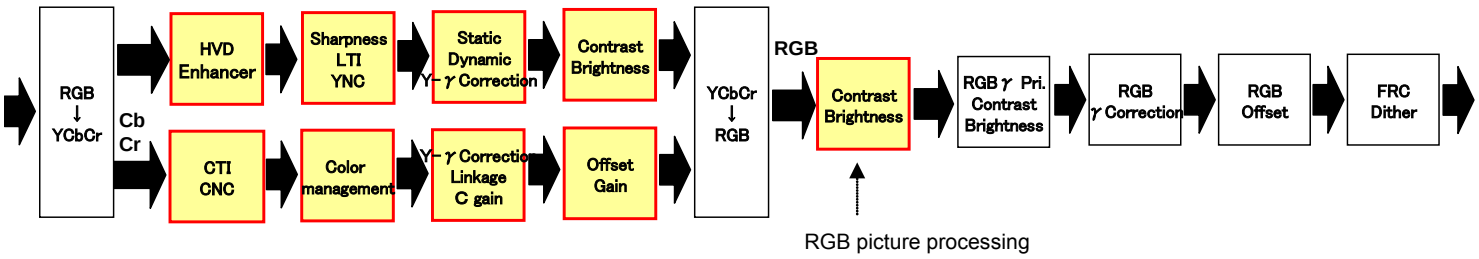
PICT_CONTON : Set up picture contrast function
0 : OFF 1 : OFF
PICT_CONT_SAME : Mode selection for picture contrast
0 : Set up RGB independently
(Each of RGB is set via **PICT_RCONT[7:0]**、**PICT_GCONT[7:0]**、**PICT_BCONT[7:0]**)
1 : Control all of RGB at the same time
(The value of **PICT_RCONT [7:0]** becomes effective with G and B.)

PICT_RCONT[7:0] : Adjust picture contrast (R signal)
PICT_GCONT[7:0] : Adjust picture contrast (G signal)
PICT_BCONT[7:0] : Adjust picture contrast (B signal)
0000_0000 : x0 ～ 1000_0000 : x1 ～ 1111_1111 : x1.992

PICT_BRTON：Set up picture brightness function
0：OFF 1：OFF
PICT_BRT_SAME：Mode selection for picture brightness
0：Set up RGB independently
(Each of RGB is set via **PICT_RBRT[7:0]**、**PICT_GBRT[7:0]**、**PICT_BBRT[7:0]**)
1：Control all of RGB at the same time
(The value of PICT **PICT_RBRT [7:0]** becomes effective with G and B.)

PICT_RBRT[5:0]：Adjust picture brightness (R signal)
PICT_GBRT[5:0]：Adjust picture brightness (G signal)
PICT_BBRT[5:0]：Adjust picture brightness (B signal)
10_0000：-32LSB ～ 00_0000：±0LSB ～ 01_1111：+31LSB

(Note) Regarding the partition arrangement of RGB picture processing, refer to as shown below.



6.20. Sub Address 0x76 to 0x7F (RGB contrast/brightness, FRC/Dither)

Sub	D7	D6	D5	D4	D3	D2	D1	D0
0x76	**RCONT[7:0]**							
	RGB contrast (Red) before RGB gamma correction							
INIT: 0X80	0000_0000 : x0 to 1000_0000 : x1 to 1111_1111 : x1.992							
0x77	**GCONT[7:0]**							
	RGB contrast (Green) before RGB gamma correction							
INIT: 0X80	0000_0000 : x0 to 1000_0000 : x1 to 1111_1111 : x1.992							
0x78	**BCONT[7:0]**							
	RGB contrast (Blue) before RGB gamma correction							
INIT: 0X80	0000_0000 : x0 to 1000_0000 : x1 to 1111_1111 : x1.992							
0x79	**CONTON**	**CONT_SAME**	**RBRT[5:0]**					
	Contrast before RGB gamma	Contrast before RGB gamma Setting mode	RGB brightness (Red) before RGB gamma correction					
INIT: 0X00	0: OFF 1: ON	0: Each Signal 1: RGB same setting	10_0000: -32LSB to 00_0000: ±0LSB to 01_1111: +31LSB					
0x7A	**BRTON**	**BRT_ RGBSAME**	**GBRT[5:0]**					
	Brightness before RGB gamma	Brightness before RGB gamma Setting mode	RGB brightness (Green) before RGB gamma correction					
INIT: 0X00	0: OFF 1: ON	0: Each Signal 1: RGB same setting	10_0000: -32LSB to 00_0000: ±0LSB to 01_1111: +31LSB					
0x7B	**DITHERON**	**N_HALF**	**BBRT[5:0]**					
	Dither process		RGB brightness (Blue) before RGB gamma correction					
INIT: 0X00	0: OFF 1: ON	0: 3bit 1: 2bit	10_0000: -32LSB to 00_0000: ±0LSB to 01_1111: +31LSB					
0x7C	**OFSTON**	**OFST_ RGBSAME**	**ROFST[5:0]**					
	RGB brightness after RGB gamma	RGB brightness after RGB gamma Setting mode	RGB brightness (Red) after RGB gamma correction					
INIT: 0X00	0: OFF 1: ON	0: Each Signal 1: RGB same setting	10_0000: -32LSB to 00_0000: ±0LSB to 01_1111: +31LSB					
0x7D	**FRCON**	**HALF_FRC**	**GOFST[5:0]**					
	FRC	FRC Frame process	RGB brightness (Green) after RGB gamma correction					
INIT: 0X00	0: OFF 1: ON	0: 4 Frame 1: 2 Frame	10_0000: -32LSB to 00_0000: ±0LSB to 01_1111: +31LSB					
0x7E	**FRC_PCON[1:0]**		**BOFST[5:0]**					
	FRC Line process		RGB brightness (Blue) after RGB gamma correction					
INIT: 0X00	00:Line process ON 01:Line process OFF 10:Line process (1/2 rate) 11:Line process (1/4 rate)		10_0000: -32LSB to 00_0000: ±0LSB to 01_1111: +31LSB					
0x7F	**FDOUTON**	**FDOTIME**			**FDINON**	**FDITIM**		
	Fade Out				Fade IN			
INIT: 0X00	0: OFF 1: ON	000: (8V) to 111: (64V)			0: OFF 1: ON	000: (8V) to 111: (64V)		

< Contrast / Brightness control for all of picture area (include masked area) >

＜RGB Contrast adjust before stage of γ correction＞
CONTON：Set up RGB Contrast adjustment function
0：OFF 1：OFF
CONT_SAME：Mode selection for RGB Contrast
0：Set up RGB independently (**RCONT[7:0], GCONT[7:0], BCONT[7:0]**)
1：Control all of RGB at the same time
(The value of **RCONT [7:0]** becomes effective with G and B.)

RCONT[7:0]：Contrast adjust for R signal
GCONT[7:0]：Contrast adjust for G signal
BCONT[7:0]：Contrast adjust for B signal
0000_0000：x0 ～ 1000_0000：x1 ～ 1111_1111：x1.992

＜RGB Brightness adjust before stage of γ correction＞
BRTON：Set up RGB Brightness adjustment function
0：OFF 1：OFF

BRT_RGBSAME：Mode selection for RGB Brightness
0：Set up RGB independently (**RBRT[5:0], GBRT[5:0], BBRT[5:0]**)
1：Control all of RGB at the same time
(The value of **RBRT [5:0]** becomes effective with G and B.)

RBRT[5:0]：Brightness adjust for R signal
GBRT[5:0]：Brightness adjust for G signal
BBRT[5:0]：Brightness adjust for B signal
10_0000：-32LSB ～ 00_0000：±0LSB ～ 01_1111：+31LSB

＜RGB Offset adjust after stage of γ correction＞
OFSTON：Set up Offset control
0：OFF 1：OFF

OFST_RGBSAME：Mode selection for RGB Offset
0：Set up RGB independently (**ROFST [5:0]、GOFST [5:0]、BOFST [5:0]**)
1：Control all of RGB at the same time
(The value of **ROFST [5:0]** becomes effective with G and B.)

ROFST [5:0]：Offset adjust for R signal
GOFST [5:0]：Offset adjust for G signal
BOFST [5:0]：Offset adjust for B signal
10_0000：-32LSB ～ 00_0000：±0LSB ～ 01_1111：+31LSB

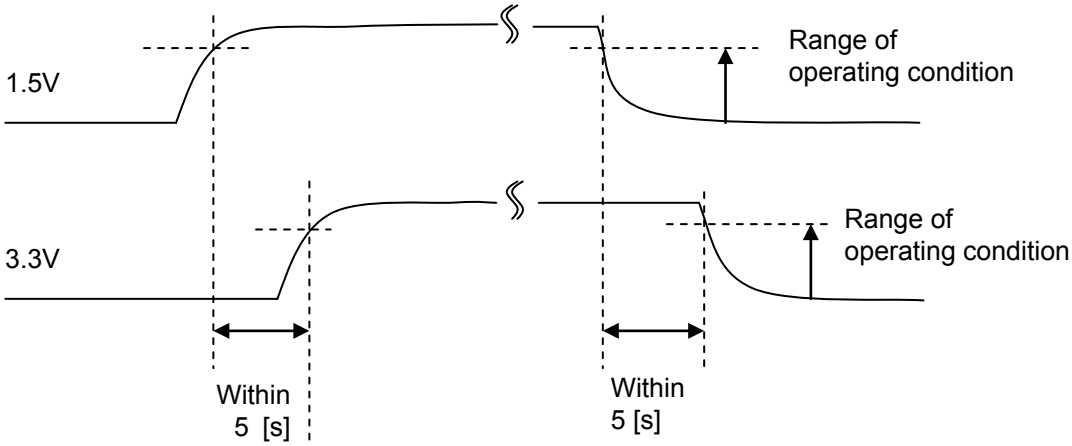
＜Dither (adding LSB) process＞
DITHERON：Set up ON/OFF of Dither process
0：OFF 1：ON
N_HALF：Set up the bit range for Dither process (10bit processing)
0：3bit (0～7LSB) 1：2bit (0～3LSB)

＜FRC process＞
FRCON：Set up FRC ON/OFF
0：OFF 1：ON
HALF_FRC：Mode selection for FRC
0：4 frame 1：2 frame

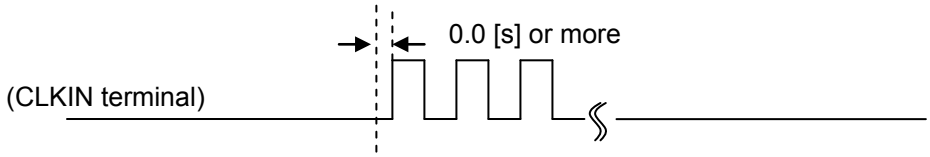
7. Control condition for Power ON and OFF sequence

This section is critical to the reliability assurance of the IC.
Read it carefully before setting power-on/off control, reset control and I^2C-BUS control timing settings.

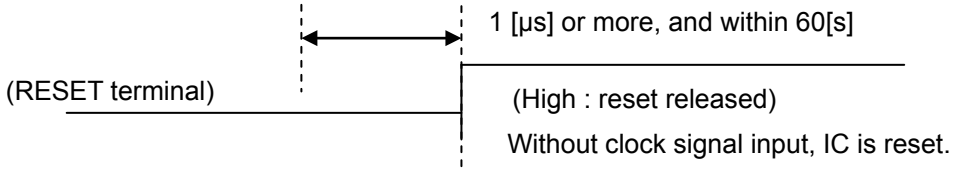
(1) Power ON/OFF
Supply voltage are 1.5V and 3.3V.
The order of power-on and power-off of 2-system VDD is good with random order.
However, please complete power-on and power-off of 2-system VDD within 5 seconds.



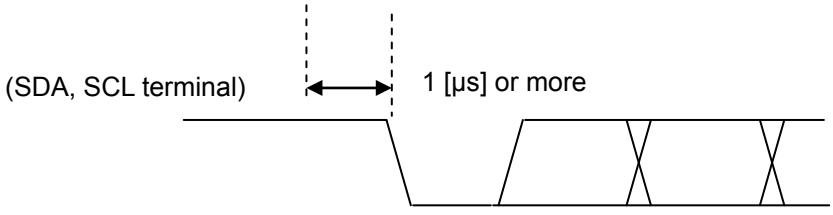
(2) Clock input
Clock signal is inputted after operating condition for 3.3V supply voltage.



(3) Reset
Keep the RESET state at least 1µs after all 2 system power have reached operating condition power voltage.
The maximum period for retaining the RESET state is 60 seconds.



(4) I^2C-BUS Control start
Start the I^2C-BUS control 1µs or more, after inputting clock and releasing the RESET.



8. Revision History

Date	Revision	Contents
2016/05/13	1.0	First edition for application note of summary version
2016/08/02	2.0	2nd edition

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