

## TB6560AFTG

### Usage considerations

#### **Summary**

The TB6560AFTG drives a two-phase bipolar stepping motor. It drives at a constant current by PWM control. The TB6560AFTG can be used in applications that require 2-phase, 1-2-phase, 2W1-2-phase and 4W1-2-phase excitation modes. It is capable of forward and reverse driving of a two-phase bipolar stepping motor using only a clock signal.

**Contents**

Summary .....	1
1. Power supply voltage .....	3
2. Output Current.....	4
3. Output ON-Resistance .....	4
4. Output Residual Voltage.....	4
5. Power Dissipation.....	5
6. Application Circuit Example .....	6
7. Excitation Mode Setting .....	9
Notes on Contents.....	13
IC Usage Considerations.....	13
Notes on handling of ICs .....	13
Points to remember on handling of ICs.....	14
RESTRICTIONS ON PRODUCT USE.....	15

## 1. Power supply voltage

### (1) Operating Range of Power Supply Voltage

Characteristic	Symbol	Operating Voltage Range	Absolute Maximum Ratings	Unit
Control power supply voltage	V <sub>DD</sub>	4.5 to 5.5	6	V
Motor power supply voltage	V <sub>MA</sub> , V <sub>MB</sub>	4.5 to 34	40	V

The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.

If a voltage outside the operating range as follows;  $4.5 \leq V_{DD} \leq 5.5$ ,  $4.5 \leq V_{MA/B} \leq 34$ ,  $V_{DD} \leq V_{MA/B}$  is applied, the IC may not operate properly or the IC and peripheral parts may be permanently damaged. Ensure that the voltage range does not exceed the upper and lower limits of the specified range.

### (2) Power-on Sequence with Control Input Signals

Turn on V<sub>DD</sub>. Then, when the V<sub>DD</sub> voltage has stabilized, turn on V<sub>MA/B</sub>.

Hold the control input pins Low while turning on V<sub>DD</sub> and V<sub>MA/B</sub>.

(All the control input pins are internally pulled down.)

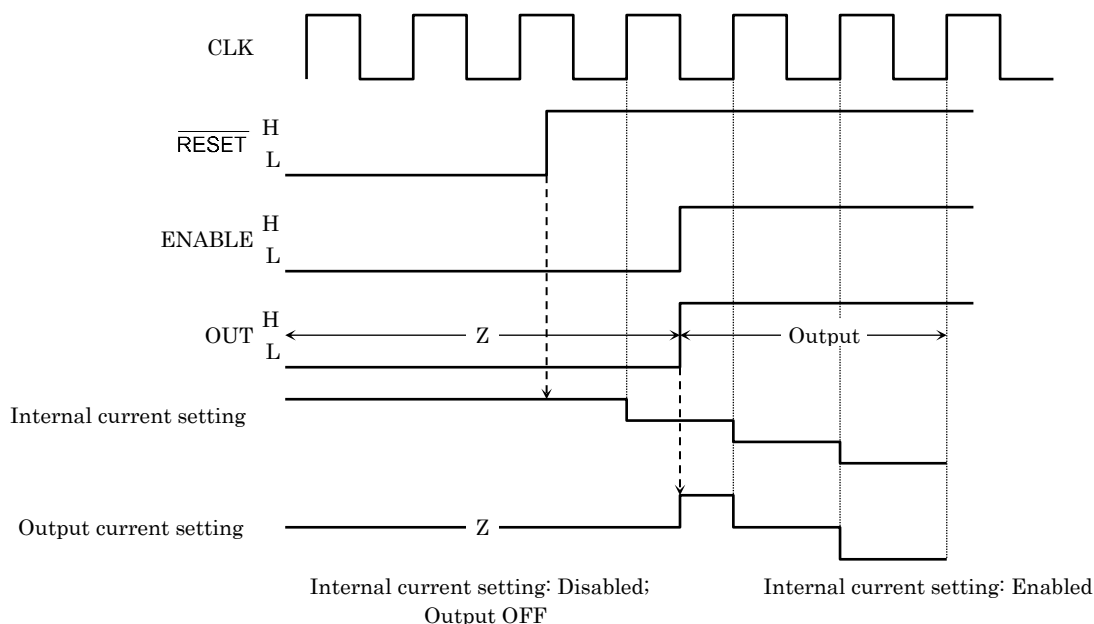
After V<sub>DD</sub> and V<sub>MA/B</sub> completely stabilizes at the rated voltages, the  $\overline{\text{RESET}}$  and ENABLE pins can be set High. If this sequence is not properly followed, the IC may not operate correctly, or the IC and the peripheral parts may be damaged.

When  $\overline{\text{RESET}}$  is released High, the CLK signal is applied and excitation is started. Only after ENABLE is also set High, outputs are enabled. When only  $\overline{\text{RESET}}$  is set High, outputs are disabled and only the internal counter advances. Likewise, when only ENABLE is set High, the excitation will not be performed even if the CLK signal is applied and the outputs will remain in the initial state.

An example of a control input sequence is shown below.

A power-off sequence should be the reverse of this sequence.

Recommended Control Input Sequence is indicated below.



## 2. Output Current

The absolute maximum rating is 2.5 A per phase, and the upper limit of operating current is 1.5 A per phase. The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.

The average permissible current is restricted by total power dissipation. Please use the IC within the range of the power dissipation.

## 3. Output ON-Resistance

Output ON-resistances for H-bridge: 0.7  $\Omega$  typical (upper and lower sum) and 1.0  $\Omega$  maximum (upper and lower sum) with a test condition of the  $I_{out} = 1.5$  A

## 4. Output Residual Voltage

The residual voltages of the MO and Protect output pins are up to 0.5 V each where  $I_o = 1$  mA.

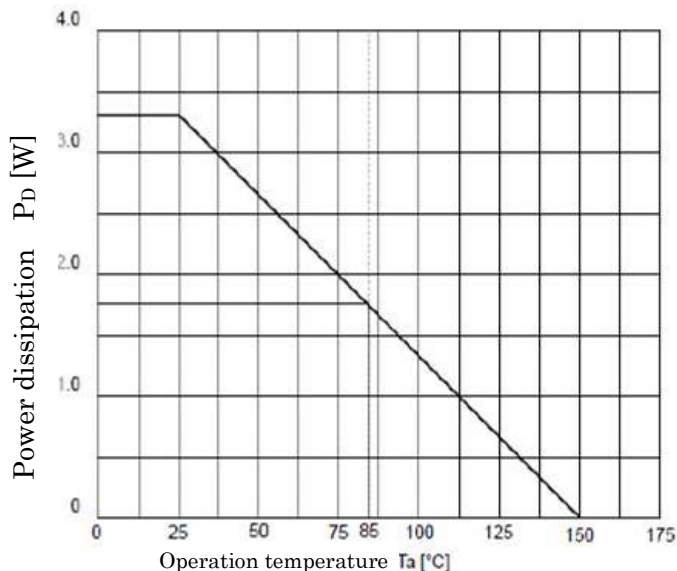
## 5. Power Dissipation

$P_D$ - $T_a$  curve of the TB6560AFTG in each mounted condition are shown below.

The operation temperature of the TB6560AFTG is up to 85°C.

When QFN48-P-0707-0.5 glass epoxy exclusive 2 layers board is mounted

(Number of layers: 2 layers, Cu thickness: 55  $\mu$ m, Board size: 85 mm  $\times$  85 mm  $\times$  1.6 mm,  $\theta_{j-a}$ : 38°C/W(typ.))



Power consumption in each excitation mode is calculated at a rough estimate as follows:

- 2-phase excitation

$$P = V_{DD} \times I_{DD} + (R_{on}(U + L) \times I_o \times I_o) \times 2$$

- 1-2 phase excitation

$$P = V_{DD} \times I_{DD} + \{(R_{on}(U + L) \times I_o \times 100\% \times I_o \times 100\% \times (2/8)) + (R_{on}(U + L) \times I_o \times 71\% \times I_o \times 71\% \times (4/8)) + (R_{on}(U + L) \times I_o \times 0\% \times I_o \times 0\% \times (2/8))\} \times 2$$

- 2W1-2 phase excitation

$$P = V_{DD} \times I_{DD} + \{(R_{on}(U + L) \times I_o \times 100\% \times I_o \times 100\% \times (2/32)) + (R_{on}(U + L) \times I_o \times 98\% \times I_o \times 98\% \times (4/32)) + (R_{on}(U + L) \times I_o \times 92\% \times I_o \times 92\% \times (4/32)) + (R_{on}(U + L) \times I_o \times 83\% \times I_o \times 83\% \times (4/32)) + (R_{on}(U + L) \times I_o \times 71\% \times I_o \times 71\% \times (4/32)) + (R_{on}(U + L) \times I_o \times 56\% \times I_o \times 56\% \times (4/32)) + (R_{on}(U + L) \times I_o \times 38\% \times I_o \times 38\% \times (4/32)) + (R_{on}(U + L) \times I_o \times 20\% \times I_o \times 20\% \times (4/32)) + (R_{on}(U + L) \times I_o \times 0\% \times I_o \times 0\% \times (2/32))\} \times 2$$

- 4W1-2 phase excitation

$$P = V_{DD} \times I_{DD} + \{(R_{on}(U + L) \times I_o \times 100\% \times I_o \times 100\% \times (2/64)) + (R_{on}(U + L) \times I_o \times 98\% \times I_o \times 98\% \times (4/64)) + (R_{on}(U + L) \times I_o \times 96\% \times I_o \times 96\% \times (4/64)) + (R_{on}(U + L) \times I_o \times 92\% \times I_o \times 92\% \times (4/64)) + (R_{on}(U + L) \times I_o \times 88\% \times I_o \times 88\% \times (4/64)) + (R_{on}(U + L) \times I_o \times 83\% \times I_o \times 83\% \times (4/64)) + (R_{on}(U + L) \times I_o \times 77\% \times I_o \times 77\% \times (4/64)) + (R_{on}(U + L) \times I_o \times 71\% \times I_o \times 71\% \times (4/64)) + (R_{on}(U + L) \times I_o \times 63\% \times I_o \times 63\% \times (4/64)) + (R_{on}(U + L) \times I_o \times 56\% \times I_o \times 56\% \times (4/64)) + (R_{on}(U + L) \times I_o \times 47\% \times I_o \times 47\% \times (4/64)) + (R_{on}(U + L) \times I_o \times 38\% \times I_o \times 38\% \times (4/64)) + (R_{on}(U + L) \times I_o \times 29\% \times I_o \times 29\% \times (4/64)) + (R_{on}(U + L) \times I_o \times 20\% \times I_o \times 20\% \times (4/64)) + (R_{on}(U + L) \times I_o \times 10\% \times I_o \times 10\% \times (4/64)) + (R_{on}(U + L) \times I_o \times 10\% \times I_o \times 10\% \times (2/64))\} \times 2$$

(Notes)

$V_{DD}$  = Power supply pin for control block

$I_{DD}$  = Supply current for control block

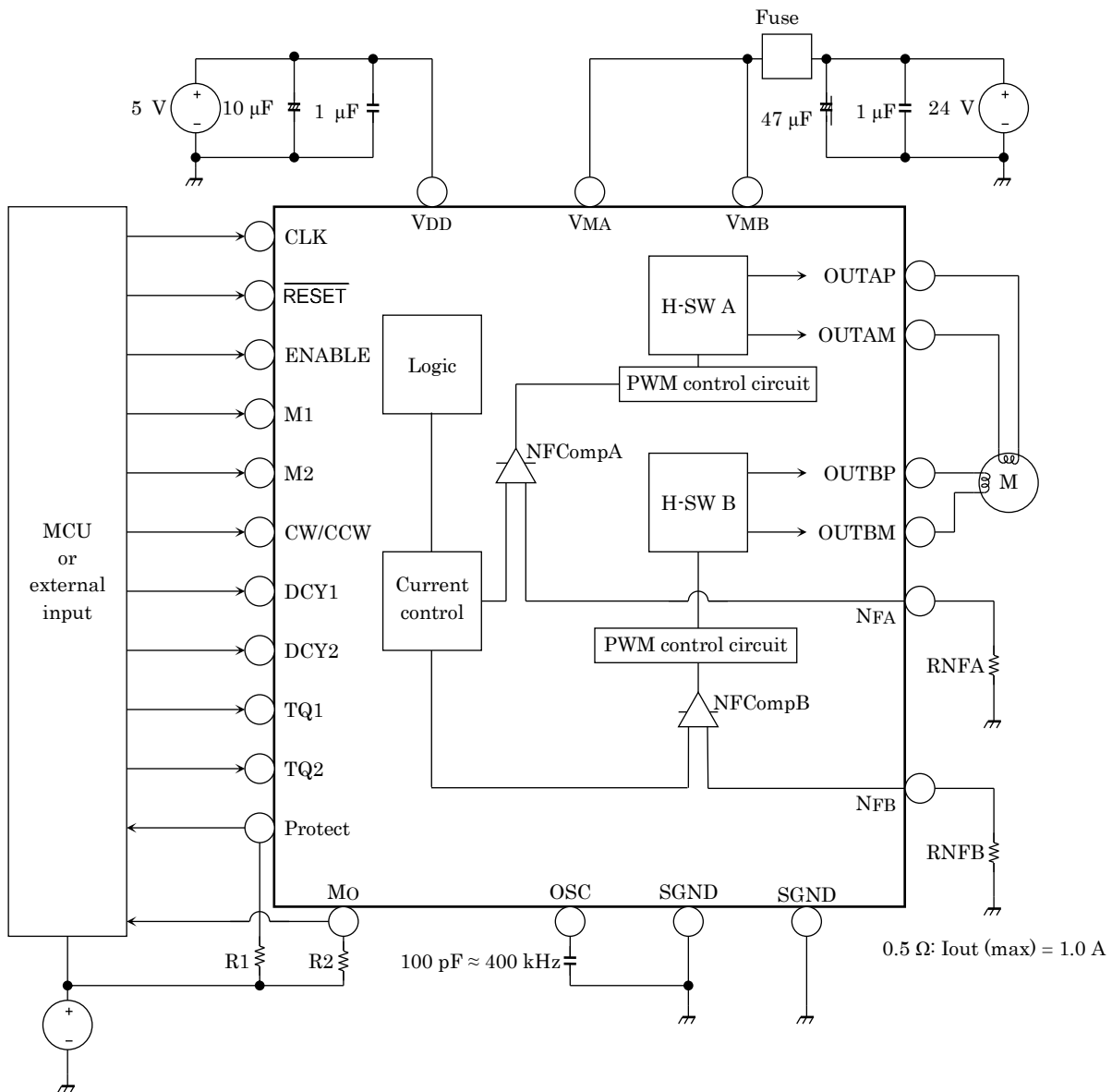
$R_{on}(U + L)$  = Output on-resistance (Upper + lower)

$I_o$  = Output current (Peak value of 100%)

Please confirm the operation in the actual operation conditions because thermal characteristics changes widely depending on the discharge characteristics of the board and the transient characteristics in the mounted state.

Heat loss can be promoted by taking the GND pattern of the print board widely. Usage of a heat sink is recommended to promote more heat loss.

**6. Application Circuit Example**



Note: Capacitors for the power supply lines should be connected as close to the IC as possible.

**Usage Considerations**

- A large current might abruptly flow through the IC in case of a short-circuit across its outputs, a short-circuit to power supply or a short-circuit to ground, leading to a damage of the IC. Also, the IC or peripheral parts may be permanently damaged or emit smoke or fire resulting in injury especially if power supply pins (VDD, VMA and VMB) or output pins (OUTAP, OUTAM, OUTBP and OUTBM) are short-circuited to adjacent or any other pins. These possibilities should be fully considered in the design of the output, VDD, VM, and ground lines.
- A fuse should be connected to the power supply line. The rated maximum current of the TB6560AFTG is 2.5 A/phase. Considering those maximum ratings, an appropriate fuse must be selected depending on operating conditions of a motor to be used. Toshiba recommends that a fast-blow fuse be used.
- The power-on sequence described on page 2 must be properly followed.  
If a voltage outside the operating range specified on page 1 ( $4.5 \leq VDD \leq 5.5$ ,  $4.5 \leq VMA/B \leq 34$ ,  $VDD \leq VMA/B$ ) is applied, the IC may not operate properly or the IC and peripheral parts may be permanently damaged. Ensure that the voltage range does not exceed the upper and lower limits of the specified range.

**(1) Capacitors for the Power Supply Lines**

Capacitors for the power supply lines between  $V_{DD}$  and GND should be connected as close to the IC as possible.

**Recommended Value**

Characteristic	Recommended Value	Remarks
$V_{DD} - GND$	10 $\mu$ F to 100 $\mu$ F	Electrolytic capacitor
	0.1 $\mu$ F to 1 $\mu$ F	Ceramic capacitor

**(2) Capacitors for  $V_M$  Terminal**

Capacitors for  $V_M$  terminal between  $V_M$  and GND should be connected as close to the IC as possible.

**Recommended Value**

Characteristic	Recommended Value	Remarks
$V_M - GND$	10 $\mu$ F to 100 $\mu$ F	Electrolytic capacitor
	0.1 $\mu$ F to 1 $\mu$ F	Ceramic capacitor

**(3) Resistances for NFA and NFB Terminals**

The resistance of NFA terminal (RNFA) and that of NFB terminal (RNFB) determine the maximum current of phase A and B.

The reference current for the constant current operation should be set by the external resistance. When voltage for NFA and NFB terminals become 0.5 V or more (in case torque is 100 %.), it stops charging and the current which is over the reference value does not flow.

$$I_{out} (A) = 0.5 V/RNF (\Omega)$$

Example: When the maximum current is 1 A, external resistance is 0.5  $\Omega$ .

**(4) Adjusting the External Capacitor Value ( $C_{OSC}$ ) and Minimum Clock Pulse Width ( $t_w$  (CLK))**

A triangular-wave is generated internally by CR oscillation. The capacitor is externally connected to the OSC pin. The recommended capacitor value is between 100 pF and 1000 pF.

Approximate equation:  $f_{osc} = 1/\{C_{OSC} \times 1.5 \times (10/C_{OSC} + 1)/66\} + 1000$  kHz

(Since this is an approximation formula, the calculation result may not be exactly equal to the actual value.)

The approximate values are shown below.

The minimum clock pulse width ( $t_w$ (CLK)) corresponds to the external capacitor ( $C_{OSC}$ ) as follows:

Capacitor	Oscillating Frequency	Minimum Clock Pulse Width $t_w$ (CLK) (Note)
1000 pF	44 kHz	90 $\mu$ s
330 pF	130 kHz	30 $\mu$ s
100 pF	400 kHz	10 $\mu$ s

Note: When the frequency of an input clock signal is high, the  $C_{OSC}$  value should be small so that the duty cycle of an input clock pulse does not become extremely high (should be around 50% or lower).

- (5) To set decay mode (current decay by DCY1 and DCY2 terminals), set the appropriate mode by monitoring the waveform of motor coil current. The appropriate mode depends on the conditions (usage motor, power supply voltage, CLK frequency, and so on).

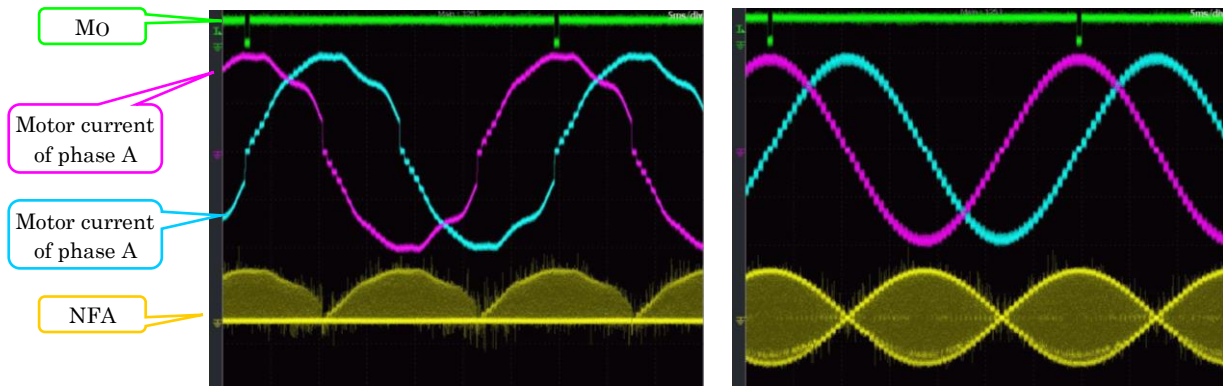
**Example: Set current decay**

**(a) Normal mode**

(First decay = 0%, DCY1 = Low, DCY2 = Low)

**(b) 50%Decay mode**

(First decay = 50%, DCY1 = Low, DCY2 = High)

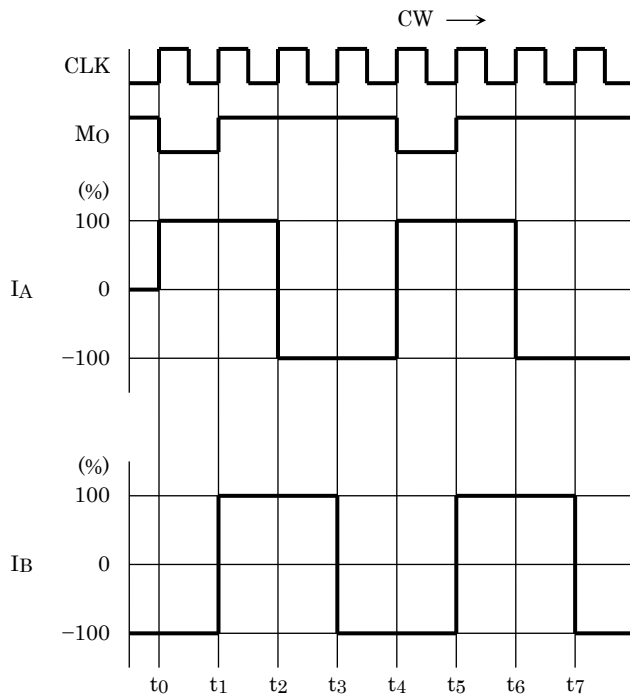




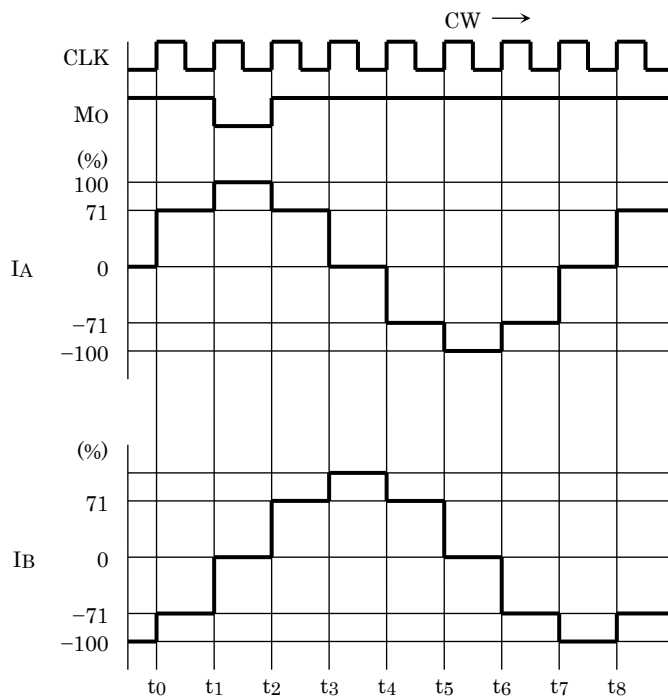
## 7. Excitation Mode Setting

The excitation mode can be selected from 2 phase, 1-2 phase, 2W1-2 phase, and 4W1-2 phase modes using the M1 and M2 inputs. It is capable of forward and reverse driving of a two-phase bipolar stepping motor with CW and CCW terminals using only a clock signal.

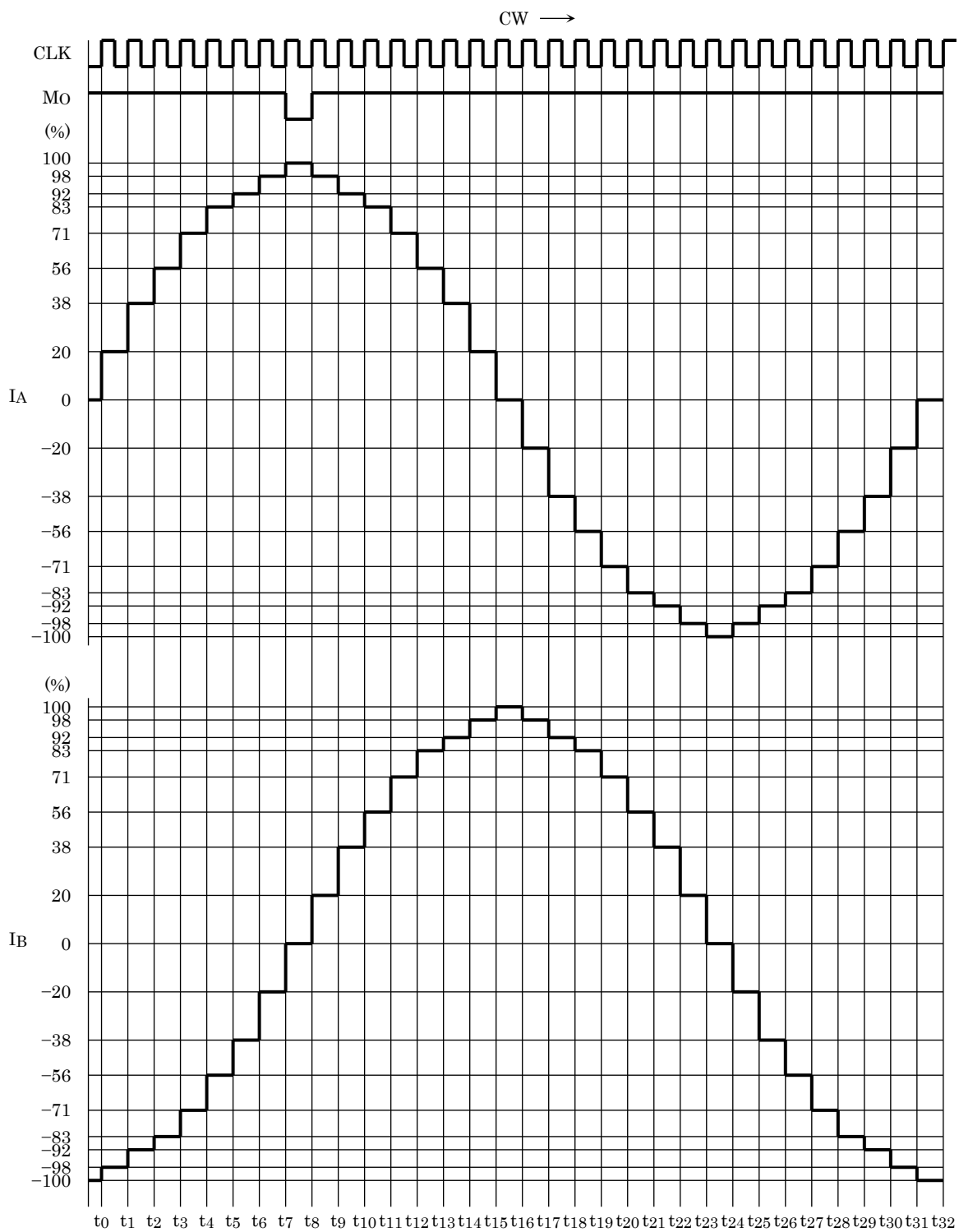
### 2-Phase Excitation (M1: L, M2: L, CW mode)



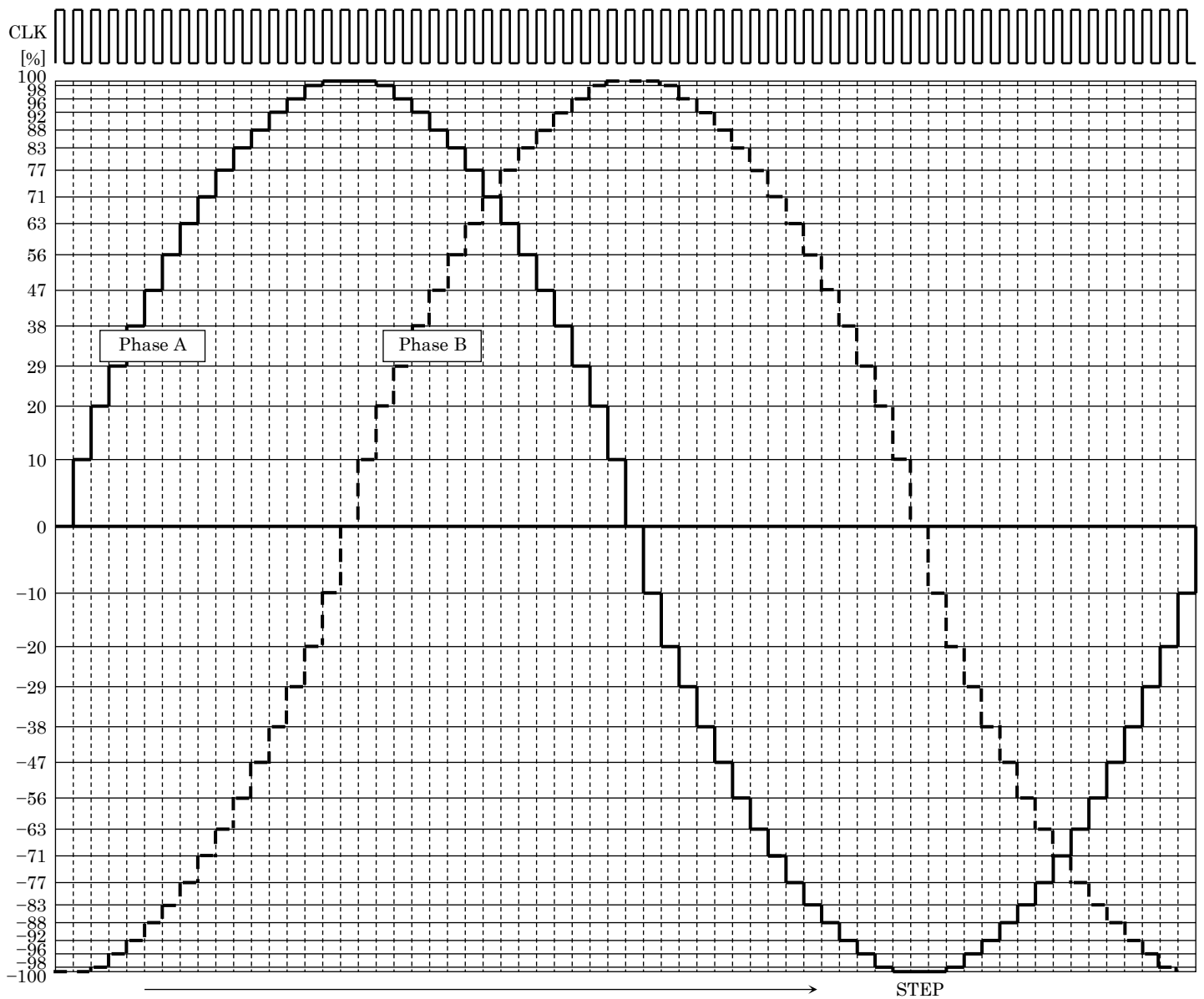
### 1-2 Phase Excitation (M1: H, M2: L, CW mode)



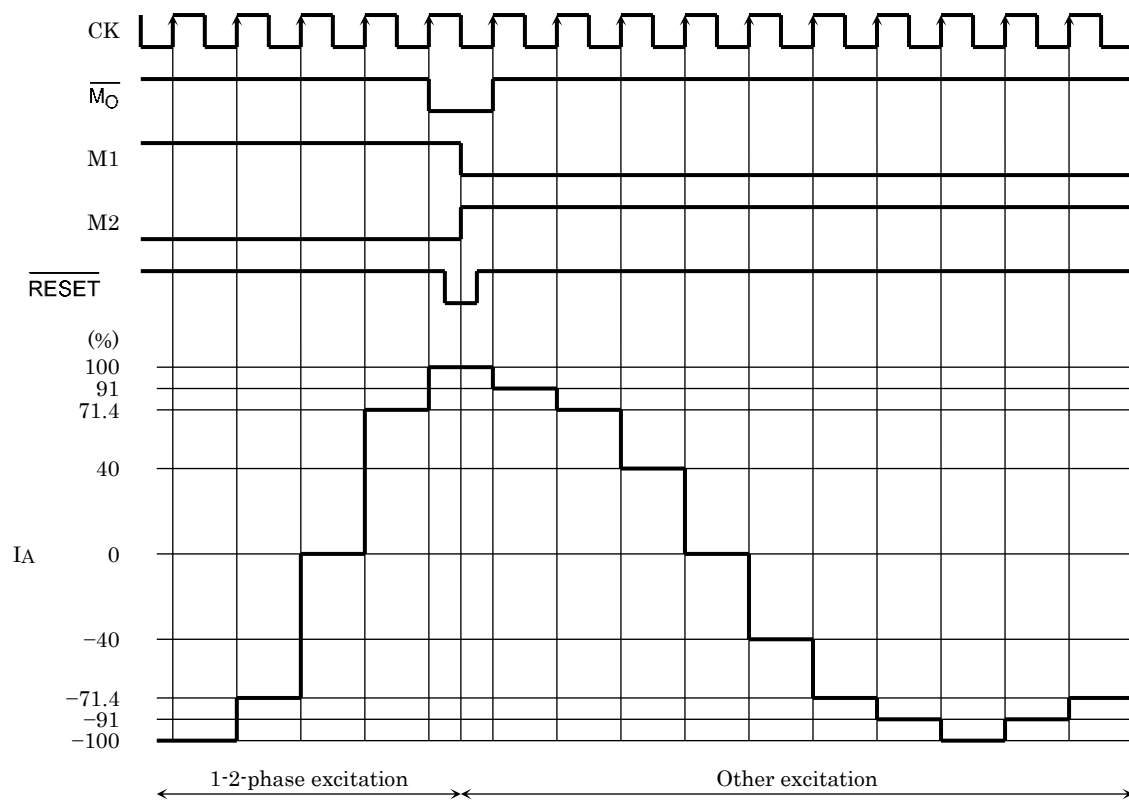
## 2W1-2 Phase Excitation (M1: H, M2: H, CW mode)



## 4W1-2 Phase Excitation (M1: L, M2: H, CW mode)



## Input Signal Example



It is recommended that the state of the M1 and M2 pins be changed after setting the  $\overline{\text{RESET}}$  signal Low during the Initial state ( $\overline{\text{M0}} = \text{Low}$ ). Even when the  $\overline{\text{M0}}$  signal is Low, changing the M1 and M2 signals without setting the  $\overline{\text{RESET}}$  signal Low may cause a discontinuity in the current waveform.

## Notes on Contents

1. Block diagram  
Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.
2. Equivalent Circuits  
The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.
3. Timing Charts  
Timing charts may be simplified for explanatory purposes.
4. Application Circuit  
The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass production design stage. Toshiba does not grant any license to any industrial property rights by providing these examples of application circuits.
5. Test Circuit  
Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

## IC Usage Considerations

### Notes on handling of ICs

- (1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings. Exceeding the rating(s) may cause device breakdown, damage or deterioration, and may result in injury by explosion or combustion.
- (2) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in the case of overcurrent and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead to smoke or ignition. To minimize the effects of the flow of a large current in the case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.
- (3) If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition. Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.
- (4) Do not insert devices in the wrong orientation or incorrectly. Make sure that the positive and negative terminals of power supplies are connected properly. Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion. In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.

**Points to remember on handling of ICs**

- (1) **Thermal Shutdown Circuit**  
Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over temperature, clear the heat generation status immediately.  
Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the thermal shutdown circuit to not operate properly or IC breakdown before operation.
- (2) **Heat Radiation Design**  
In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature ( $T_j$ ) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into consideration the effect of IC heat radiation with peripheral components.
- (3) **Back-EMF**  
When a motor rotates in the reverse direction, stops or slows down abruptly, a current flow back to the motor's power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond absolute maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.
- (4) **The IC may be permanently damaged in case of a short-circuit across its outputs, a short-circuit to power supply or a short-circuit to ground. These possibilities should be fully considered in the design of the output, VDD, VM and ground lines.**

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