TOSHIBA CMOS Integrated Circuit Silicon Monolithic

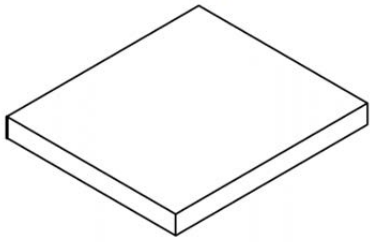
TC7738WBG

System Power IC

1. Overview

TC7738WBG is a system power IC which builds in 6 channels of a buck DC-DC convertor and 2 channels of LDO. The IC operation voltage(3.3 V or 5 V) can be changed using I^2C interface and pin settings, power supply can be provided to various systems. In addition, this product incorporates the PROTECTION-SW for the input protection.
(*Refer to as hereinafter, Channel: CH, DC-DC convertor: DC-DC)

Package



S-UFBGA45-0403-0.40-001
Weight: 10 mg (Typ.)

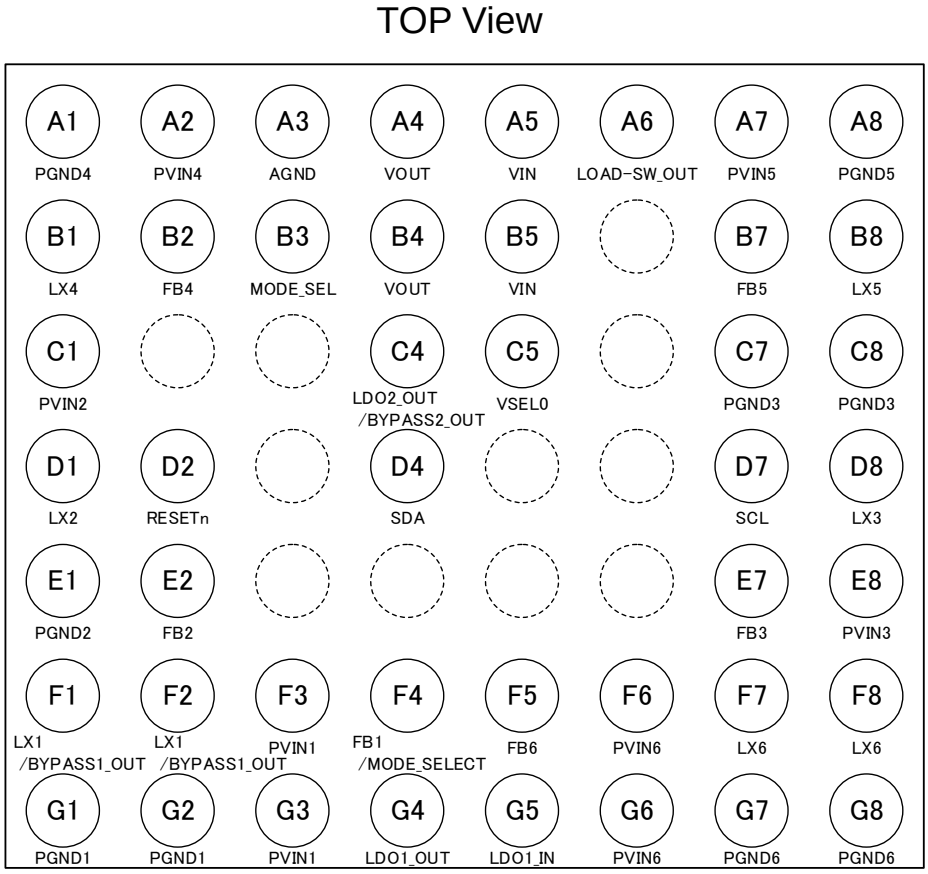
2. Application

SSD (Solid State Drive), portable devices, etc.

3. Features

- Power supply voltage (VIN):2.9 V to 5.5 V
  (PVIN1 to 6):2.9 V to 5.5 V
  (LDO1_IN): 2.9 V to 5.5 V
- IC operation condition setting when the power supply voltage is set to 3.3 V/5.0 V by MODE_SEL pin.
- 6 CH DC-DC convertor + 2 CH LDO
  - CH1: 2.325 V to 2.700 V (25 mV step), 4.0 A (MAX)
  - CH2: 1.175 V to 1.550 V / 1.025 V to 1.400 V (25 mV step), 1.0 A (MAX)
  - CH3: 1.625 V to 2.000 V (25 mV step), 2.0 A(MAX)
  - CH4: 0.825 V to 1.200 V / 1.625 V to 2.000 V (25 mV step), 1.0 A (MAX)
  - CH5: 0.825 V to 1.200 V / 0.725 V to 1.100 V (25 mV step), 1.0 A (MAX)
  - CH6: 0.825 V to 1.200 V / 0.725 V to 1.100 V (25 mV step), 3.5 A (MAX)
  - LDO1: 2.325 V to 2.700 V / 1.625 V to 2.000 V (25 mV step), 0.3 A (MAX)
  - LDO2: 3.125 V to 3.500 V (25 mV step), 0.3 A (MAX)
- Built-in BYPASS-SW: CH1, LDO2
- Built-in LOAD-SW: CH5
- Efficiency control in the case of the light load (PWM/PFM operation)
- Control by I^2C interface
- Initial values selection of DC-DC (CH1 to CH6) and LDO1 output by VSEL0 pin
- Built-in input PROTECTION-SW
- Built-in protection functions
  - Low input voltage detection circuit (UVLO)
  - Input power supply Over Voltage Protection (OVP_1)
  - Input power supply Over Current Limitation (OCL_1)
  - Input power supply Over Current Protection (OCP)
  - Output Over Voltage Protection (OVP_2)
  - Output Under Voltage Protection (UVP)
  - Output Over Current Limitation (OCL_2)
  - Thermal Shutdown protection (TSD)
- Package: S-UFBGA45-0403-0.40-001 (2.91 mm ×3.31 mm, 0.4 mm Pitch)

4. Pin Layout



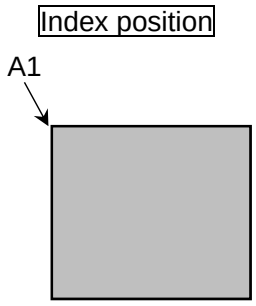


Figure 4-1 Pin Layout

5. Pin description

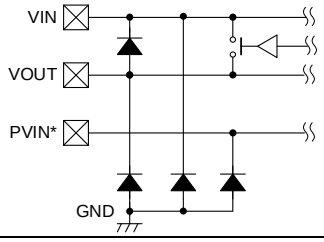
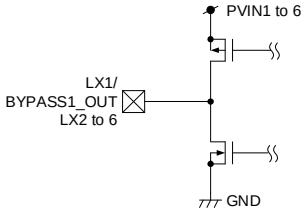
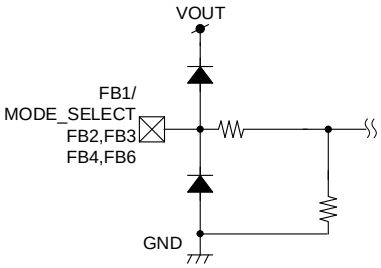
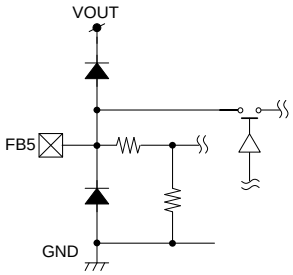
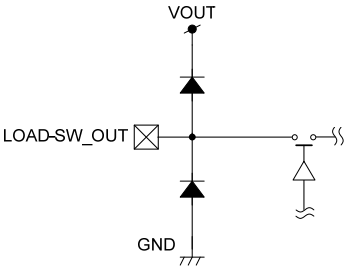
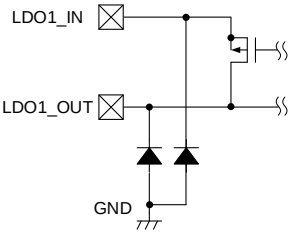
Table 5.1 Pin description

Pin number	Name	I/O	Description
A1	PGND4	—	Ground pin for CH4
A2	PVIN4	—	Power supply pin for CH4
A3	AGND	—	Ground pin for the IC
A4,B4	VOUT	O	Output pin for PROTECTION-SW circuit
A5,B5	VIN	—	Power supply pin for the IC
A6	LOAD-SW_OUT	O	Output pin for LOAD-SW
A7	PVIN5	—	Power supply pin for CH5
A8	PGND5	—	Ground pin for CH5
B1	LX4	O	Switching output pin for CH4
B2	FB4	I	Feedback pin for CH4 output voltage
B3	MODE_SEL	I	IC operation condition setting pin when the voltage to be supplied to VIN pin is 3.3 V or 5.0 V. This pin is pulled up by resistsance in the IC. In the case of 3.3 V, connect to GND. In the case of 5 V, open. The setting should not be changed during operation.
B7	FB5	I	Feedback pin for CH5 and input pin of LOAD-SW
B8	LX5	O	Switching output pin for CH5
C1	PVIN2	—	Power supply pin for CH2
C4	LDO2_OUT / BYPASS2_OUT	O	Output pin for LDO2 In the BYPASS MODE, VOUT pin voltage is output.
C5	VSEL0	I	Initial values selection pin for the voltage from CH1 to CH6 and LDO1 This pin is pulled down by resistance in the IC. This pin should be connected to GND or VOUT. The setting should not be changed during operation.
C7,C8	PGND3	—	Ground pin for CH3
D1	LX2	O	Switching output pin for CH2
D2	RESETn	O	Pin of output “L” during power-on-reset , connect to pull-up resistance
D4	SDA	I/O	Data input and output pin for I^2C
D7	SCL	I	Clock input pin for I^2C
D8	LX3	O	Switching output pin for CH3
E1	PGND2	—	Ground pin for CH2
E2	FB2	I	Feedback pin for CH2 output voltage
E7	FB3	I	Feedback pin for CH3 output voltage
E8	PVIN3	—	Power supply pin for CH3
F1,F2	LX1 / BYPASS1_OUT	O	Switching pin for CH1 In the BYPASS MODE, PVIN1 pin voltage is output.
F3,G3	PVIN1	—	Power supply pin for CH1
F4	FB1 / MODE_SELECT	I	Feedback pin for CH1, shared with the setting pin of BYPASS MODE
F5	FB6	I	Feedback pin for CH6 output voltage
F6,G6	PVIN6	—	Power supply pin for CH6
F7,F8	LX6	O	Switching output pin for CH6
G1,G2	PGND1	—	Ground pin for CH1
G4	LDO1_OUT	O	Output pin for LDO1
G5	LDO1_IN	—	Power supply pin for LDO1
G7,G8	PGND6	—	Ground pin for CH6

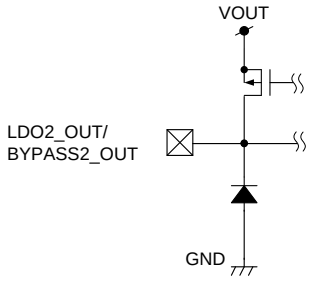
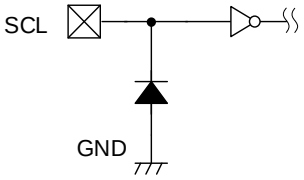
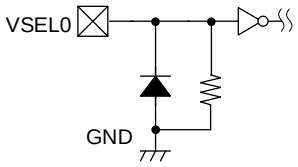
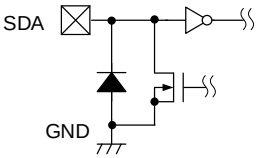
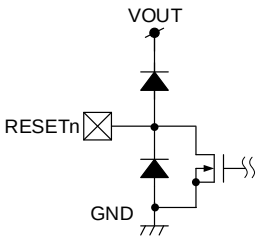
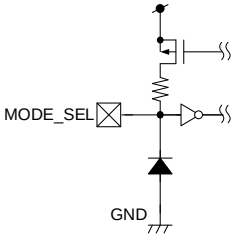
6. I/O Equivalent Pin Circuit

Table 6.1 I/O Equivalent Pin Circuit

Note: Equivalent circuit is simplified to understand.

Pin name	Equivalent circuit
VIN VOUT PVIN1 to 6 AGND PGND1 to 6	
LX1/BYPASS1_OUT LX2 to 6	
FB1/MODE_SELECT FB2 FB3 FB4 FB6	
FB5	
LOAD-SW_OUT	
LDO1_IN LDO1_OUT	

Note: Equivalent circuit is simplified to understand.

Pin name	Equivalent circuit
LDO2_OUT/ BYPASS2_OUT	
SCL	
VSEL0	
SDA	
RESETn	
MODE_SEL	

7. Block diagram

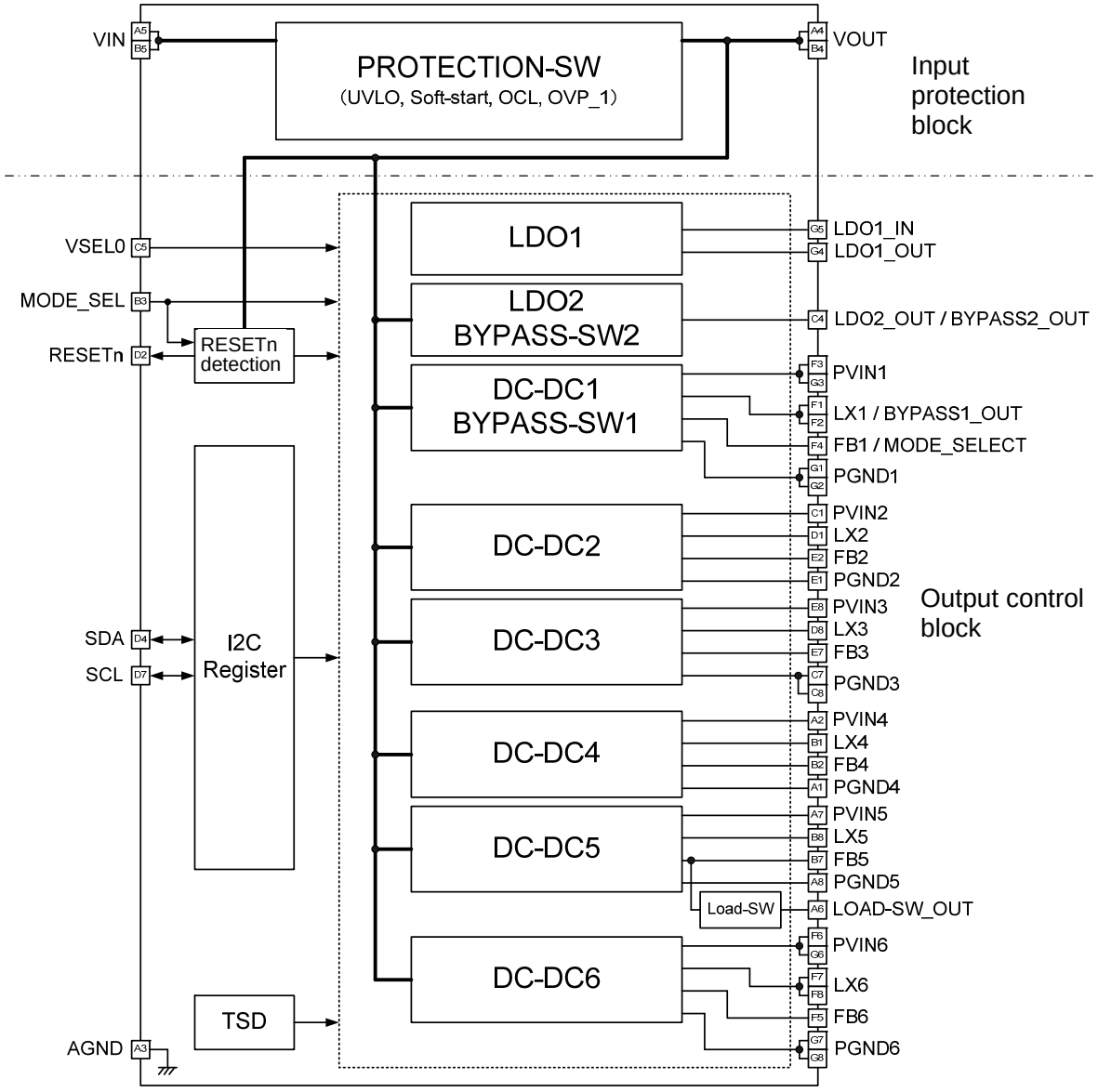


Figure 7-1 Block diagram

Note: Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

8. Functional specifications

8.1. Operation description

TC7738WBG consists with PROTECTION-SW for the input protection, 6 channels of DC-DC and 2 channels of LDO. When the voltage is applied to the VIN, PROTECTION-SW is turned on, supplied to the output control block, and each channels start to output. Since it includes I^2C interface, various settings such as output voltage can be set.

Since using MODE_SEL pin enables setting of RESETn and OVP_1 threshold voltage, both 3.3 V and 5 V system can be used. Moreover, VSEL0 pin input enables default output voltage setting of each channel.

8.2. Input protection function (PROTECTION-SW)

TC7738WBG has a built-in low ON resistance MOSFET for ON/OFF control between VIN and VOUT, and protects the IC from over voltage of input and overcurrent of output.

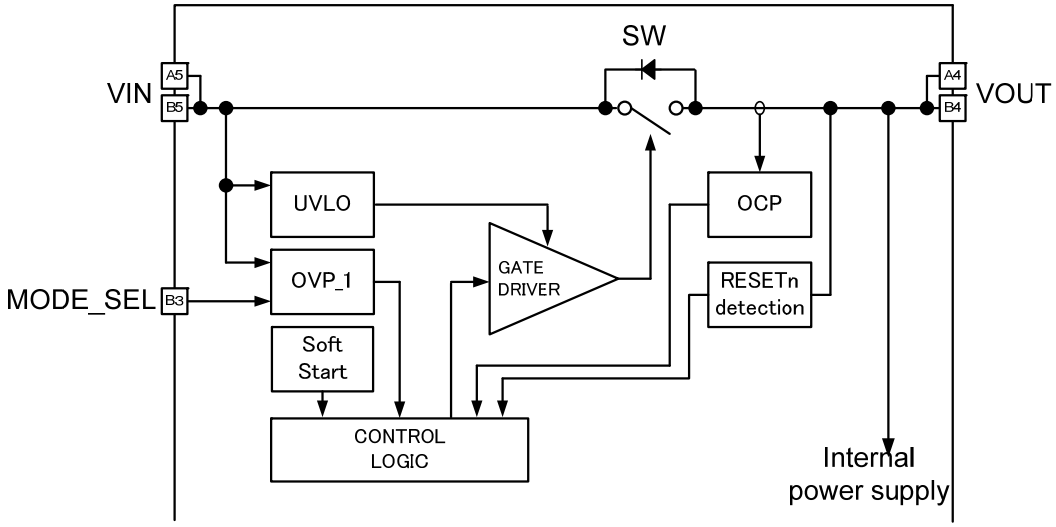


Figure 8-1 Block diagram of PROTECTION-SW

8.2.1. Low input voltage detection (UVLO)

If VIN input voltage exceeds UVLO deactive voltage, PROTECTION-SW turns on. If the voltage is lower than UVLO detection voltage, PROTECTION-SW is turned off and power supply to the internal circuit is stopped.

Table 8.1 PROTECTION-SW UVLO threshold

Deactive/Detection	Threshold
UVLO deactive (rise/fall)	1.9 V (typ.)

8.2.2. Input overvoltage protection (OVP_1)

This product incorporates an input overvoltage protection (OVP_1) circuit and the threshold is determined by MODE_SEL pin setting.
When VIN voltage exceeds OVP detection value, PROTECTION-SW is turned off. It is turned on after the voltage is returned to less than OVP deactive voltage.

Table 8.2 OVP_1 voltage

MODE_SEL	L (3.3 V mode)	Open (5.0 V mode)
OVP_1 detection (rise)	3.9 V (typ.)	5.8 V (typ.)
OVP_1 deactive (fall)	3.8 V (typ.)	5.7 V (typ.)

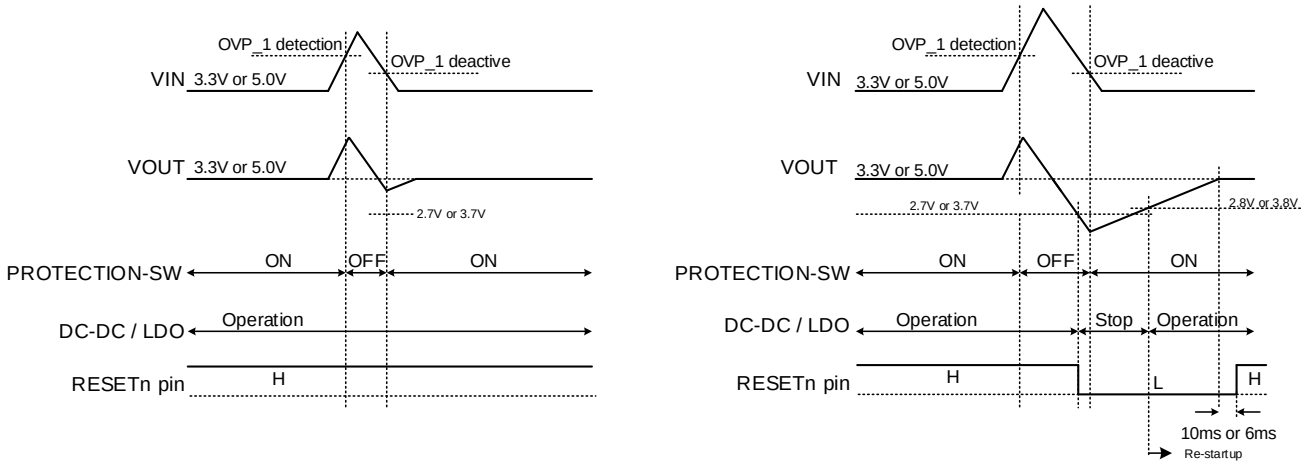
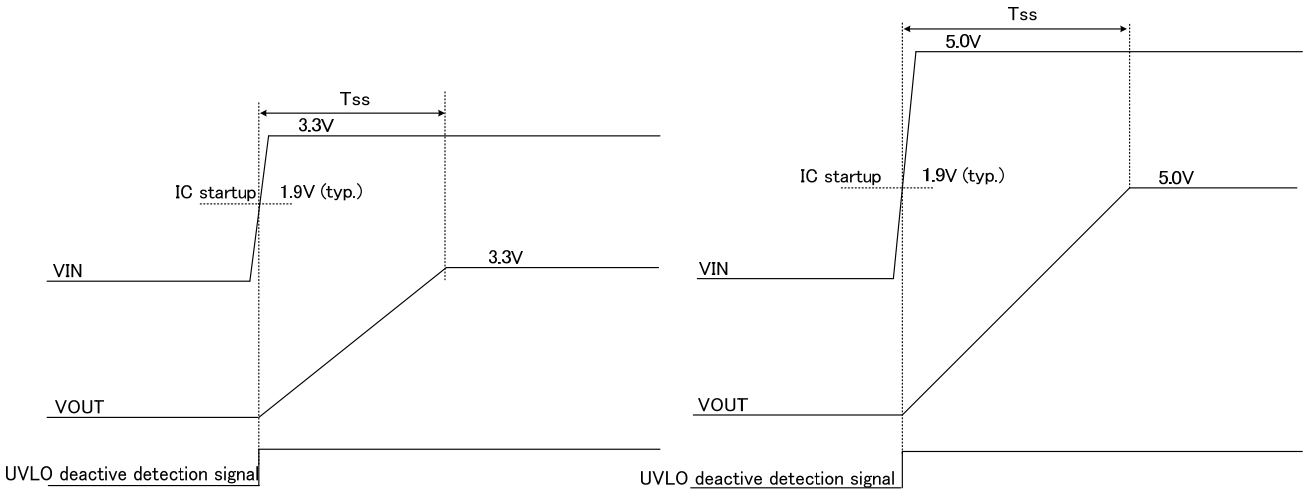


Figure 8-2 OVP_1 operation

8.2.3. Soft start function

If VIN input voltage exceeds UVLO deactive voltage, VOUT voltage rises with the soft start function.
This product incorporates 200 mA (Max) of the current limitation circuit, and VOUT rising gradient is determined by the current limited by this circuit and the charge time to the capacitor.



Note: UVLO deactive detection signal is internal signal.

Figure 8-3 Soft start

8.2.4. Current limitation function (OCL_1) / Over current protection (OCP)

If the current which flows into PROTECTION-SW reaches OCL current value, the input current is limited (min 4.5 A).

(1) Output stopped by OCP
If the input OCL state continues for 100 μs, all channels are stopped, registers are initialized, and RESETn changes from H to L.
Additionally the internal OCP counter is counted up 1. When the input OCL state is reset by channel stop, each channel restarts up according to startup sequence.

(2) Output stopped by VOUT voltage dropping
If the VOUT voltage is dropped by increasing output current, and lower than RESETn threshold voltage, all channels are stopped, registers are initialized, and RESETn changes from H to L.
The internal OCP counter is counted up 1 also in this case. The VOUT voltage is returned by channel stop, each channel restarts up according to startup sequence.

(3) Input shut down by OCP
If output stops of the above (1) and (2) are repeated and the internal OCP counter is counted up to 10, PROTECTION-SW is turned off and input is shut down.
In order to reset the input shut down and clear the OCP counter, VIN pin voltage has to be drop lower than UVLO detection voltage.

8.2.5. Thermal shut down (TSD)

In the case that IC temperature exceeds 140°C (Typ.), all channels are stopped, registers are initialized, and RESETn is changed from H to L. Then PROTECTION-SW is turned off. When the temperature of IC is returned less than 120°C (typ.), it restarts according to the startup sequence.

8.3. Output control block

When PROTECTION-SW is turned on and supplied voltage to VOUT, the output control block starts operation. It can be set by output voltage, input pin of each channel, and register setting by I^2C.

8.3.1. RESETn detection operation

RESETn pin outputs signals to be noticed the completion of TC7738WBG startup sequence to external systems.
When VOUT voltage exceeds RESETn deactive threshold, and reaches VIN voltage after power on, the startup sequence is started, and RESETn pin outputs from L to H after passing regulation delay time.
Additionally if VOUT voltage is dropping less than RESETn detection threshold at the time of power off, all channels are stopped, registers are initialized, and RESETn changes from H to L. (Refer to Figure 8−4 and Figure 8−5.)
RESETn pin is open-drain output of Nch-MOSFET. Connect pull-up resistance.

Threshold of RESETn detection is determined by MODE_SEL pin setting. (Refer to Table 8.3.)
Output delay time of RESETn pin is determined by VSEL0 pin setting. (Refer to Table 8.4.)

Table 8.3 RESETn threshold setting

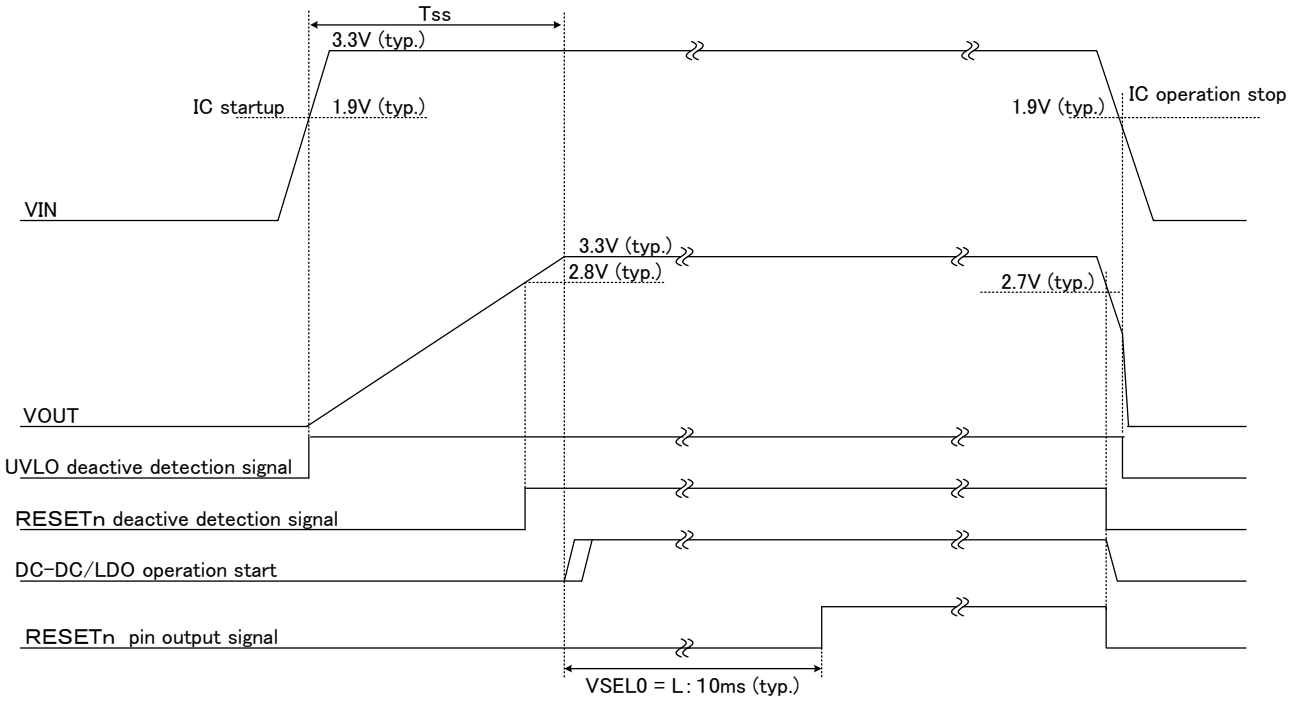
MODE_SEL	L (3.3 V mode)	Open (5.0 V mode)
RESETn deactive (rise)	2.8 V (typ.)	3.8 V (typ.)
RESETn detection (fall)	2.7 V (typ.)	3.7 V (typ.)

Table 8.4 RESETn output delay time setting

VSEL0	L	H
RESETn L -> H delay time	10 ms	6 ms

RESETn deactive/detection operation (rising/falling operation)

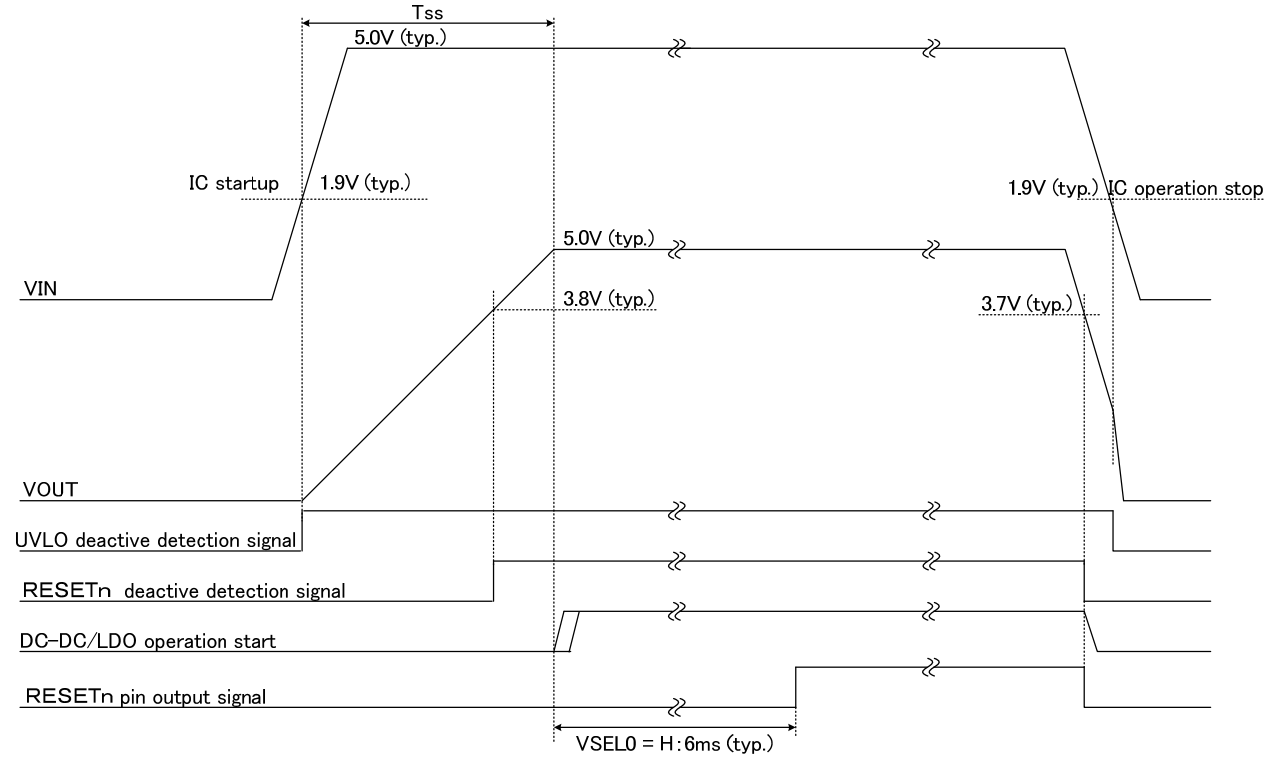
(1) VSEL0 = “L”, MODE_SEL = “L”



Note: UVLO deactive detection signal and RESETn deactive detection signal are internal signals.

Figure 8-4 RESETn deactive/detection operation (VSEL0 ="L", MODE_SEL ="L")

(2) VSEL0 = “H”, MODE_SEL = “Open”



Note: UVLO deactive detection signal and RESETn deactive detection signal are internal signals.

Figure 8-5 RESETn deactive/detection operation (VSEL0 ="H", MODE_SEL ="Open")

8.3.2. Output voltage range

The power supply of TC7738WBG consists of DC-DC1 to DC-DC6, LDO1, and LDO2. DC-DC1 and LDO2 can set BYPASS MODE. DC-DC5 incorporates LOAD-SW for extension output.

Table 8.5 Power supply configuration

CH	Output mode (Note1)	Default voltage (Note1)	Output voltage adjustment range (Note2)	Output current (MAX)	Notes
CH1	DC-DC1	2.5 V	2.325 V to 2.700 V (25 mV step)	4.0 A	—
	BYPASS MODE	—	VOUT		
CH2	DC-DC2	1.35 V	1.175 V to 1.550 V (25 mV step)	1.0 A	—
		1.2 V	1.025 V to 1.400 V (25 mV step)		
CH3	DC-DC3	1.8 V	1.625 V to 2.000 V (25 mV step)	2.0 A	—
CH4	DC-DC4	1.0 V	0.825 V to 1.200 V (25 mV step)	1.0 A	—
		1.8 V	1.625 V to 2.000 V (25 mV step)		
CH5	DC-DC5	1.0 V	0.825 V to 1.200 V (25 mV step)	1.0 A	—
		0.9 V	0.725 V to 1.100 V (25 mV step)		
CH5-SW	LOAD-SW	Applies to DC-DC5	Applies to DC-DC5	0.5 A	DC-DC5 extension output by ON/OFF in register (08h)
CH6	DC-DC6	1.0 V	0.825 V to 1.200 V (25 mV step)	3.5 A	—
		0.9 V	0.725 V to 1.100 V (25 mV step)		
LDO1	LDO1	2.5 V	2.325 V to 2.700 V (25 mV step)	0.3 A	LDO1_IN is input. Connect to VOUT.
		1.8 V	1.625 V to 2.000 V (25 mV step)		
LDO2	LDO2	3.3 V	3.125 V to 3.500 V (25 mV step)	0.3 A	—
	BYPASS MODE	—	VOUT		

Note1: For output mode and default voltage setting, refer to Table 8.6.

Note2: For output voltage setting by registers, refer to Table 8.9 to Table 8.24.

8.3.3. Default output voltage setting

Default voltage of each channel at startup can be set by VSEL0 and MODE_SEL pin input.

Table 8.6 Default output voltage

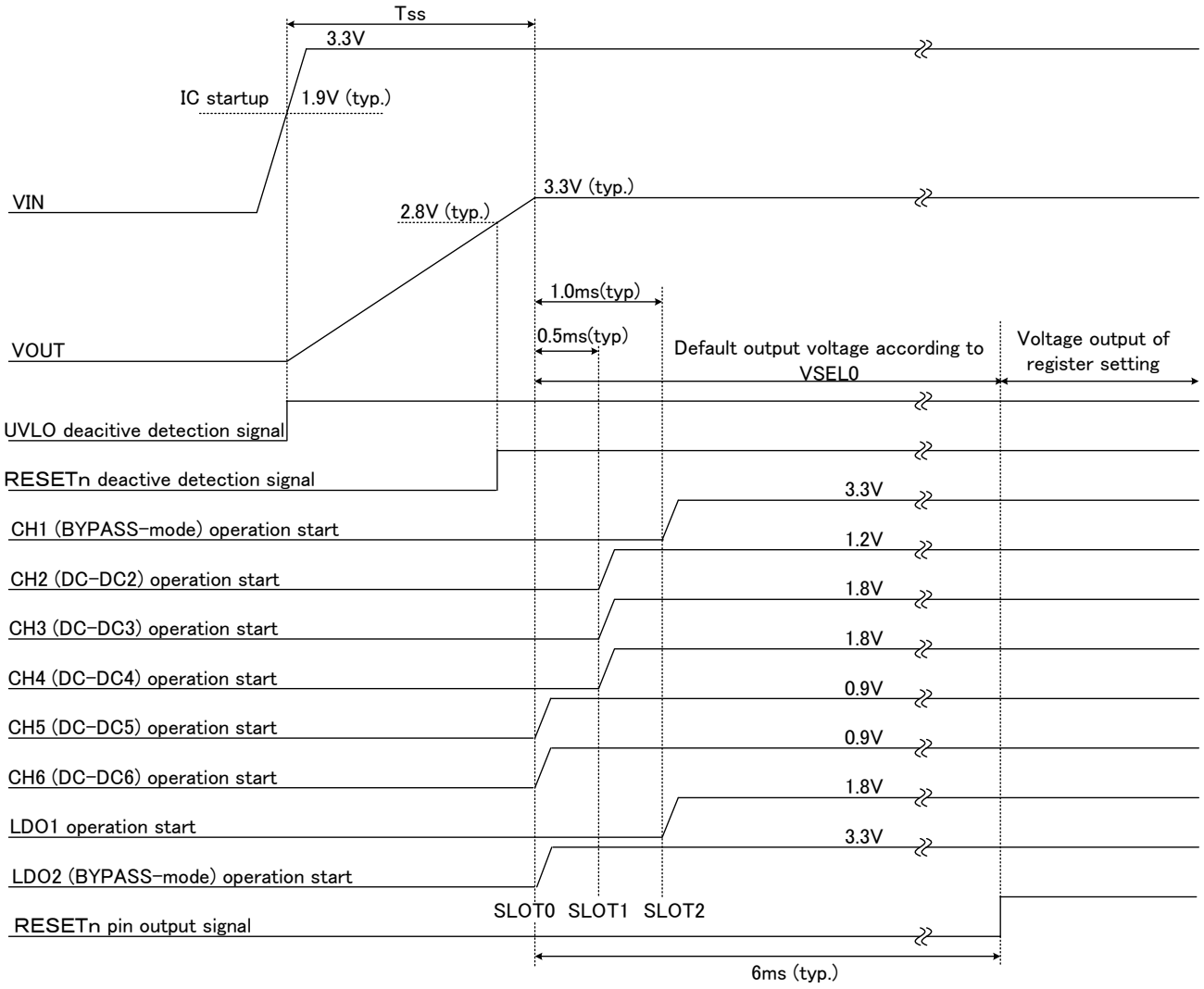
<table>
<tr><td>VSEL0
(Note1)</td><td colspan="2">L</td><td colspan="2">H</td></tr>
<tr><td>MODE_SEL
(Note1)</td><td>L
(3.3 V mode)</td><td>Open
(5.0 V mode)</td><td>L
(3.3 V mode)</td><td>Open
(5.0 V mode)</td></tr>
<tr><td rowspan="2">CH1</td><td>FB1=GND:BYPASS MODE</td><td rowspan="2">DC-DC1 = 2. 5V
(Note2)</td><td>FB1=GND:BYPASS MODE</td><td rowspan="2">DC-DC1 = 2.5 V
(Note2)</td></tr>
<tr><td>FB1=Vout1:DC-DC1 = 2.5 V</td><td>FB1=Vout1:DC-DC1 = 2.5 V</td></tr>
<tr><td>CH2</td><td colspan="2">DC-DC2= 1.35 V</td><td colspan="2">DC-DC2 = 1.2 V</td></tr>
<tr><td>CH3</td><td colspan="2">DC-DC3 = 1.8 V</td><td colspan="2">DC-DC3 = 1.8 V</td></tr>
<tr><td>CH4</td><td colspan="2">DC-DC4 = 1.0 V</td><td colspan="2">DC-DC4 = 1.8 V</td></tr>
<tr><td>CH5</td><td colspan="2">DC-DC5 = 1.0 V</td><td colspan="2">DC-DC5 = 0.9 V</td></tr>
<tr><td>CH6</td><td colspan="2">DC-DC6 = 1.0 V</td><td colspan="2">DC-DC6 = 0.9 V</td></tr>
<tr><td>LDO1</td><td colspan="2">LDO1 = 2.5 V</td><td colspan="2">LDO1 = 1.8 V</td></tr>
<tr><td>LDO2</td><td>BYPASS MODE</td><td>LDO2 = 3.3 V</td><td>BYPASS MODE</td><td>LDO2 = 3.3 V</td></tr>
</table>

Note1: VSEL0 and MODE_SEL input should not change settings during operation.
Note2: When MODE_SEL=Open, the setting should not be BYPASS MODE setting (FB1=GND).

8.3.4. Startup sequence

TC7738WBG can change the timing by writing to eFuse when the power supply of each channel turns ON. Delay time can set maximum SLT6 (3 ms (typ.)) for each channel, assuming that the SLOT time 0.5 ms (typ.) is one step.
The following shows the startup sequence of each power supply of “TC7738WBG-P00”. P00 means the setting code.

(Example) TC7738WBG-P00 setting
SLT0: CH5, CH6, LDO2
SLT1: CH2, CH3, CH4
SLT2: CH1, LDO1
VIN = 3.3 V, VSEL0 = H, MODE_SEL = L, FB1 = L



Note: UVLO deactive detection signal and RESETn deactive detection signal are internal signals.

Figure 8-6 Startup ON sequence (TC7738WBG-P00)

8.3.5. Protection function of output control part

(1) Output over voltage protection (OVP_2)
If the output voltage of DC-DC1 to 6 exceeds OVP operation threshold, MOSFET of LX pin high-side and low-side of the target DC-DC is turned OFF.
After the detection, when output voltage is dropping and over voltage state is reset, switching operation is restarted.

(2) Output under voltage protection (UVP)
If the output voltage of DC-DC1 to 6 is dropping less than UVP operation threshold, MOSFET of LX pin high-side and low-side of the target DC-DC is turned OFF and the state is held.
In order to reset, it is necessary to restart by register 09h (DC-DC*_EN=L to H), or to reset power supply.

(3) Output current limitation (OCL_2)
- DC-DC1 to 6
  In the overcurrent state, if the peak inductor current reaches OCL operation current, the output current is limited.
- LDO1, LDO2
  In the overcurrent state, OCL operation current of each LDO is limited and output voltage and current limitation value is dropping with the fold-back current characteristic.

8.3.6. Low power consumption mode

Low power mode (LPM) which is low power consumption operation of each channel can be set by registers.
For each current at a stationary time, refer to electric characteristics.

The operation state of DC-DC or LDO is enabled by the register DC-DCCTRL2_REG (0Bh) at SLEEP (0Ch, bit0) = 0, and is enabled by the register SLEEP_REG2 (0Dh) at SLEEP=1.

Table 8.7 Setting by SLEEP signal

SLEEP (0Ch,bit0)	DC-DC*_LPM, LDO*_LPM (0Bh, bit0 to bit7)	DC-DC*_ALIVE, LDO*_ALIVE (0Dh, bit0 to bit7)	DC-DC*/LDO* operation mode
0	0	X	High power mode
0	1	X	Low power mode
1	X	0	OFF
1	X	1	Low power mode

Note: The output current of each channel should be used at 100 mA or less in Low power mode.

8.4. Register

8.4.1. Register table

For the register table, refer to the following list.

Table 8.8 Register table

Address	Name	Setting
00h	DC-DC1_VSET_REG	The register to set DC-DC1 output level
01h	DC-DC2_VSET_REG	The register to set DC-DC2 output level
02h	DC-DC3_VSET_REG	The register to set DC-DC3 output level
03h	DC-DC4_VSET_REG	The register to set DC-DC4 output level
04h	DC-DC5_VSET_REG	The register to set DC-DC5 output level
05h	DC-DC6_VSET_REG	The register to set DC-DC6 output level
06h	LDO1_VSET_REG	The register to set LDO1 output level
07h	LDO2_VSET_REG	The register to set LDO2 output level
08h	LOADSW_CTRL_REG	The register to control LOAD-SW
09h	VOUT_CTRL_REG	The register to control each DC-DC and Enable/Disable of LDO
0Ah	DC-DCCTRL1_REG	The register to set pulse skip/PWM mode of each DC-DC
0Bh	DC-DCCTRL2_REG	The register to set High/Low power mode of each DC-DC and LDO
0Ch	SLEEP_REG1	The register to set SLEEP MODE
0Dh	SLEEP_REG2	The register to set the operation setting of each DC-DC and LDO in SLEEP MODE

8.4.2. DC-DC1 output voltage setting (Address 00h)

This is the register to set DC-DC1 output voltage

Table 8.9 DC-DC1_VSET_REG (00h)

Bit	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	Reserved				DC-DC1_VSET[3:0]			
Default	0	0	0	0	0	1	1	1
Read/Write	R	R	R	R	R/W	R/W	R/W	R/W

Table 8.10 DC-DC1 output voltage setting

Setting	CH	1	
	VSEL0	L	H
	MODE_SEL	X (Note1)	
DC-DC1_VSET[3:0]	0000	2.325 V	2.325 V
	0001	2.350 V	2.350 V
	0010	2.375 V	2.375 V
	0011	2.400 V	2.400 V
	0100	2.425 V	2.425 V
	0101	2.450 V	2.450 V
	0110	2.475 V	2.475 V
	0111(Note2)	**2.500 V**	**2.500 V**
	1000	2.525 V	2.525 V
	1001	2.550 V	2.550 V
	1010	2.575 V	2.575 V
	1011	2.600 V	2.600 V
	1100	2.625 V	2.625 V
	1101	2.650 V	2.650 V
	1110	2.675 V	2.675 V
	1111	2.700 V	2.700 V

Note1: When MODE_SEL = L, and FB1 is connected to GND, it is in BYPASS MODE.
Note2: Default output voltage according to VSEL0

8.4.3. DC-DC2 output voltage setting (Address 01h)

This is the register to set DC-DC2 output voltage.

Table 8.11 DC-DC2_VSET_REG (01h)

Bit	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	Reserved				DC-DC2_VSET[3:0]			
Default	0	0	0	0	0	1	1	1
Read/Write	R	R	R	R	R/W	R/W	R/W	R/W

Table 8.12 DC-DC2 output voltage setting

Setting	CH	2	
	VSEL0	L	H
	MODE_SEL	X	
DC-DC2_VSET[3:0]	0000	1.175 V	1.025 V
	0001	1.200 V	1.050 V
	0010	1.225 V	1.075 V
	0011	1.250 V	1.100 V
	0100	1.275 V	1.125 V
	0101	1.300 V	1.150 V
	0110	1.325 V	1.175 V
	0111(Note1)	**1.350 V**	**1.200 V**
	1000	1.375 V	1.225 V
	1001	1.400 V	1.250 V
	1010	1.425 V	1.275 V
	1011	1.450 V	1.300 V
	1100	1.475 V	1.325 V
	1101	1.500 V	1.350 V
	1110	1.525 V	1.375 V
	1111	1.550 V	1.400 V

Note1: Default output voltage according to VSEL0

8.4.4. DC-DC3 output voltage setting (Address 02h)

This is the register to set DC-DC3 output voltage.

Table 8.13 DC-DC3_VSET_REG (02h)

Bit	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	Reserved				DC-DC3_VSET[3:0]			
Default	0	0	0	0	0	1	1	1
Read/Write	R	R	R	R	R/W	R/W	R/W	R/W

Table 8.14 DC-DC3 output voltage setting

Setting	CH	3
	VSEL0	X
	MODE_SEL	X
DC-DC3_VSET[3:0]	0000	1.625 V
	0001	1.650 V
	0010	1.675 V
	0011	1.700 V
	0100	1.725 V
	0101	1.750 V
	0110	1.775 V
	0111(Note1)	**1.800 V**
	1000	1.825 V
	1001	1.850 V
	1010	1.875 V
	1011	1.900 V
	1100	1.925 V
	1101	1.950 V
	1110	1.975 V
	1111	2.000 V

Note1: Default output voltage

8.4.5. DC-DC4 output voltage setting (Address 03h)

This is the register to set DC-DC4 output voltage.

Table 8.15 DC-DC4_VSET_REG (03h)

Bit	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	Reserved				DC-DC4_VSET[3:0]			
Default	0	0	0	0	0	1	1	1
Read/Write	R	R	R	R	R/W	R/W	R/W	R/W

Table 8.16 DC-DC4 output voltage setting

Setting	CH	4	
	VSEL0	L	H
	MODE_SEL	X	
DC-DC4_VSET[3:0]	0000	0.825 V	1.625 V
	0001	0.850 V	1.650 V
	0010	0.875 V	1.675 V
	0011	0.900 V	1.700 V
	0100	0.925 V	1.725 V
	0101	0.950 V	1.750 V
	0110	0.975 V	1.775 V
	0111(Note1)	**1.000 V**	**1.800 V**
	1000	1.025 V	1.825 V
	1001	1.050 V	1.850 V
	1010	1.075 V	1.875 V
	1011	1.100 V	1.900 V
	1100	1.125 V	1.925 V
	1101	1.150 V	1.950 V
	1110	1.175 V	1.975 V
	1111	1.200 V	2.000 V

Note1: Default output voltage according to VSEL0

8.4.6. DC-DC5 output voltage setting (Address 04h)

This is the register to set DC-DC5 output voltage.

Table 8.17 DC-DC5_VSET_REG (04h)

Bit	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	Reserved				DC-DC5_VSET[3:0]			
Default	0	0	0	0	0	1	1	1
Read/Write	R	R	R	R	R/W	R/W	R/W	R/W

Table 8.18 DC-DC5 output voltage setting

Setting	CH	5	
	VSEL0	L	H
	MODE_SEL	X	
DC-DC5_VSET[3:0]	0000	0.825 V	0.725 V
	0001	0.850 V	0.750 V
	0010	0.875 V	0.775 V
	0011	0.900 V	0.800 V
	0100	0.925 V	0.825 V
	0101	0.950 V	0.850 V
	0110	0.975 V	0.875 V
	0111(Note1)	**1.000 V**	**0.900 V**
	1000	1.025 V	0.925 V
	1001	1.050 V	0.950 V
	1010	1.075 V	0.975 V
	1011	1.100 V	1.000 V
	1100	1.125 V	1.025 V
	1101	1.150 V	1.050 V
	1110	1.175 V	1.075 V
	1111	1.200 V	1.100 V

Note1: Default output voltage according to VSEL0

8.4.7. DC-DC6 output voltage setting (Address 05h)

This is the register to set DC-DC6 output voltage.

Table 8.19 DC-DC6_VSET_REG (05h)

Bit	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	Reserved				DC-DC6_VSET[3:0]			
Default	0	0	0	0	0	1	1	1
Read/Write	R	R	R	R	R/W	R/W	R/W	R/W

Table 8.20 DC-DC6 output voltage setting

Setting	CH	6	
	VSEL0	L	H
	MODE_SEL	X	
DC-DC6_VSET[3:0]	0000	0.825 V	0.725 V
	0001	0.850 V	0.750 V
	0010	0.875 V	0.775 V
	0011	0.900 V	0.800 V
	0100	0.925 V	0.825 V
	0101	0.950 V	0.850 V
	0110	0.975 V	0.875 V
	0111(Note1)	**1.000 V**	**0.900 V**
	1000	1.025 V	0.925 V
	1001	1.050 V	0.950 V
	1010	1.075 V	0.975 V
	1011	1.100 V	1.000 V
	1100	1.125 V	1.025 V
	1101	1.150 V	1.050 V
	1110	1.175 V	1.075 V
	1111	1.200 V	1.100 V

Note1: Default output voltage according to VSEL0

8.4.8. LDO1 output voltage setting (Address 06h)

This is the register to set LDO1 output voltage.

Table 8.21 LDO1_VSET_REG (06h)

Bit	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	Reserved				LDO1_VSET[3:0]			
Default	0	0	0	0	0	1	1	1
Read/Write	R	R	R	R	R/W	R/W	R/W	R/W

Table 8.22 LDO1 output voltage setting

Setting	CH	LDO1	
	VSEL0	L	H
	MODE_SEL	X	
LDO1_VSET[3:0]	0000	2.325 V	1.625 V
	0001	2.350 V	1.650 V
	0010	2.375 V	1.675 V
	0011	2.400 V	1.700 V
	0100	2.425 V	1.725 V
	0101	2.450 V	1.750 V
	0110	2.475 V	1.775 V
	0111(Note1)	**2.500 V**	**1.800 V**
	1000	2.525 V	1.825 V
	1001	2.550 V	1.850 V
	1010	2.575 V	1.875 V
	1011	2.600 V	1.900 V
	1100	2.625 V	1.925 V
	1101	2.650 V	1.950 V
	1110	2.675 V	1.975 V
	1111	2.700 V	2.000 V

Note1: Default output voltage according to VSEL0

8.4.9. LDO2 output voltage setting (Address 07h)

This is the register to set LDO2 output voltage.

Table 8.23 LDO2_VSET_REG (07h)

Bit	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	Reserved				LDO2_VSET[3:0]			
Default	0	0	0	0	0	1	1	1
Read/Write	R	R	R	R	R/W	R/W	R/W	R/W

Table 8.24 LDO2 output voltage setting

Setting	CH	LDO2	
	VSEL0	X	
	MODE_SEL	L	Open
LDO2_VSET[3:0]	0000	BYPASS MODE	3.125 V
	0001		3.150 V
	0010		3.175 V
	0011		3.200 V
	0100		3.225 V
	0101		3.250 V
	0110		3.275 V
	0111(Note1)		**3.300 V**
	1000		3.325 V
	1001		3.350 V
	1010		3.375 V
	1011		3.400 V
	1100		3.425 V
	1101		3.450 V
	1110		3.475 V
	1111		3.500 V

Note: Default output voltage according to MODE_SEL

8.4.10. LOAD-SW setting (Address 08h)

This is the register to set LOAD-SW.

Table 8.25 LOAD-SW_CTRL_REG (08h)

Bit	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	Reserved							LDSW-ON
Default	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R/W

Table 8.26 LOAD-SW control

LDSW_ON	Description
0	LOAD -SW OFF
1	LOAD -SW ON

8.4.11. Output setting of DC-DC and LDO (Address 09h)

This is the register to control Enable/Disable of each DC-DC and LDO.

Table 8.27 VOUT_CTRL_REG (09h)

Bit	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	DC-DC1 _EN	DC-DC2 _EN	DC-DC3 _EN	DC-DC4 _EN	DC-DC5 _EN	DC-DC6 _EN	LDO1 _EN	LDO2 _EN
Default	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 8.28 Output setting of DC-DC and LDO

・DC-DC1 Enable / Disable setting

DC-DC1_EN	Description
0	DC-DC1 Disable
1	DC-DC1 Enable

・DC-DC2 Enable / Disable setting

DC-DC2_EN	Description
0	DC-DC2 Disable
1	DC-DC2 Enable

・DC-DC3 Enable / Disable setting

DC-DC3_EN	Description
0	DC-DC3 Disable
1	DC-DC3 Enable

・DC-DC4 Enable / Disable setting

DC-DC4_EN	Description
0	DC-DC4 Disable
1	DC-DC4 Enable

・DC-DC5 Enable / Disable setting

DC-DC5_EN	Description
0	DC-DC5 Disable
1	DC-DC5 Enable

・DC-DC6 Enable / Disable setting

DC-DC6_EN	Description
0	DC-DC6 Disable
1	DC-DC6 Enable

・LDO1 Enable / Disable setting

LDO1_EN	Description
0	LDO1 Disable
1	LDO1 Enable

・LDO2 Enable / Disable setting

LDO2_EN	Description
0	LDO2 Disable
1	LDO2 Enable

8.4.12. DC-DC pulse skip / PWM mode setting (Address 0Ah)

This is the register to select each DC-DC pulse skip or PWM mode setting.

Table 8.29 DC-DCCTRL1_REG (0Ah)

Bit	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	DC-DC1 _PWM	DC-DC2 _PWM	DC-DC3 _PWM	DC-DC4 _PWM	DC-DC5 _PWM	DC-DC6 _PWM	Reserved	
Default	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Table 8.30 DC-DC pulse skip / PWM mode setting

・DC-DC1 Enable / Disable setting

DC-DC1_PWM	Description
0	DC-DC1 pulse skip mode
1	DC-DC1 PWM mode

・DC-DC2 Enable / Disable setting

DC-DC2_PWM	Description
0	DC-DC2 pulse skip mode
1	DC-DC2 PWM mode

・DC-DC3 Enable / Disable setting

DC-DC3_PWM	Description
0	DC-DC3 pulse skip mode
1	DC-DC3 PWM mode

・DC-DC4 Enable / Disable setting

DC-DC4_PWM	Description
0	DC-DC4 pulse skip mode
1	DC-DC4 PWM mode

・DC-DC5 Enable / Disable setting

DC-DC5_PWM	Description
0	DC-DC5 pulse skip mode
1	DC-DC5 PWM mode

・DC-DC6 Enable / Disable setting

DC-DC6_PWM	Description
0	DC-DC6 pulse skip mode
1	DC-DC6 PWM mode

8.4.13. DC-DC Low power mode setting (Address 0Bh)

This is the register to select High power / Low power mode of each DC-DC.

Table 8.31 DC-DCCTRL2_REG (0Bh)

Bit	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	DC-DC1 _LPM	DC-DC2 _LPM	DC-DC3 _LPM	DC-DC4 _LPM	DC-DC5 _LPM	DC-DC6 _LPM	LDO1 _LPM	LDO2 _LPM
Reset	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The setting of High power mode / Low power mode by this register is enabled only SLEEP = 0.

Table 8.32 High / Low power mode setting of DC-DC and LDO

・DC-DC1 High / Low power mode setting

DC-DC1_LPM	Description
0	DC-DC1 High power mode
1	DC-DC1 Low power mode

・DC-DC2 High / Low power mode setting

DC-DC2_LPM	Description
0	DC-DC2 High power mode
1	DC-DC2 Low power mode

・DC-DC3 High / Low power mode setting

DC-DC3_LPM	Description
0	DC-DC3 High power mode
1	DC-DC3 Low power mode

・DC-DC4 High / Low power mode setting

DC-DC4_LPM	Description
0	DC-DC4 High power mode
1	DC-DC4 Low power mode

・DC-DC5 High / Low power mode setting

DC-DC5_LPM	Description
0	DC-DC5 High power mode
1	DC-DC5 Low power mode

・DC-DC6 High / Low power mode setting

DC-DC6_LPM	Description
0	DC-DC6 High power mode
1	DC-DC6 Low power mode

・LDO1 High / Low power mode setting

LDO1_LPM	Description
0	LDO1 High power mode
1	LDO1 Low power mode

・LDO2 High / Low power mode setting

LDO2_LPM	Description
0	LDO2 High power mode
1	LDO2 Low power mode

8.4.14. SLEEP MODE setting (Address 0Ch)

This is the register to set SLEEP MODE.

Table 8.33 SLEEP_REG1 (0Ch)

Bit	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	Reserved							SLEEP
Reset	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R/W

Table 8.34 SLEEP MODE setting

SLEEP	Description
0	End of SLEEP MODE
1	Move to SLEEP MODE

8.4.15. SLEEP MODE setting (Address 0Dh)

This is the register to set each DC-DC and LDO state in SLEEP MODE.

Table 8.35 SLEEP_REG2 (0Dh)

Bit	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	DC-DC1 _ALIVE	DC-DC2 _ALIVE	DC-DC3 _ALIVE	DC-DC4 _ALIVE	DC-DC5 _ALIVE	DC-DC6 _ALIVE	LDO1 _ALIVE	LDO2 _ALIVE
Reset	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 8.36 DC-DC and LDO SLEEP MODE setting

・DC-DC1 SLEEP MODE setting

DC-DC1_ALIVE	Description
0	When SLEEP =1, DC-DC1 operation is OFF.
1	When SLEEP =1, DC-DC1 operates in Low power mode.

・DC-DC2 SLEEP MODE setting

DC-DC2_ALIVE	Description
0	When SLEEP =1, DC-DC2 operation is OFF.
1	When SLEEP =1, DC-DC2 operates in Low power mode.

・DC-DC3 SLEEP MODE setting

DC-DC3_ALIVE	Description
0	When SLEEP =1, DC-DC3 operation is OFF.
1	When SLEEP =1, DC-DC3 operates in Low power mode.

・DC-DC4 SLEEP MODE setting

DC-DC4_ALIVE	Description
0	When SLEEP =1, DC-DC4 operation is OFF.
1	When SLEEP =1, DC-DC4 operates in Low power mode.

・DC-DC5 SLEEP MODE setting

DC-DC5_ALIVE	Description
0	When SLEEP =1, DC-DC5 operation is OFF.
1	When SLEEP =1, DC-DC5 operates in Low power mode.

・DC-DC6 SLEEP MODE setting

DC-DC6_ALIVE	Description
0	When SLEEP =1, DC-DC6 operation is OFF.
1	When SLEEP =1, DC-DC6 operates in Low power mode.

・LDO1 SLEEP MODE setting

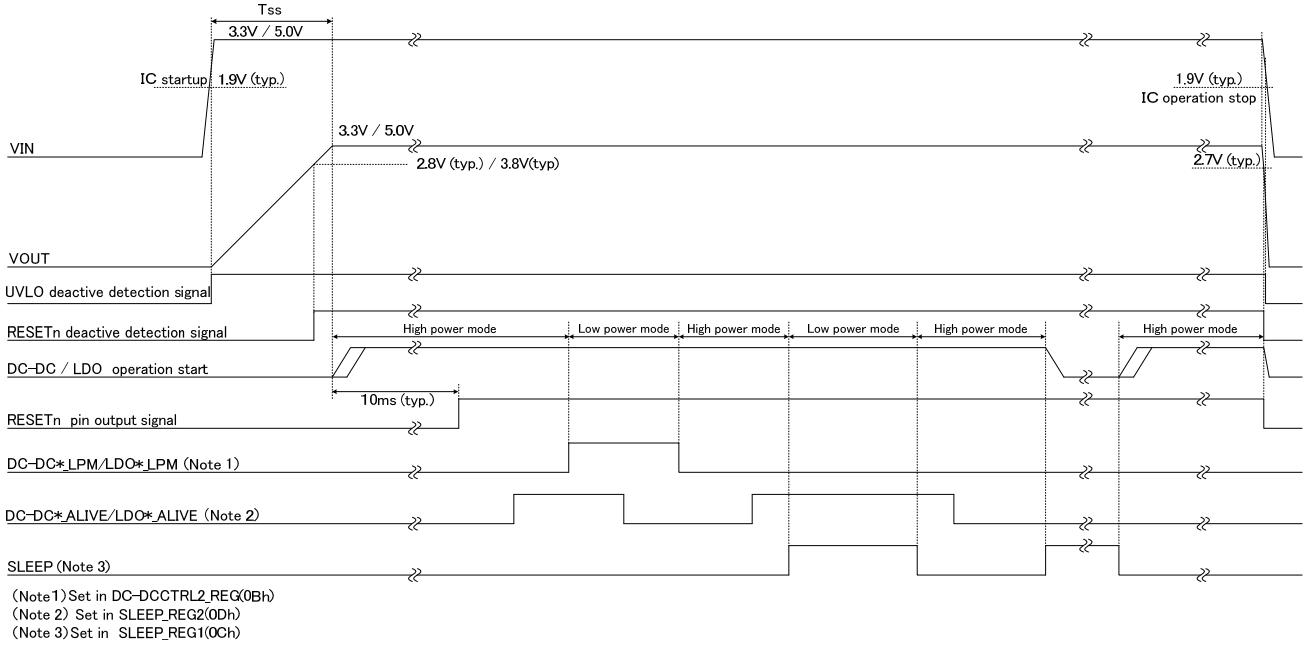
LDO1_ALIVE	Description
0	When SLEEP =1, LDO1 operation is OFF.
1	When SLEEP =1, LDO1 operates in Low power mode.

・LDO2 SLEEP MODE setting

LDO2_ALIVE	Description
0	When SLEEP =1, LDO2 operation is OFF.
1	When SLEEP =1, LDO2 operates in Low power mode.

Sequence example in the case of SLEEP MODE ON or OFF

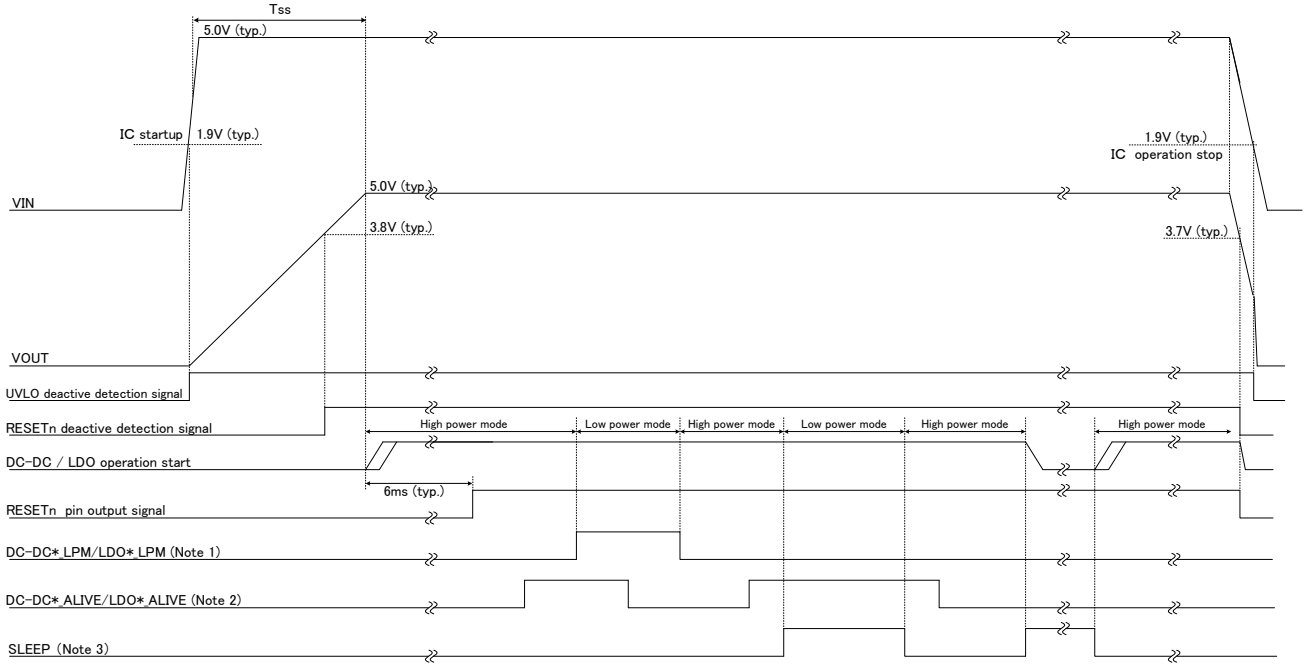
(1) VSEL0 = “L”, MODE_SEL = “L”



(Note1) Set in DC-DCCTRL2_REG(0Bh)
(Note 2) Set in SLEEP_REG2(0Dh)
(Note 3) Set in SLEEP_REG1(0Ch)

Figure 8-7 Sequence example 1 in the case of SLEEP MODE ON or OFF

(2) VSEL0 = “H”, MODE_SEL = “Open”



(Note1) Set in DC-DCCTRL2_REG(0Bh)
(Note 2) Set in SLEEP_REG2(0Dh)
(Note 3) Set in SLEEP_REG1(0Ch)

Figure 8-8 Sequence example 2 in the case of SLEEP MODE ON or OFF

8.5. I^2C interface

TC7738WBG sets each function setting using the I^2C interface.
As shown in the following, pull up SCL pin and SDA pin at external of IC, and connect to an input device.

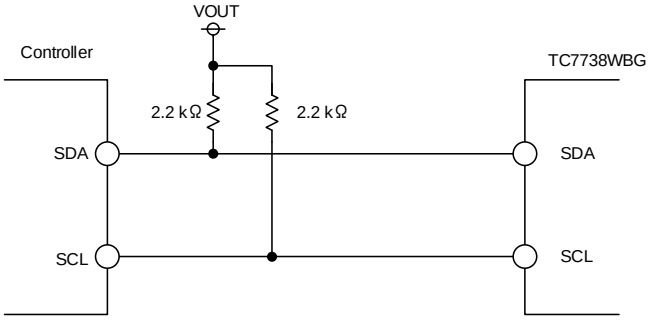


Figure 8-9 I^2C bus connection

The Interface of this product supports the following modes compliant with I^2C standard: Slave mode, Fast mode (400 kHz), and High speed mode (3.4 MHz), and they can perform the single write operation, continuous write operation, single read operation, and continuous read operation. The slave address of TC7738WBG is fixed to 0b1001101.

Table 8.37 I^2C interface description

Symbol	Description
S	Start condition
Sr	Repetitive start condition
Slave Address	Slave address (7 bit):0b1001101
R	Read mode (R/W=1)
W	Write mode (R/W=0)
A	Acknowledge signal (L level output)
NA	Non acknowledge signal (HiZ output)
P	Stop condition

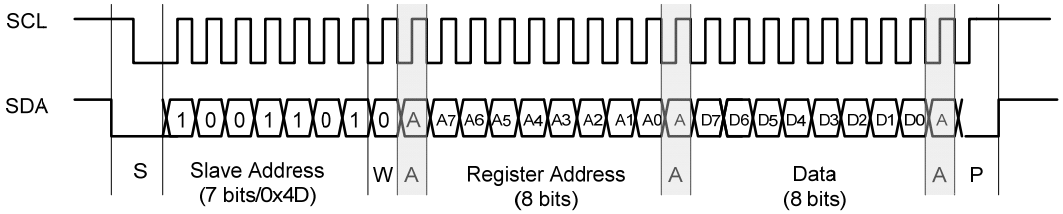


Figure 8-10 Single write mode

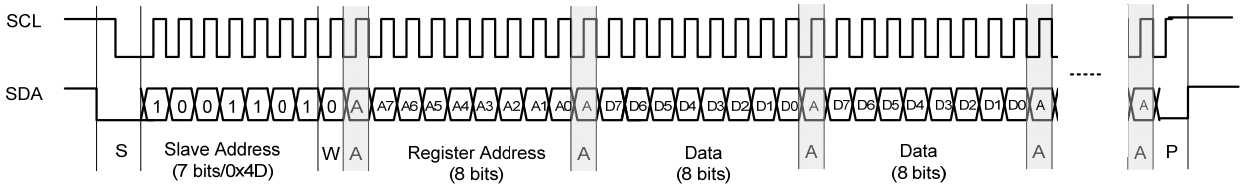


Figure 8-11 Continuous write mode

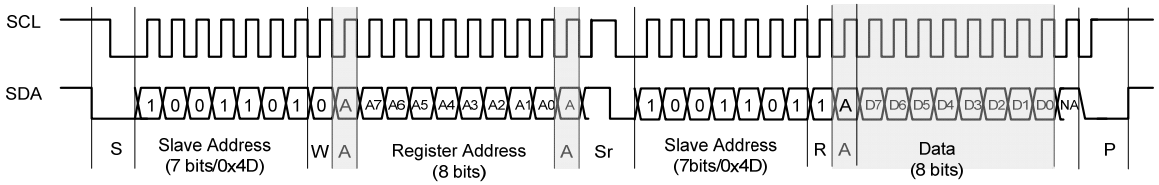


Figure 8-12 Single read mode

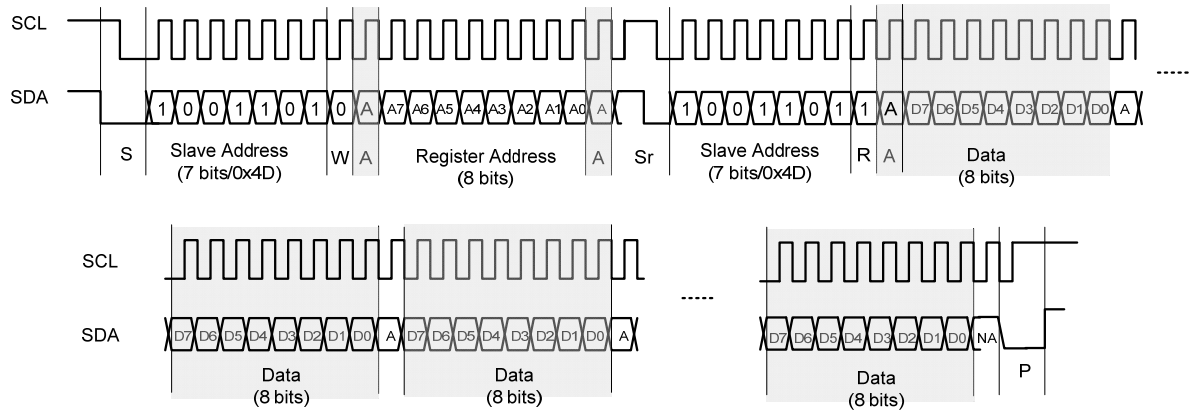


Figure 8-13 Continuous read mode

Note: In the case of ACK = "1," the controller should perform the stop condition.

Note: When the stop condition is recognized, TC7738WBG release SDA pin and waits for the start condition.
If it is accessing at this time, the transfer data is discarded, and the clock count is initialized.

Note: If the command is interrupted on the way, the command before being interrupted is reflected, and the interrupted command is not executed.
To reflect the command, set the command setting again.

Note: Although the I^2C communication is not received if the RESETn pin is “L” state, confirm the “H” state and start the communication.

9. Absolute maximum ratings (Unless otherwise specified, Ta=25°C)

Table 9.1 Absolute maximum ratings

Item	Symbol	Rating	Unit
Power supply voltage	VIN	7.0	V
Each pin maximum applied voltage	ViMAX	6.0	V
Each pin minimum applied voltage	ViMIN	GND - 0.3	V
Power dissipation (Note1)	P_D	2715	mW
Saturation heat resistance	Rth (j-a)	46.3	°C/W
Ambient temperature in operation	T_{opr}	-40 to 85	°C
Storage temperature	T_{stg}	-55 to 150	°C
Junction temperature	T_j	150	°C

Note1: Board condition: JEDEC 4 layers 76.2 mm × 114.3 mm × 1.6 mm

10. Power dissipation

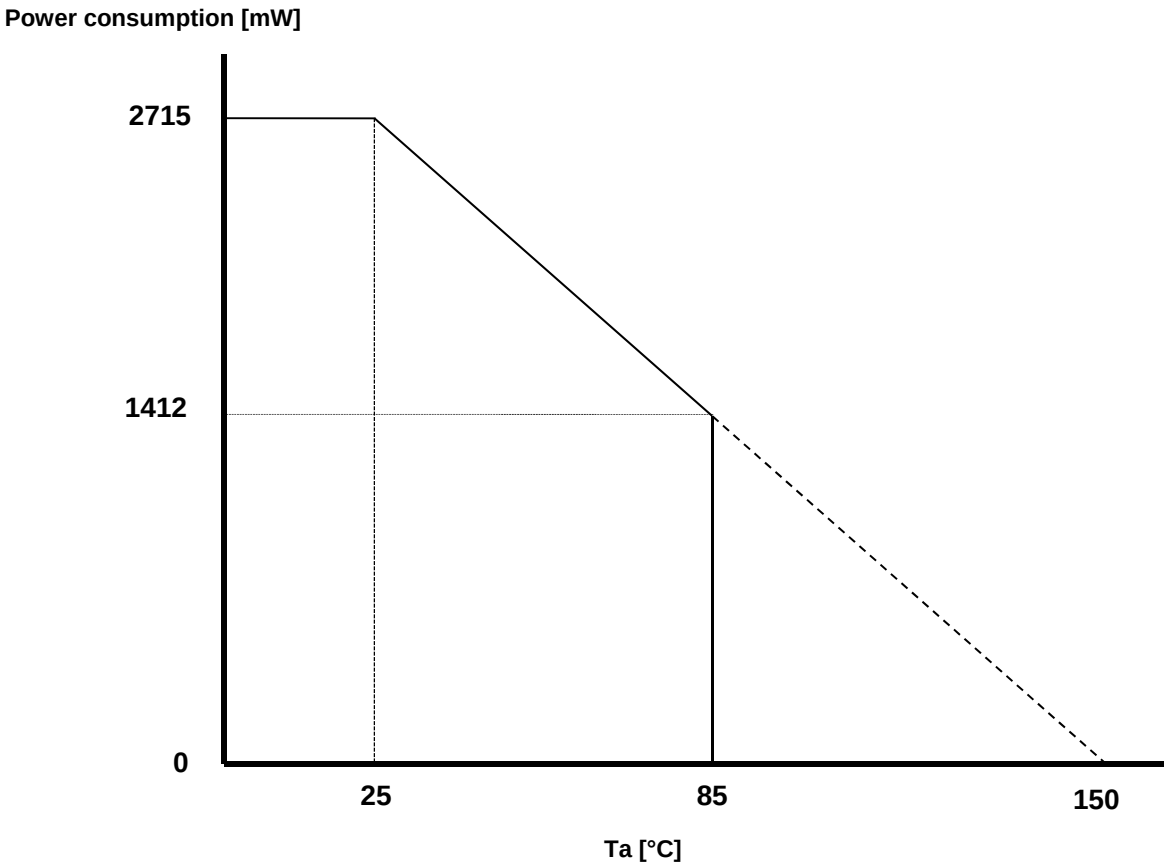


Figure 10-1 Temperature reduction curve of power consumption

11. Electric characteristic

11.1. Common characteristic (Unless otherwise specified, Ta = 25°C, VIN = 3.3 V)

Item	Symbol	Note	Min	Typ.	Max	Unit
< UVLO, OVP_1 of VIN =3.3 V setting>						
Power supply voltage (Note 1)	Vin33	MODE_SEL =“L” (VIN = 3.3 V setting)	2.9	3.3	3.6	V
Current consumption	Iin33_1	High power mode, ALL CH:ON/ No load	—	370	520	μA
	Iin33_2	SLEEP MODE, ALL CH: OFF	—	85	105	μA
	Iin33_3	SLEEP MODE, CH5:ACTIVE, other CH:OFF	—	100	125	μA
OVP_1 detection voltage	Vovp-on33	Rising	3.8	3.9	4.0	V
OVP_1 hysteresis voltage	Vovp1-on33hisy	—	—	100	—	mV
< UVLO, OVP_1 of VIN = 5.0 V setting>						
Power supply voltage (Note 1)	Vin50	MODE_SEL = Open (VIN = 5.0 V setting)	4.0	5.0	5.5	V
Current consumption	Iin50_1	High power mode, ALL CH:ON/ No load	—	465	650	μA
	Iin50_2	SLEEP MODE, ALL CH: OFF	—	100	125	μA
	Iin50_3	SLEEP MODE, CH5:ACTIVE, other CH:OFF	—	120	150	μA
OVP_1 detection voltage	Viovp-on50	Rising	5.6	5.8	6.0	V
OVP_1 hysteresis voltage	Vovp1-on50hisy	—	—	100	—	mV
< PROTECTION-SW >						
UVLO detection voltage	Vuvlop	Falling/Rising	—	1.9	—	V
OCL_1 operation current	Iocl-on	—	4.5	—	—	A
Protection switch ON resistance	Ron_pro	—	—	20	—	mΩ
Current limitaion at soft start	Iss_pro	—	100	130	200	mA
< Input pin (MODE_SEL and VSEL0 pin) >						
“H” level input voltage	VIH33	VSEL0, VIN = 3.3 V	1.2	—	—	V
	VIH50	VSEL0, VIN = 5.0 V	1.5	—	—	
“L” level input voltage	VIL	MODE_SEL, VSEL0	—	—	0.4	V
“H” level input current	IIH-vsel0	VSEL0, pin voltage = 3.3 V	—	1.65	2.0	μA
“L” level input current	IIL-vsel0	VSEL0, pin voltage = 0 V	-1.0	—	—	μA
	IIL-mode_sel	MODE_SEL, pin voltage = 0 V	—	1.3	1.6	
< RESETn >						
RESETn detection voltage	Vpor33-on	MODE_SEL =“L”(VIN = 3.3 V setting) ,Falling	2.673	2.700	2.727	V
	Vpor50-on	MODE_SEL = “Open“(VIN = 5.0 V setting), Falling	3.663	3.700	3.737	
RESETn hysteresis voltage	Vpor-hys	—	—	100	—	mV
RESETn “L” to “H” Delay time	Tpor-on0	VSEL0 = “L”	9	10	11	ms
	Tpor-on1	VSEL0 = “H”	5	6	7	
RESETn pin (“L”) voltage	Vporn	In the case of RESETn= “L”, Sink current = 4 mA	—	—	0.4	V
<Thermal shutdown (TSD)>						
Overheat protection operation temperature	Ttsd-on	—	—	140	—	°C
Overheat protection hysteresis	Ttsd-hys	—	—	20	—	°C

Note 1: It is a power supply voltage range required in order to operate this IC stably. Booting starts with VIN =2.6 V (MAX) in the case of MODE_SEL =“L”, and with VIN = 3.4 V (MAX) in the case of MODE_SEL =“Open”.

11.2. CH1 characteristic (Unless otherwise specified, Ta = 25°C, VIN = 3.3 V)

Item	Symbol	Note	Min	Typ.	Max	Unit
< DC-DC1 (4.0 A MAX) >						
Current consumption (1)	IpVIN1_ch1	High power mode, output stage OFF	—	30	—	μA
Current consumption (2)	IpVIN2_ch1	Low power mode, output stage OFF	—	20	—	μA
Output voltage variable range	VrngX_ch1	VSEL0 = “X”, I^2C control, PWM mode	2.325	—	2.700	V
Output voltage initial value	VdefX_ch1	VSEL0 = “X”, PWM mode	2.45	2.50	2.55	V
Output voltage variable step voltage	Vstep_ch1	PWM mode	—	25	—	mV
Line regulation	Regli_ch1	PWM mode	—	0.5	—	%/V
Load regulation	Reglo_ch1	PWM mode	—	0.5	—	%/A
High side ON resistance	Ronh_ch1	V(PVIN1) = 5.0 V	—	45	—	mΩ
Low side ON resistance	Ronl_ch1	V(PVIN1) = 5.0 V	—	25	—	mΩ
OCL_2 operation current	Iocp_ch1	—	5.0	—	—	A
Switching frequency	Fsw_ch1	—	2.7	3.0	3.3	MHz
Output OVP_2 operation threshold	Vovp_ch1	—	115	120	125	%
Output UVP operation threshold	Vuvp_ch1	—	55	60	65	%
Soft start time	Tss_ch1	—	—	0.5	0.8	ms
Electric discharge resistance	Rdis_ch1	—	—	50	—	Ω
< BYPASS-SW1 >						
Switch ON resistance	Ron_bpsw1	—	—	55	—	mΩ
OCL_2 operation; current	Iocl_bpsw1	—	5.0	—	—	A

11.3. CH2 characteristic (Unless otherwise specified, Ta = 25°C, VIN = 3.3 V)

Item	Symbol	Note	Min	Typ.	Max	Unit
< DC-DC2 (1.0 A MAX) >						
Current consumption (1)	IpVIN1_ch2	High power mode, output stage OFF	—	30	—	μA
Current consumption (2)	IpVIN2_ch2	Low power mode, output stage OFF	—	20	—	μA
Output voltage variable range	Vrng0_ch2	VSEL0 = “L”, I^2C control, PWM mode	1.175	—	1.550	V
	Vrng1_ch2	VSEL0 = “H”, I^2C control, PWM mode	1.025	—	1.400	
Output voltage initial value	Vdef0_ch2	VSEL0 = “L”, PWM mode	1.32	1.35	1.38	V
	Vdef1_ch2	VSEL0 = “H”, PWM mode	1.17	1.20	1.23	
Output voltage variable step voltage	Vstep_ch2	PWM mode	—	25	—	mV
Line regulation	Regli_ch2	PWM mode	—	0.5	—	%/V
Load regulation	Reglo_ch2	PWM mode	—	0.5	—	%/A
High side ON resistance	Ronh_ch2	V(PVIN2) = 5.0 V	—	55	—	mΩ
Low side ON resistance	Ronl_ch2	V(PVIN2) = 5.0 V	—	35	—	mΩ
OCL_2 operation current	Iocp_ch2	—	2.0	—	—	A
Switching frequency	Fsw_ch2	—	2.7	3.0	3.3	MHz
Output OVP_2 operation threshold	Vovp_ch2	—	115	125	135	%
Output UVP operation threshold	Vuvp_ch2	—	55	60	65	%
Soft start time	Tss_ch2	—	—	0.5	0.8	ms
Electric discharge resistance	Rdis_ch2	—	—	200	—	Ω

11.4. CH3 characteristic (Unless otherwise specified, Ta = 25°C, VIN = 3.3 V)

Item	Symbol	Note	Min	Typ.	Max	Unit
< DC-DC3 (2.0 A MAX) >						
Current consumption (1)	IpVIN1_ch3	High power mode, output stage OFF	—	30	—	μA
Current consumption (2)	IpVIN2_ch3	Low power mode, output stage OFF	—	20	—	μA
Output voltage variable range	VrngX_ch3	VSEL0 = “X”, I^2C control, PWM mode	1.625	—	2.0	V
Output voltage initial value	VdefX_ch3	VSEL0 = “X”, PWM mode	1.76	1.80	1.84	V
Output voltage variable step voltage	Vstep_ch3	PWM mode	—	25	—	mV
Line regulation	Regli_ch3	PWM mode	—	0.5	—	%/V
Load regulation	Reglo_ch3	PWM mode	—	0.5	—	%/A
High side ON resistance	Ronh_ch3	V(PVIN3) = 5.0 V	—	55	—	mΩ
Low side ON resistance	Ronl_ch3	V(PVIN3) = 5.0 V	—	35	—	mΩ
OCL_2 operation current	Iocp_ddc3	—	3.5	—	—	A
Switching frequency	Fsw_ch3	—	2.7	3.0	3.3	MHz
Output OVP_2 operation threshold	Vovp_ch3	—	120	125	130	%
Output UVP operation threshold	Vuvp_ch3	—	55	60	65	%
Soft start time	Tss_ch3	—	—	0.5	0.8	ms
Electric discharge resistance	Rdis_ch3	—	—	100	—	Ω

11.5. CH4 characteristic (Unless otherwise specified, Ta = 25°C, VIN = 3.3 V)

Item	Symbol	Note	Min	Typ.	Max	Unit
< DC-DC4 (1.0 A MAX) >						
Current consumption (1)	IpVIN1_ch4	High power mode, output stage OFF	—	30	—	μA
Current consumption (2)	IpVIN2_ch4	Low power mode, output stage OFF	—	20	—	μA
Output voltage variable range	Vrng0_ch4	VSEL0 = “L”, I^2C control, PWM mode	0.825	—	1.200	V
	Vrng1_ch4	VSEL0 = “H”, I^2C control, PWM mode	1.625	—	2.000	
Output voltage initial value	Vdef0_ch4	VSEL0 = “L”, PWM mode	0.98	1.00	1.02	V
	Vdef1_ch4	VSEL0 = “H”, PWM mode	1.76	1.80	1.84	
Output voltage variable step voltage	Vstep_ch4	PWM mode	—	25	—	mV
Line regulation	Regli_ch4	PWM mode	—	0.5	—	%/V
Load regulation	Reglo_ch4	PWM mode	—	0.5	—	%/A
High side ON resistance	Ronh_ch4	V(PVIN4) = 5.0 V	—	65	—	mΩ
Low side ON resistance	Ronl_ch4	V(PVIN4) = 5.0 V	—	40	—	mΩ
OCL_2 operation current	Iocp_ch4	—	2.0	—	—	A
Switching frequency	Fsw_ch4	—	2.7	3.0	3.3	MHz
Output OVP_2 operation threshold	Vovp_ch4	—	115	125	135	%
Output UVP operation threshold	Vuvp_ch4	—	55	60	65	%
Soft start time	Tss_ch4	—	—	0.5	0.8	ms
Electric discharge resistance	Rdis_ch4	—	—	200	—	Ω

11.6. CH5 characteristic (Unless otherwise specified, Ta = 25°C, VIN = 3.3 V)

Item	Symbol	Note	Min	Typ.	Max	Unit
< DC-DC5 (1.0 A MAX) >						
Current consumption (1)	IpVIN1_ch5	High power mode, output stage OFF	—	30	—	μA
Current consumption (2)	IpVIN2_ch5	Low power mode, output stage OFF	—	20	—	μA
Output voltage variable range	Vrng0_ch5	VSEL0 = “L”, I^2C control, PWM mode	0.825	—	1.200	V
	Vrng1_ch5	VSEL0 = “H”, I^2C control, PWM mode	0.725	—	1.100	
Output voltage initial value	Vdef0_ch5	VSEL0 = “L”, PWM mode	0.99	1.00	1.01	V
	Vdef1_ch5	VSEL0 = “H”, PWM mode	0.89	0.90	0.91	
Output voltage variable step voltage	Vstep_ch5	PWM mode	—	25	—	mV
Line regulation	Regli_ch5	PWM mode	—	0.5	—	%/V
Load regulation	Reglo_ch5	PWM mode	—	0.5	—	%/A
High side ON resistance	Ronh_ch5	V(PVIN5) = 5.0 V	—	65	—	mΩ
Low side ON resistance	Ronl_ch5	V(PVIN5) = 5.0 V	—	40	—	mΩ
OCL_2 operation current	Iocp_ch5	—	2.0	—	—	A
Switching frequency	Fsw_ch5	—	2.7	3.0	3.3	MHz
Output OVP_2 operation threshold	Vovp_ch5	—	115	125	135	%
Output UVP operation threshold	Vuvp_ch5	—	55	60	65	%
Soft start time	Tss_ch5	—	—	0.5	0.8	ms
Electric discharge resistance	Rdis_ch5	—	—	300	—	Ω
< LOAD-SW >						
Soft start time	Tss_ldsw	0 V to 0.9 V	—	0.36	—	ms
Switch ON resistance	Ron_ldsw	—	—	40	—	mΩ
OCL_3 operation current	Iocl_ldsw	Shutdown operation	550	—	—	mA
Electric discharge resistance	Rdis_ldsw	—	—	140	—	Ω

11.7. CH6 characteristic (Unless otherwise specified, Ta = 25°C, VIN = 3.3 V)

Item	Symbol	Note	Min	Typ.	Max	Unit
< DC-DC6 (3.5 A MAX) >						
Current consumption (1)	IpVIN1_ch6	High power mode, output stage OFF	—	30	—	μA
Current consumption (2)	IpVIN2_ch6	Low power mode, output stage OFF	—	20	—	μA
Output voltage variable range	Vrng0_ch6	VSEL0 = “L”, I^2C control, PWM mode	0.825	—	1.200	V
	Vrng1_ch6	VSEL0 = “H”, I^2C control, PWM mode	0.725	—	1.100	
Output voltage initial value	Vdef0_ch6	VSEL0 = “L”, PWM mode	0.98	1.00	1.02	V
	Vdef1_ch6	VSEL0 = “H”, PWM mode	0.88	0.90	0.92	
Output voltage variable step voltage	Vstep_ch6	PWM mode	—	25	—	mV
Line regulation	Regli_ch6	PWM mode	—	0.5	—	%/V
Load regulation	Reglo_ch6	PWM mode	—	0.5	—	%/A
High side ON resistance	Ronh_ch6	V(PVIN6) = 5.0 V	—	50	—	mΩ
Low side ON resistance	Ronl_ch6	V(PVIN6) = 5.0 V	—	25	—	mΩ
OCL_2 operation current	Iocp_ch6	—	4.5	—	—	A
Switching frequency	Fsw_ch6	—	2.7	3.0	3.3	MHz
Output OVP_2 operation threshold	Vovp_ch6	—	115	125	135	%
Output UVP operation threshold	Vuvp_ch6	—	55	60	65	%
Soft start time	Tss_ch6	—	—	0.5	0.8	ms
Electric discharge resistance	Rdis_ch6	—	—	150	—	Ω

11.8. LDO1 characteristic (Unless otherwise specified, Ta = 25°C, VIN = 3.3 V)

Item	Symbol	Note	Min	Typ.	Max	Unit
< LDO1 (0.3 A MAX) >						
Current consumption	I_ldo1in	No load	—	17	—	μA
Output voltage variable range	Vrng0_ldo1	VSEL0 = “L”, I^2C control	2.325	—	2.700	V
	Vrng1_ldo1	VSEL0 = “H”, I^2C conrol	1.625	—	2.000	
Output voltage initial value	Vdef0_ldo1	VSEL0 = “L”	2.45	2.50	2.55	V
	Vdef1_ldo1	VSEL0 = “H”	1.76	1.80	1.84	
Output voltage variable step voltage	Vstep_ldo1	—	—	25	—	mV
Line regulation	Regli_ldo1	—	—	0.5	—	%/V
Load regulation	Reglo_ldo1	—	—	0.5	—	%/A
OCL_2 operation current	Iocp_ldo1	—	0.3	0.4	—	A
Output short-circuit current	Ishort_ldo1	Fold-back characteristic	—	30	—	mA
Soft start time	Tss_ldo1	EN to 95 %	—	0.3	0.6	ms
Electric discharge resistance	Rdis_ldo1	—	—	200	—	Ω

11.9. LDO2 characteristic (Unless otherwise specified, Ta = 25°C, VIN = 3.3 V)

Item	Symbol	Note	Min	Typ.	Max	Unit
< LDO2 (0.3 A MAX) > MODE_SEL = “Open”(VIN = 5.0 V setting)						
Current consumption	I_ldo2in	No load	—	17	—	μA
Output voltage variable range	VrngX_ldo2	VSEL0 = “X”, I^2C control	3.125	—	3.500	V
Output voltage initial value	VdefX_ldo2	VSEL0 = “X”	3.23	3.30	3.37	V
Output voltage variable step voltage	Vstep_ldo2	—	—	25	—	mV
Line regulation	Regli_ldo2	—	—	0.5	—	%/V
Load regulation	Reglo_ldo2	—	—	0.5	—	%/A
OCL_2 operation current	Iocp_ldo2	—	0.3	0.4	—	A
Output short-circuit current	Ishort_ldo2	Fold-back characteristic	—	30	—	mA
Soft start time	Tss_ldo2	EN to 95 %	—	0.3	0.6	ms
Electric discharge resistance	Rdis_ldo2	—	—	200	—	Ω
< BYPASS-SW2 > MODE_SEL = “L” (VIN = 3.3 V setting)						
Switch ON resistance	Ron_bpsw2	—	—	450	—	mΩ
OCL_2 operation current	Iocl_bpsw2	—	0.3	—	—	A

11.10. AC characteristic (Unless otherwise specified, Ta = 25°C, VIN = 3.3 V)

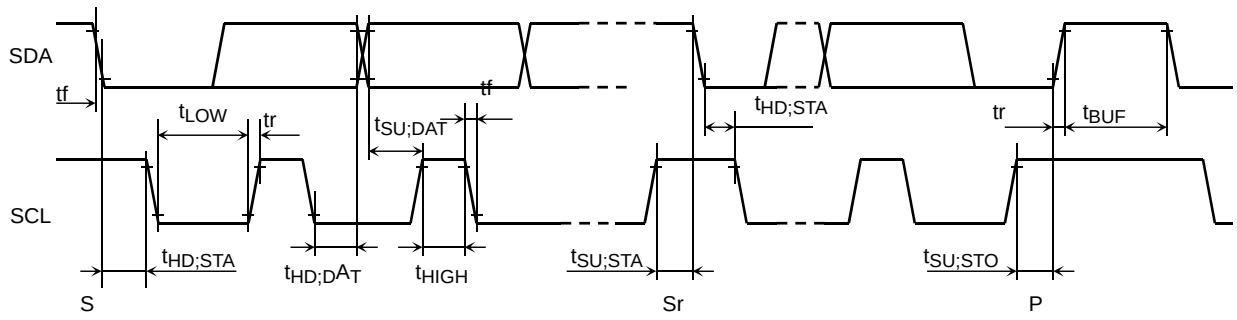


Figure 11-1 I^2C bus

I^2C Fast mode

Item	Symbol	Measurement condition	Min	Typ.	Max	Unit
SDA and SCL input voltage	VIH1	—	1.2	—	—	V
	VIL1	—	—	—	0.4	
SDA output voltage	VOL1	Sink current = 4 mA	—	—	0.4	V
Operation clock frequency	f_{SCL}	—	—	—	400	kHz
Hold time of repetitive start condition	$t_{HD:STA}$	—	0.6	—	—	μs
Setup time of repetitive start condition	$t_{SU:STA}$	—	0.6	—	—	μs
Data hold time	$t_{HD;DAT}$	—	0	—	0.9	μs
Data setup time	$t_{SU;DAT}$	—	100	—	—	ns
Low period of SCL signal	t_{LOW}	—	1.3	—	—	μs
High period of SCL signal	t_{HIGH}	—	0.6	—	—	μs

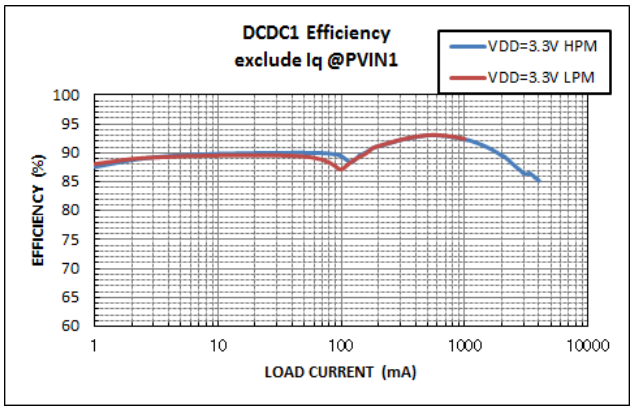
I^2C High speed mode

Item	Symbol	Measurement condition	Min	Typ.	Max	Unit
SDA and SCL input voltage	VIH1	—	1.2	—	—	V
	VIL1	—	—	—	0.4	
SDA output voltage	VOL1	Sink current = 4 mA	—	—	0.4	V
Operation clock frequency	f_{SCL}	—	—	—	3.4	MHz
Hold time of repetitive start condition	$t_{HD:STA}$	—	60	—	—	ns
Setup time of repetitive start condition	$t_{SU:STA}$	—	60	—	—	ns
Data hold time	$t_{HD;DAT}$	—	0	—	70	ns
Data setup time	$t_{SU;DAT}$	—	10	—	—	ns
Low period of SCL signal	t_{LOW}	—	160	—	—	ns
High period of SCL signal	t_{HIGH}	—	60	—	—	ns

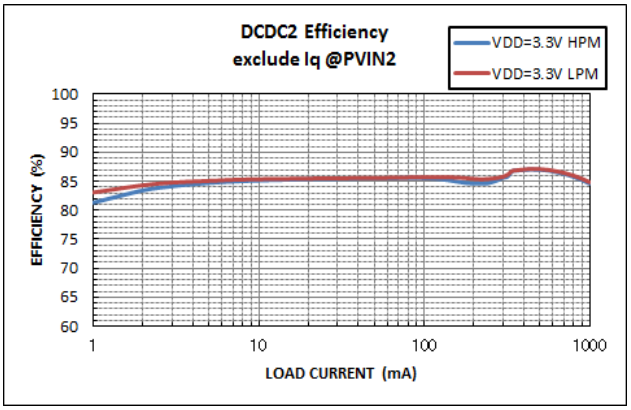
12. Typical characteristics (reference value)

12.1. DC-DC efficiency characteristics (Ta = 25°C, VIN = 3.3 V)

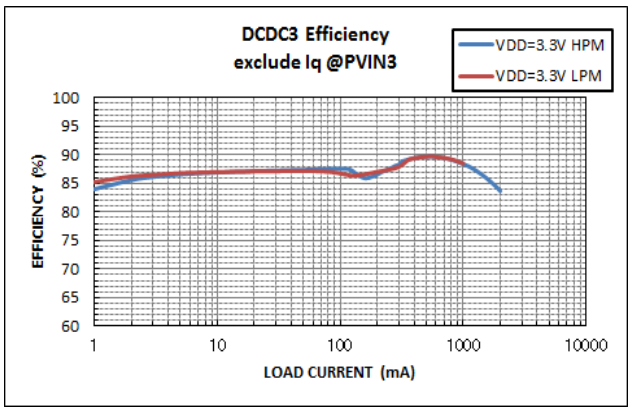
DC-DC1



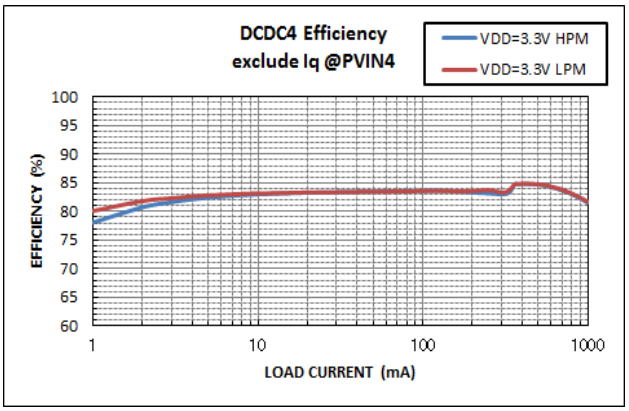
DC-DC2



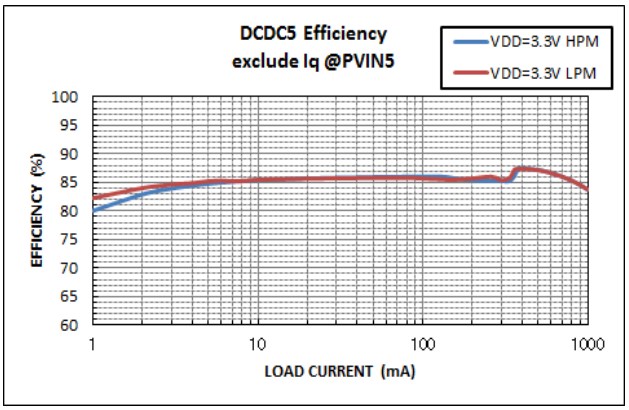
DC-DC3



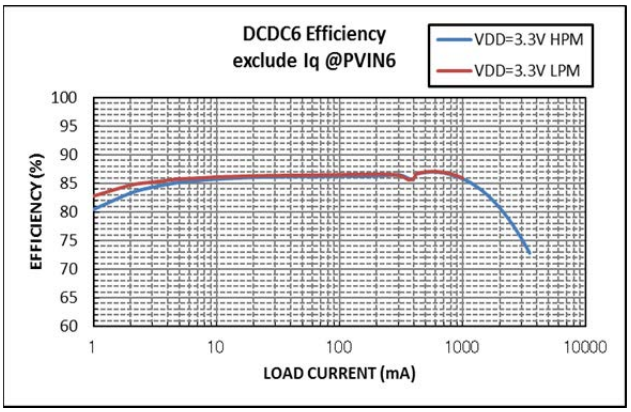
DC-DC4



DC-DC5

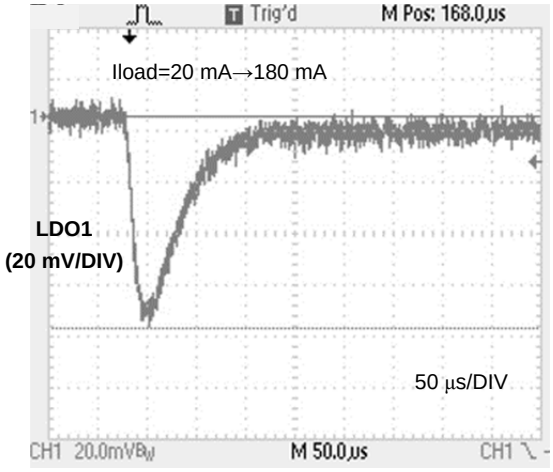


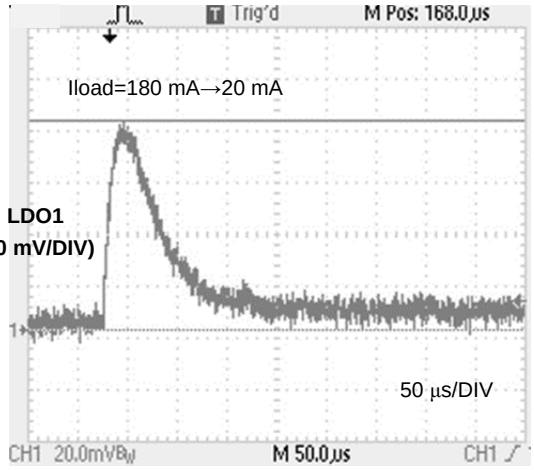
DC-DC6



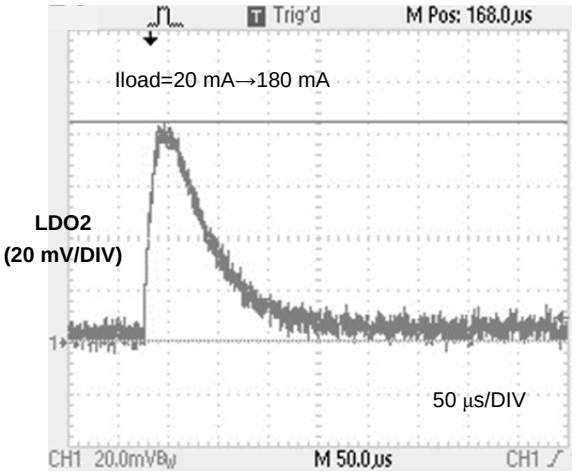
12.2. LDO load response regulation (Ta = 25°C)

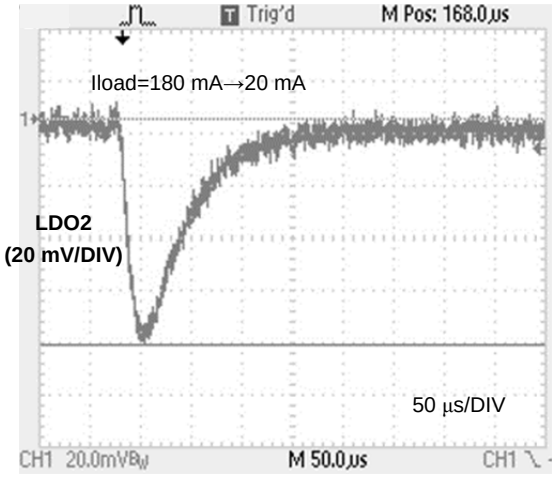
LDO1 (VIN=3.3 V, MODE_SEL=L, VSEL0=L)





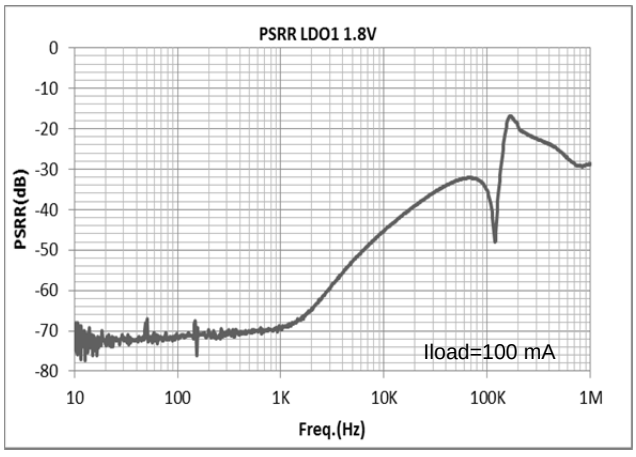
LDO2 (VIN=5V, MODE_SEL=Open, VSEL0=L)



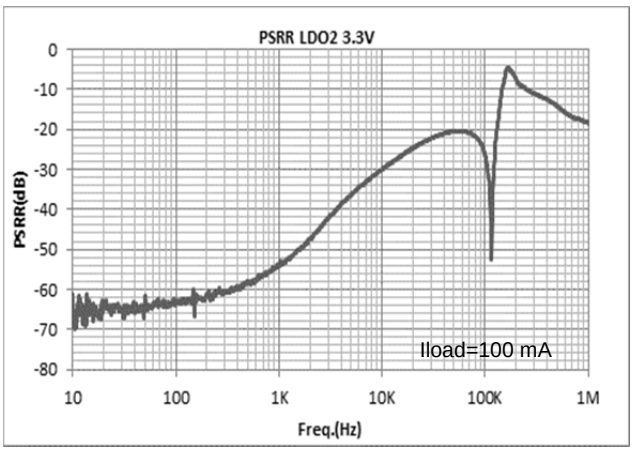


12.3. LDO PSRR (Ta = 25°C)

LDO1 (VIN=3.3 V, MODE_SEL=L, VSEL0=L)



LDO2 (VIN=5 V, MODE_SEL=Open, VSEL0=L)



13. Example of application circuit

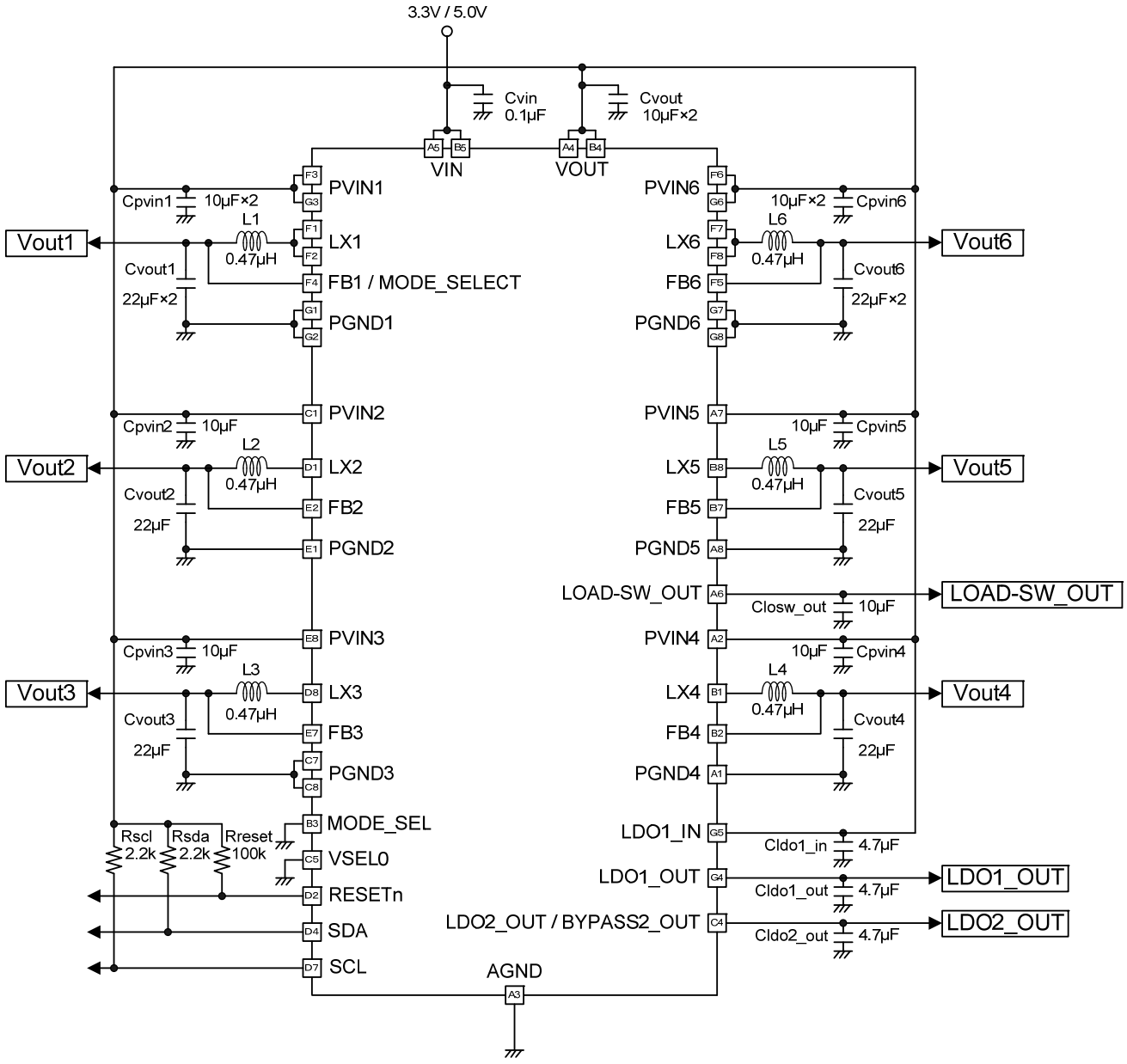


Figure 13-1 Example of application circuit

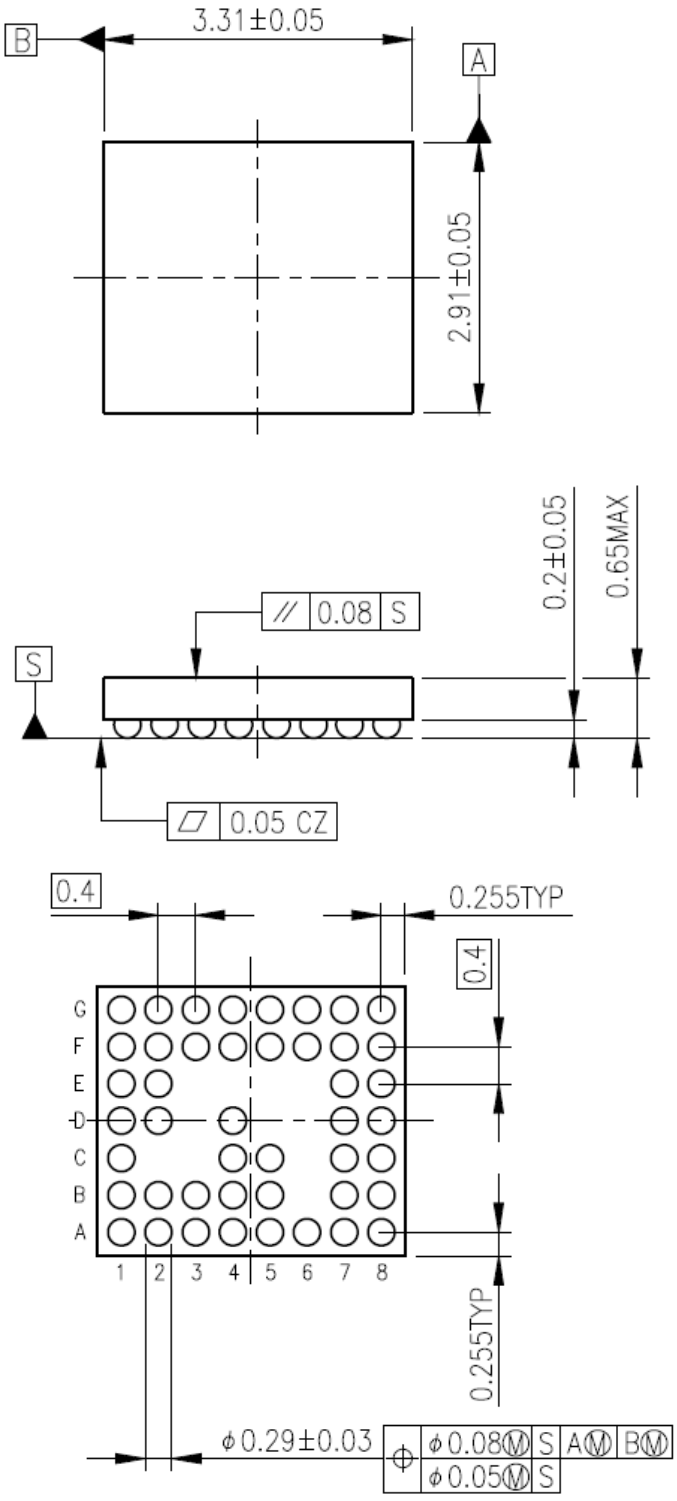
14. Recommended external components

Table 14.1 Example of external components

Parts No.	Purpose for use	Value	Size	Name of components	Manufacturer
L1	Inductor for DC-DC1	0.47 μH	2.5 × 2.0	TFM252010ALM_R47MTAA	TDK
L2	Inductor for DC-DC2	0.47 μH	2.0 × 1.6	MLP2016WR47M	TDK
L3	Inductor for DC-DC3	0.47 μH	2.5 × 2.0	MLP2520WR47M	TDK
L4	Inductor for DC-DC4	0.47 μH	2.0 × 1.6	MLP2016WR47M	TDK
L5	Inductor for DC-DC5	0.47 μH	2.0 × 1.6	MLP2016WR47M	TDK
L6	Inductor for DC-DC6	0.47 μH	2.5 × 2.0	TFM252010ALM_R47MTAA	TDK
Cvin	VIN input capacitor	0.1 μF (min)	—	—	—
Cpvin1	PVIN1 input capacitor	20 μF	1005	GRM155C80J106ME11D×2	Murata
Cpvin2	PVIN2 input capacitor	10 μF	1005	GRM155C80J106ME11D	Murata
Cpvin3	PVIN3 input capacitor	10 μF	1005	GRM155C80J106ME11D	Murata
Cpvin4	PVIN4 input capacitor	10 μF	1005	GRM155C80J106ME11D	Murata
Cpvin5	PVIN5 input capacitor	10 μF	1005	GRM155C80J106ME11D	Murata
Cpvin6	PVIN6 input capacitor	20 μF	1005	GRM155C80J106ME11D×2	Murata
Cldo1_in	LDO1 input capacitor	4.7 μF	1005	GRM155C80J475MEAAD	Murata
Cvout	VOUT output capacitor	22 μF	1608	GRM188C80J226ME15D	Murata
Cvout1	DC-DC1 output capacitor	44 μF	1608	GRM188C80J226ME15D×2	Murata
Cvout2	DC-DC2 output capacitor	22 μF	1608	GRM188C80J226ME15D	Murata
Cvout3	DC-DC3 output capacitor	22 μF	1608	GRM188C80J226ME15D	Murata
Cvout4	DC-DC4 output capacitor	22 μF	1608	GRM188C80J226ME15D	Murata
Cvout5	DC-DC5 output capacitor	22 μF	1608	GRM188C80J226ME15D	Murata
Cvout6	DC-DC6 output capacitor	44 μF	1608	GRM188C80J226ME15D×2	Murata
Cldo1_out	LDO1 output capacitor	4.7 μF	1005	GRM155C80J475MEAAD	Murata
Cldo2_out	LDO2 output capacitor	4.7 μF	1005	GRM155C80J475MEAAD	Murata
Closw_out	LOAD-SW output capacitor	10 μF	1005	GRM155C80J106ME11D	Murata
Rreset	RESETn pull up resistance	100 kΩ	—	—	—
RsdaA	SDA pull up resistance	2.2 kΩ	—	—	—
Rscl	SCL pull up resistance	2.2 kΩ	—	—	—

15. Package

S-UFBGA45-0403-0.40-001 Unit: mm



Note: This diagram aims at only explanation.
Please contact us about the size which is not indicated in this diagram.

Figure 15-1 Package dimensions

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