

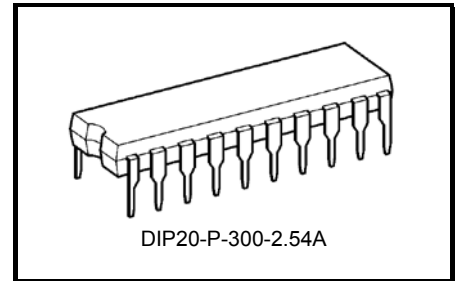
TBD62089APG

8-ch Sink Type DMOS Transistor Array with D-type Flip-Flop

The TBD62089APG is an 8-ch DMOS transistor array with D-type flip-flop. Please be careful about thermal conditions during use.

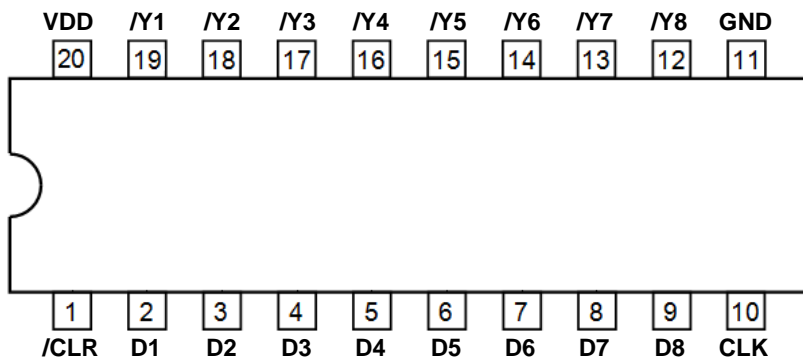
Features

- Built-in 8 circuits
- High output voltage : $V_{OUT} = 50\text{ V (max)}$
- High output current : $I_{OUT} = 500\text{ mA/ch (max)}$
- Package : DIP20-P-300-2.54A



Weight: 1.4 g (typ.)

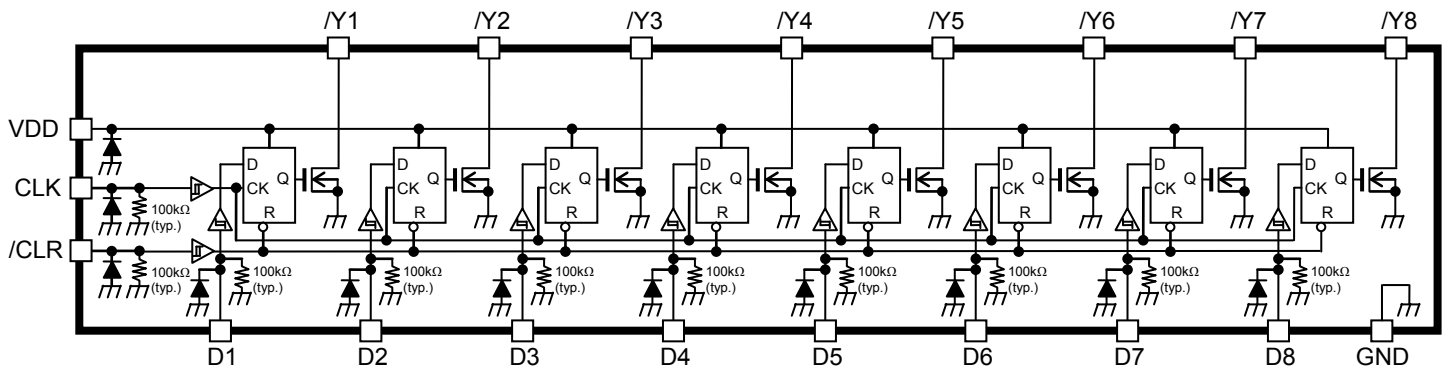
Pin assignment (top view)



Pin description

Pin No.	Pin name	Function
1	/CLR	Clear signal input pin
2	D1	Data signal input pin
3	D2	Data signal input pin
4	D3	Data signal input pin
5	D4	Data signal input pin
6	D5	Data signal input pin
7	D6	Data signal input pin
8	D7	Data signal input pin
9	D8	Data signal input pin
10	CLK	Clock signal input pin
11	GND	Ground pin
12	/Y8	Output pin
13	/Y7	Output pin
14	/Y6	Output pin
15	/Y5	Output pin
16	/Y4	Output pin
17	/Y3	Output pin
18	/Y2	Output pin
19	/Y1	Output pin
20	VDD	Power supply pin

Block diagram



Equivalent circuit may be omitted or simplified for explanatory purpose.

Function table

INPUT			OUTPUT: /Y
/CLR	CLK	D	
L	X	X	H
H	↑	L	H
H	↑	H	L
H	L	X	Y0
H	↓	X	Y0

↑: "L" to "H"

↓: "H" to "L"

H: High level

L: Low level

X: Don't care

Y0: /Y level just before inputting conditions in the table are fixed

*: Operating conditions in the table: OUTPUT is connected to the power supply through resistors.

Absolute maximum ratings (T_a = 25°C)

Characteristics	Symbol	Rating	Unit
Output voltage	V _{OUT}	50	V
Power supply voltage	V _{DD}	-0.5 to 6	V
Output current	I _{OUT}	500	mA/ch
Input voltage	V _{IN}	-0.5 to 6	V
Power dissipation	P _D (Note1)	1.76 (Note2)	W
Operating temperature	T _{opr}	-40 to 85	°C
Storage temperature	T _{stg}	-55 to 150	°C

Note1: In mounting on a board, based on JEDEC 2s2p standards

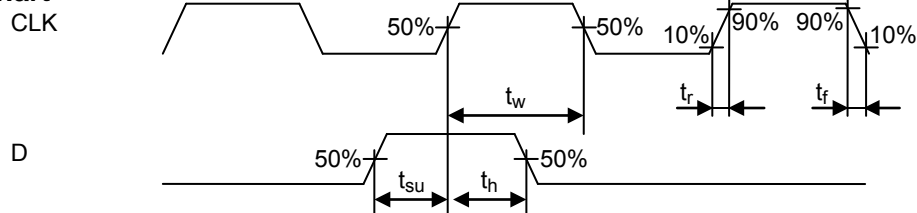
Note2: When T_a exceeds 25 °C, derating with 14.1 mW/°C is necessary.

Operating range (T_a = - 40 to 85°C, unless otherwise specified)

Characteristics	Symbol	Test conditions	Min	Typ.	Max	Unit	
Output voltage	V _{OUT}	—	—	—	50	V	
Power supply voltage	V _{DD}	—	3	—	5.5	V	
Output current (per channel) (Note)	I _{OUT}	1 channel ON, T _a = 25 °C	0	—	400	mA	
		t _{pw} = 25 ms 8 channels ON T _a = 85°C T _j = 120°C	Duty = 10 %	0	—		400
			Duty = 50 %	0	—		195
Input voltage (Output on)	V _{IN (ON)}	—	0.7×V _{DD}	—	V _{DD}	V	
Input voltage (Output off)	V _{IN (OFF)}	—	0	—	0.3×V _{DD}	V	
Voltage rising time of CLK input	t _r	V _{DD} = 3 V to 5.5 V	0	—	500	ns	
Voltage falling time of CLK input	t _f	V _{DD} = 3 V to 5.5 V	0	—	500	ns	
Setup time	t _{su}	V _{DD} = 3 V to 5.5 V Setup time of D input for CLK input	10	—	—	ns	
Hold time	t _h	V _{DD} = 3 V to 5.5 V Hold time of D input for CLK input	10	—	—	ns	
Pulse width (CLK, /CLR)	t _w	V _{DD} = 3 V to 5.5 V	30	—	—	ns	
Logic clock frequency	f _{CLK}	V _{DD} = 3 V to 5.5 V	—	—	20	MHz	

Note: In mounting on a board, based on JEDEC 2s2p standards

Timing chart

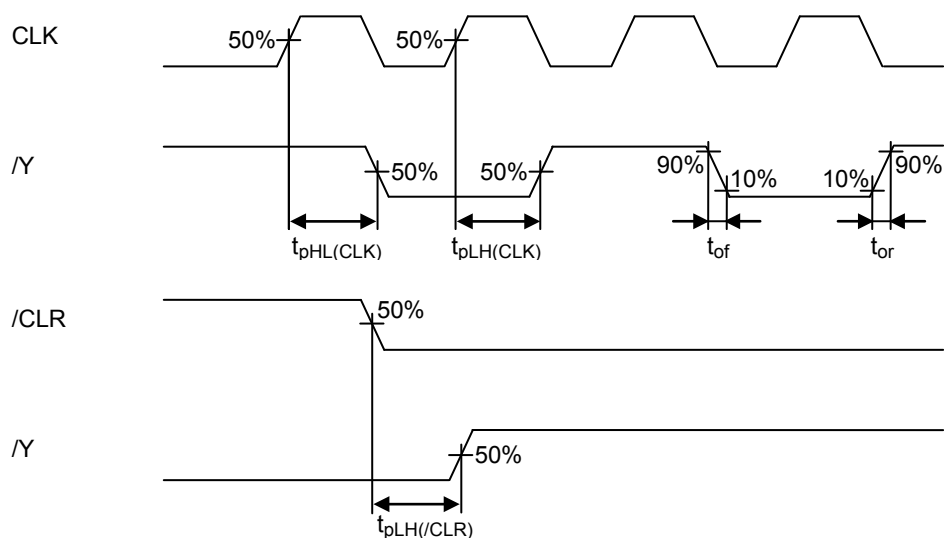


Timing charts may be omitted or simplified for explanatory purposes.

Electrical characteristics ($T_a = 25^\circ\text{C}$ and $V_{DD} = 5\text{ V}$, unless otherwise specified)

Characteristics	Symbol	Test Circuit	Test conditions	Min	Typ.	Max	Unit	
Output leakage current	I_{leak}	1	$V_{OUT} = 50\text{ V}$, $T_a = 85^\circ\text{C}$ $V_{IN} = 0\text{ V}$	—	—	1.0	μA	
Output voltage (Output ON-resistance)	V_{DS} (R_{ON})	2	$I_{OUT} = 350\text{ mA}$	—	0.56 (1.6)	1.14 (3.25)	V (Ω)	
			$I_{OUT} = 200\text{ mA}$	—	0.32 (1.6)	0.65 (3.25)		
			$I_{OUT} = 100\text{ mA}$	—	0.16 (1.6)	0.325 (3.25)		
Input current (Output on)	$I_{IN(ON)}$	3	$V_{IN} = 5.5\text{ V}$, $V_{DD} = 5.5\text{ V}$	—	—	80	μA	
Input current (Output off)	$I_{IN(OFF)}$	4	$V_{IN} = 0\text{ V}$, $V_{DD} = 5.5\text{ V}$	—	—	1.0	μA	
Power supply current (per channel)	$I_{CC(ON)}$	3	$V_{IN} = 5.5\text{ V}$, $V_{DD} = 5.5\text{ V}$	—	—	75	μA	
	$I_{CC(OFF)}$	4	$V_{IN} = 0\text{ V}$, $V_{DD} = 5.5\text{ V}$	—	—	1.0	μA	
Propagation delay time	$t_{pHL(CLK)}$	5	CLK (50 %) to /Y (50 %) /Y: H to L $C_L = 30\text{ pF}$ $R_L = 240\ \Omega$, pull-up to 24 V	$V_{DD} = 4.5\text{ to }5.5\text{ V}$	—	270	430	ns
				$V_{DD} = 3.0\text{ to }3.6\text{ V}$	—	470	670	
	$t_{pLH(CLK)}$	5	CLK (50 %) to /Y (50 %) /Y: L to H $C_L = 30\text{ pF}$ $R_L = 240\ \Omega$, pull-up to 24 V	$V_{DD} = 4.5\text{ to }5.5\text{ V}$	—	350	510	ns
				$V_{DD} = 3.0\text{ to }3.6\text{ V}$	—	350	510	
	$t_{pLH(/CLR)}$	5	/CLR (50 %) to /Y (50 %) /Y: L to H $C_L = 30\text{ pF}$ $R_L = 240\ \Omega$, pull-up to 24 V	$V_{DD} = 4.5\text{ to }5.5\text{ V}$	—	350	510	ns
				$V_{DD} = 3.0\text{ to }3.6\text{ V}$	—	350	510	
Turn-on delay time	t_{or}	5	/Y waveform: 10 % to 90 % $C_L = 30\text{ pF}$ $R_L = 240\ \Omega$, pull-up to 24 V	$V_{DD} = 4.5\text{ to }5.5\text{ V}$	—	280	400	ns
				$V_{DD} = 3.0\text{ to }3.6\text{ V}$	—	280	400	
Turn-off delay time	t_{of}	5	/Y waveform: 90 % to 10 % $C_L = 30\text{ pF}$ $R_L = 240\ \Omega$, pull-up to 24 V	$V_{DD} = 4.5\text{ to }5.5\text{ V}$	—	330	480	ns
				$V_{DD} = 3.0\text{ to }3.6\text{ V}$	—	620	860	

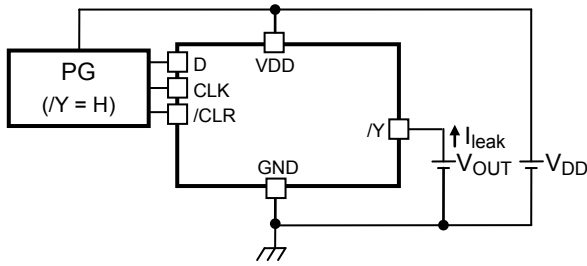
Timing chart



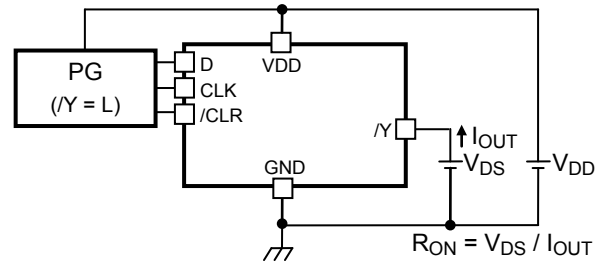
Timing charts may be omitted or simplified for explanatory purposes.

Test circuit

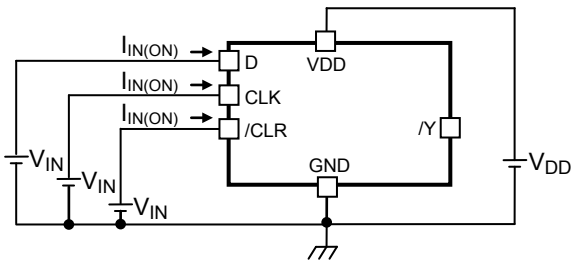
1. I_{leak}



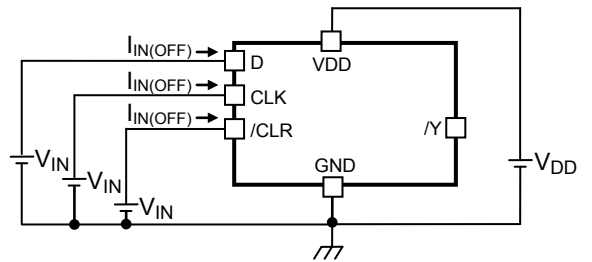
2. $V_{DS} (R_{ON})$



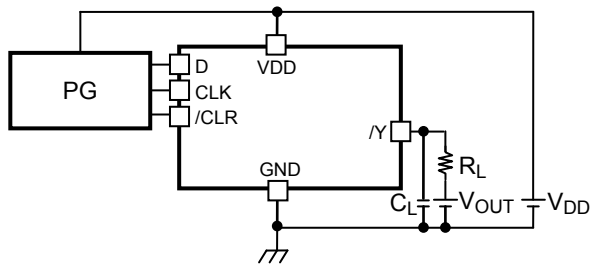
3. $I_{IN(ON)}$ and $I_{CC(ON)}$



4. $I_{IN(OFF)}$ and $I_{CC(OFF)}$



5. $t_{pHL}(CLK)$, $t_{pLH}(CLK)$, $t_{pLH}(/CLR)$, t_{or} , and t_{of}

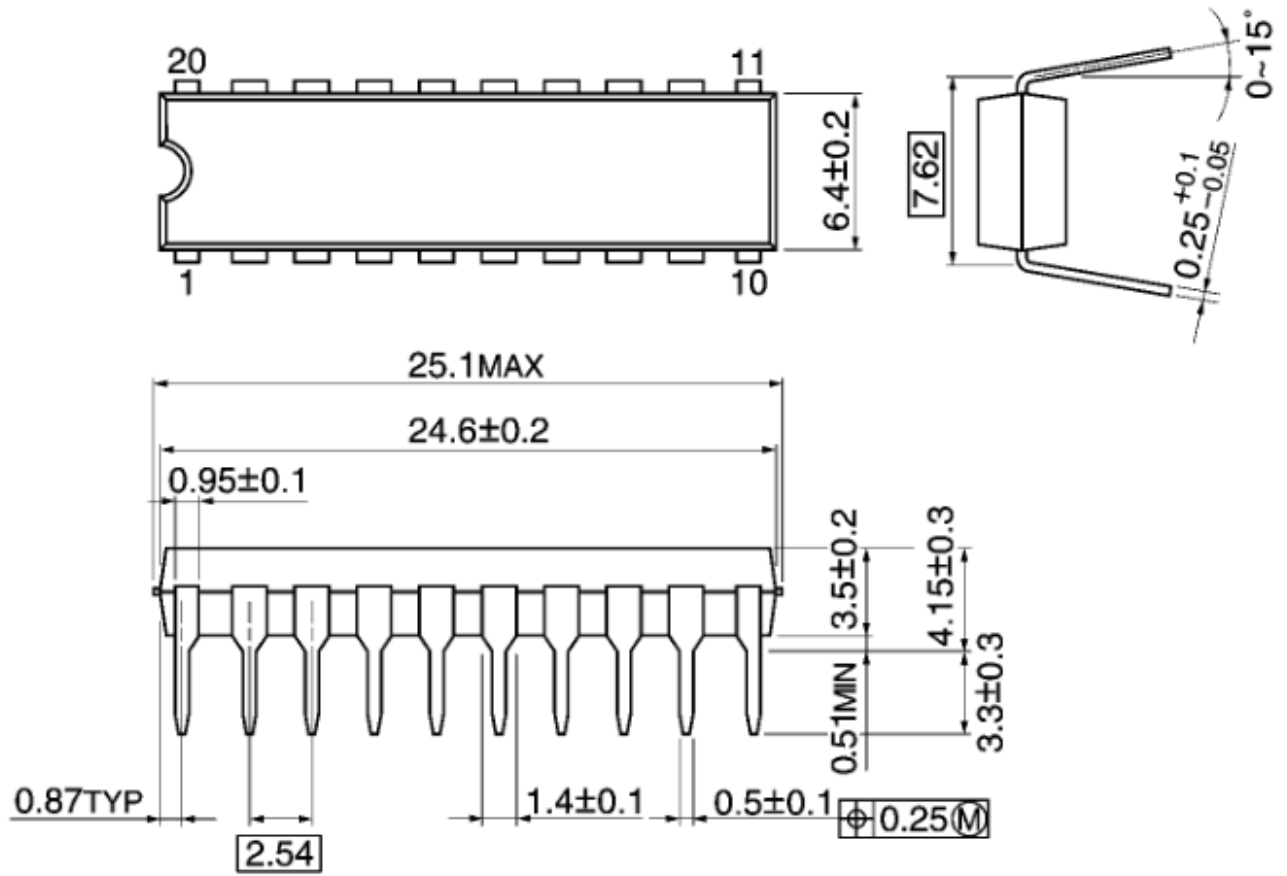


Test circuits may be omitted or simplified for explanatory purposes.

Package dimensions

DIP20-P-300-2.54A

Unit: mm



Weight: 1.4 g (typ.)

Notes on Contents

1. Block diagram

Block diagram may be simplified for explanatory purpose.

2. Test circuit

Test circuit may be simplified for explanatory purpose.

3. Timing chart

Timing charts may be simplified for explanatory purposes.

IC Usage Considerations

Notes on handling of ICs

- (1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings. Exceeding the rating(s) may cause device breakdown, damage or deterioration, and may result in injury by explosion or combustion.
- (2) Do not insert devices in the wrong orientation or incorrectly. Make sure that the positive and negative terminals of power supplies are connected properly. Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause device breakdown, damage or deterioration, and may result in injury by explosion or combustion. In addition, do not use any device inserted in the wrong orientation or incorrectly to which current is applied even just once.
- (3) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in the case of overcurrent and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead to smoke or ignition. To minimize the effects of the flow of a large current in the case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.
- (4) If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition. Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.
- (5) Carefully select external components (such as inputs and negative feedback capacitors) and load components (such as speakers), for example, power amp and regulator. If there is a large amount of leakage current such as from input or negative feedback condenser, the IC output DC voltage will increase. If this output voltage is connected to a speaker with low input withstand voltage, overcurrent or IC failure may cause smoke or ignition. (The overcurrent may cause smoke or ignition from the IC itself.) In particular, please pay attention when using a Bridge Tied Load (BTL) connection-type IC that inputs output DC voltage to a speaker directly.

Points to remember on handling of ICs

Heat Radiation Design

When using an IC with large current flow such as power amp, regulator or driver, design the device so that heat is appropriately radiated, in order not to exceed the specified junction temperature (T_J) at any time or under any condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, when designing the device, take into consideration the effect of IC heat radiation with peripheral components.

Back-EMF

When a motor rotates in the reverse direction, stops or slows abruptly, current flows back to the motor's power supply owing to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond the absolute maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

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