ESD Protection Diodes Silicon Epitaxial Planar

DF6D6M4N

1. General

The DF6D6M4N is a TVS diode (ESD protection diode) protects semiconductor devices used in mobile device interfaces and other applications to protect against static electricity and noise.

Utilizing snapback characteristics, the DF6D6M4N provides low dynamic resistance and superior protective performance. Furthermore, the DF6D6M4N is a multibit device with a flow-through type design that is easy for board layout and mounting.

2. Applications

Mobile Equipment

- Smartphones
- Tablets
- Notebook PCs

Desktop PCs

Note: This product is designed for protection against electrostatic discharge (ESD) and is not intended for any other purpose, including, but not limited to, voltage regulation.

3. Features

(1) Suitable for use with a 5 V signal line. ($V_{RWM} \leq 5.5$ V)

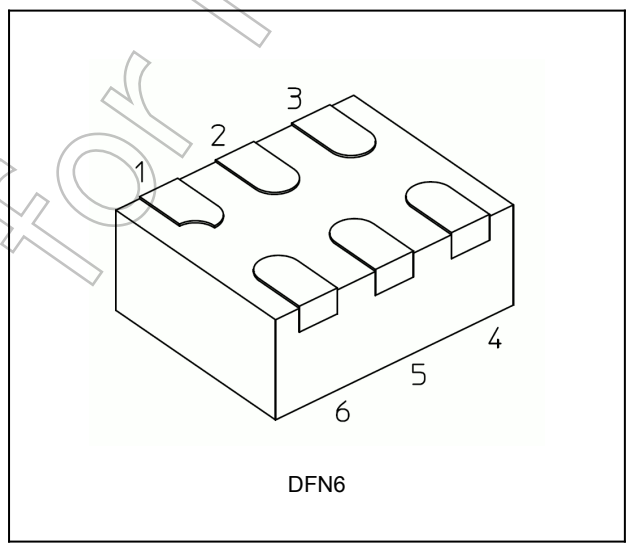
(2) Protects devices with its high ESD performance.
(V_{ESD} = ±20 kV (Contact / Air) @IEC61000-4-2)

(3) Low dynamic resistance protects semiconductor devices from static electricity and noise.
(R_{DYN} = 0.8 Ω (typ.))

(4) Snapback characteristics realizing low clamping voltage protects semiconductor devices.
(V_C = 10 V@I_{PP} = 2 A (typ.))

(5) The DF6D6M4N is a multibit device with a flow-through type.
(1.25 mm × 1.0 mm size (Nickname: DFN6))

4. Packaging

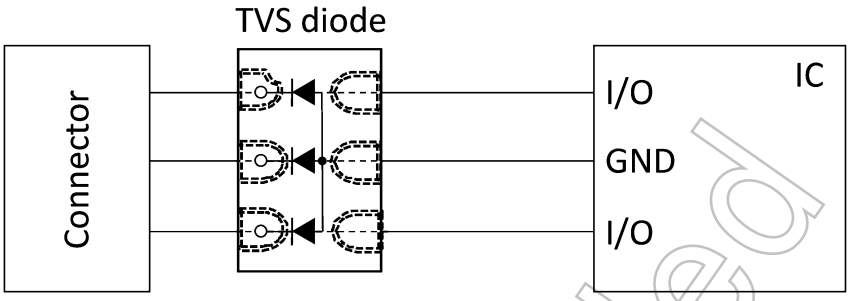


DFN6

Start of commercial production
2022-03

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5. Example of Circuit Diagram



6. Quick Reference Data

Characteristics	Symbol	Note	Test Condition	Min	Typ.	Max	Unit
Working peak reverse voltage	V_{RWM}	(Note 1)	—	—	—	5.5	V
Total capacitance	C_t		V_R = 0 V, f = 1 MHz	—	0.2	0.3	pF
Dynamic resistance	R_{DYN}	(Note 2)	—	—	0.8	—	Ω
Electrostatic discharge voltage (IEC61000-4-2) (Contact)	V_{ESD}	(Note 3)	—	—	—	20	kV

Note 1: Recommended operating condition.

Note 2: TLP parameters: Z0 = 50 Ω, tp = 100 ns, tr = 300 ps, averaging window: t1 = 30 ns to t2 = 60 ns, extraction of dynamic resistance using least squares fit of TLP characteristics between I_{PP1} = 8 A and I_{PP2} = 16 A.

Note 3: Criterion: No damage to devices.

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6.1. ESD Clamp Waveform (Note)

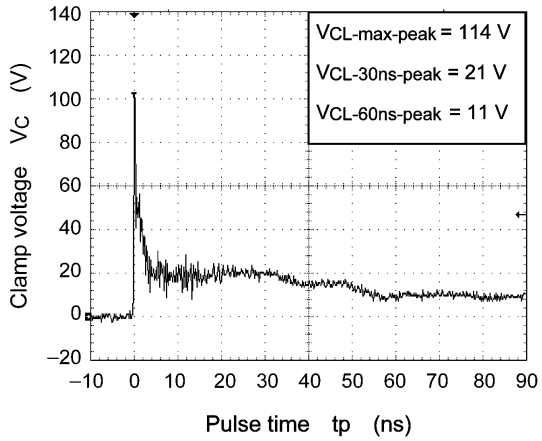


Fig. 6.1.1 +8 kV

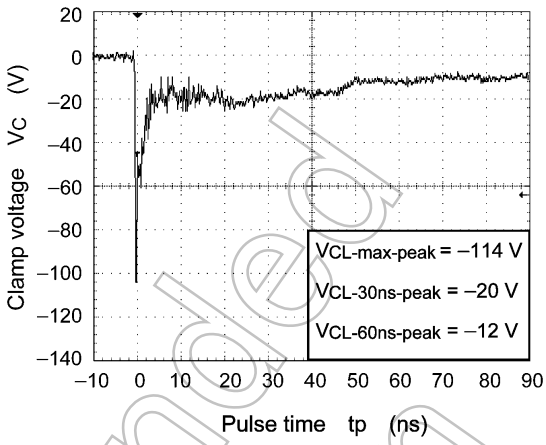


Fig. 6.1.2 -8 kV

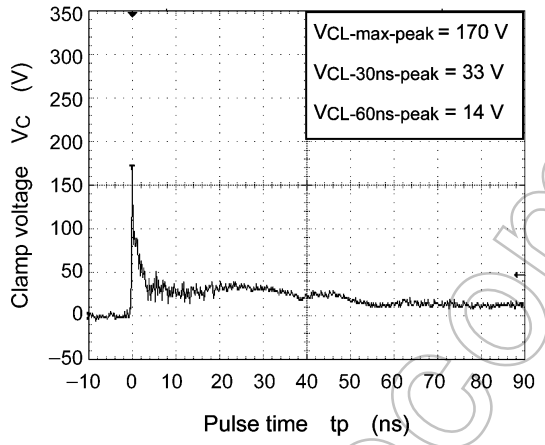


Fig. 6.1.3 +15 kV

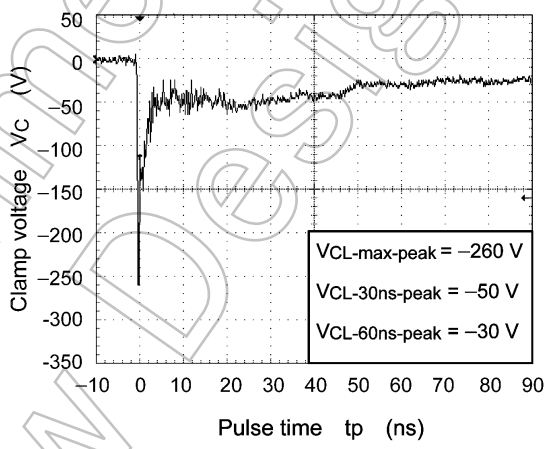


Fig. 6.1.4 -15 kV

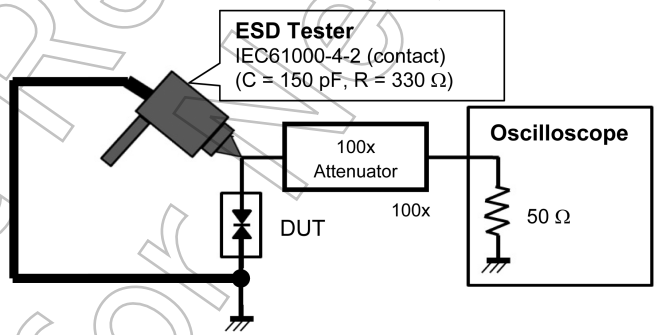
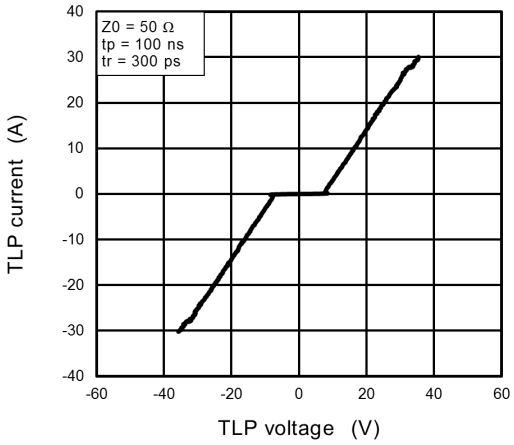


Fig. 6.1.5 IEC61000-4-2 (Contact)

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Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

6.2. TLP Characteristics (Note)



Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

6.3. Clamp Voltage - Peak Pulse Current (V_C - I_{PP}) (Note)

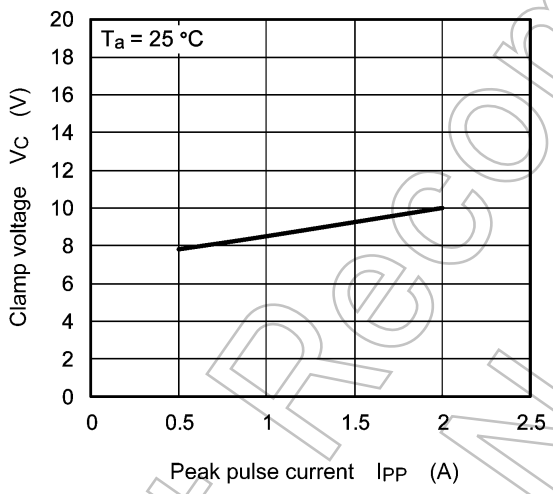


Fig. 6.3.1 V_C - I_{PP}

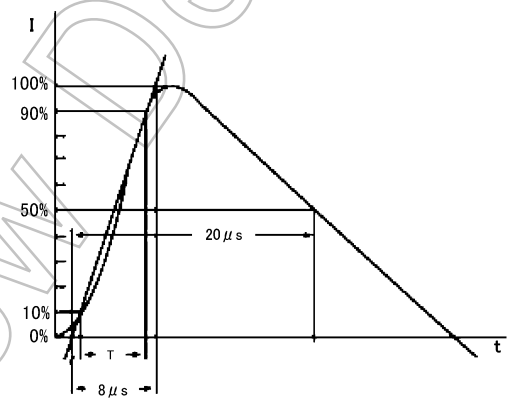


Fig. 6.3.2 Based on IEC61000-4-5 8/20 μs pulse.

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

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7. Absolute Maximum Ratings (Note) (Unless otherwise specified, T_a = 25 °C)

Characteristics	Symbol	Note	Rating	Unit
Electrostatic discharge voltage (IEC61000-4-2) (Contact)	V_{ESD}	(Note 1)	±20	kV
Electrostatic discharge voltage (IEC61000-4-2) (Air)			±20	
Peak pulse power (tp = 8/20 μs)	P_{PK}		30	W
Peak pulse current (tp = 8/20 μs)	I_{PP}	(Note 2)	2	A
Junction temperature	T_j		125	°C
Storage temperature	T_{stg}		-55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: According to IEC61000-4-2.

Note 2: According to IEC61000-4-5.

8. Electrical Characteristics (Unless otherwise specified, T_a = 25 °C)

V_{RWM}: Working peak reverse voltage
V_{BR}: Reverse breakdown voltage
I_{BR}: Reverse breakdown current
I_R: Reverse current
V_C: Clamp voltage
I_{PP}: Peak pulse current
R_{DYN}: Dynamic resistance

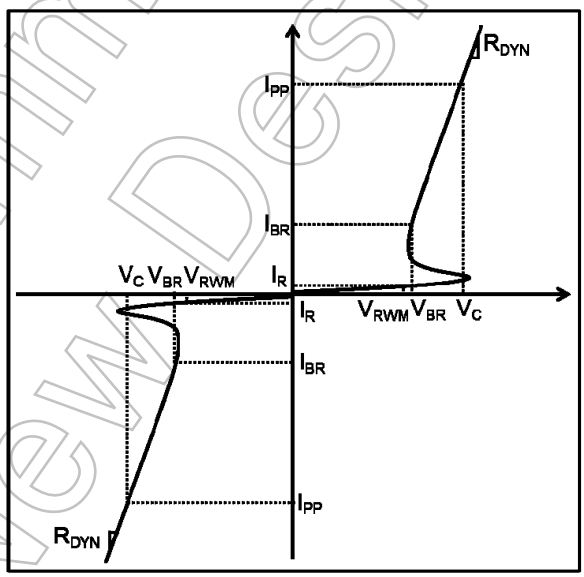


Fig. 8.1 Definitions of Electrical Characteristics

Characteristics	Symbol	Note	Test Condition	Min	Typ.	Max	Unit
Working peak reverse voltage	V_{RWM}	(Note 1)	—	—	—	5.5	V
Total capacitance	C_t		V_R = 0 V, f = 1 MHz	—	0.2	0.3	pF
Dynamic resistance	R_{DYN}	(Note 2)	—	—	0.8	—	Ω
Reverse breakdown voltage	V_{BR}		I_{BR} = 1 mA	5.6	6.2	8.0	V
Reverse current	I_R		V_{RWM} = 5.5 V	—	—	0.1	μA
Clamp voltage	V_C	(Note 3)	I_{PP} = 1 A	—	8.5	—	V
			I_{PP} = 2 A	—	10	15	
		(Note 2)	I_{TLP} = 16 A	—	22	—	V
			I_{TLP} = 30 A	—	34	—	

Note 1: Recommended operating condition.

Note 2: TLP parameters: Z0 = 50 Ω, tp = 100 ns, tr = 300 ps, averaging window: t1 = 30 ns to t2 = 60 ns, extraction of dynamic resistance using least squares fit of TLP characteristics between I_{PP1} = 8 A and I_{PP2} = 16 A.

Note 3: Based on IEC61000-4-5 8/20 μs pulse.

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9. Characteristics Curves (Note)

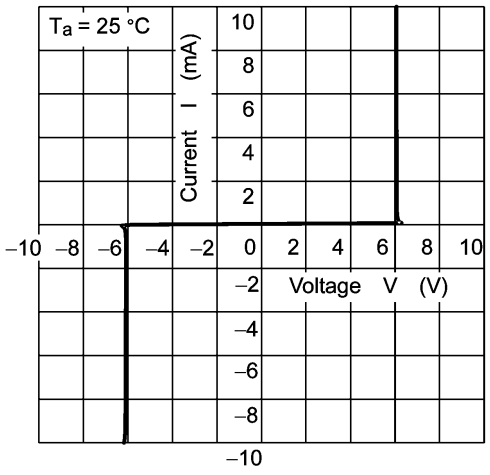


Fig. 9.1 I - V

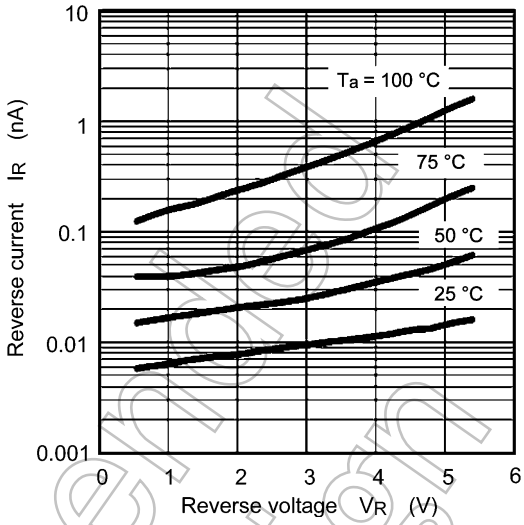


Fig. 9.2 I_R - V_R

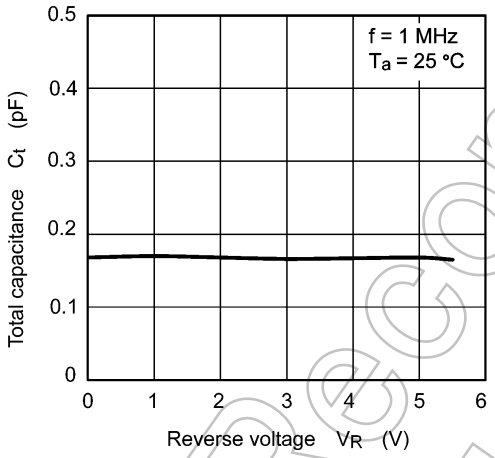


Fig. 9.3 C_t - V_R

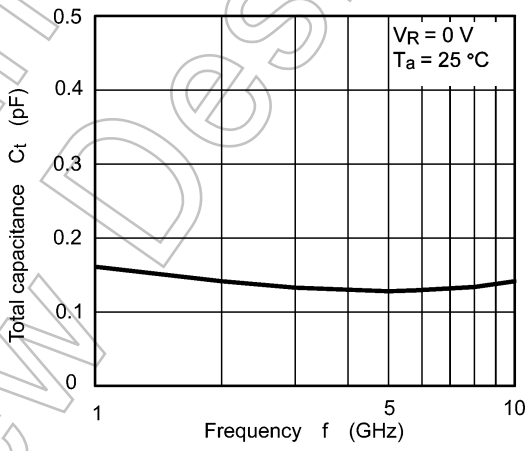


Fig. 9.4 C_t - f

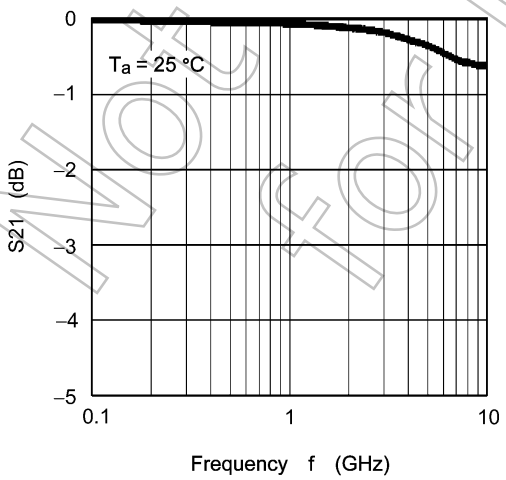
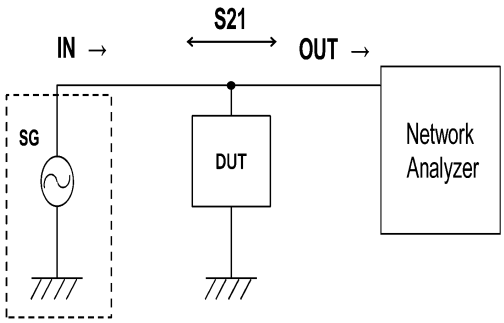


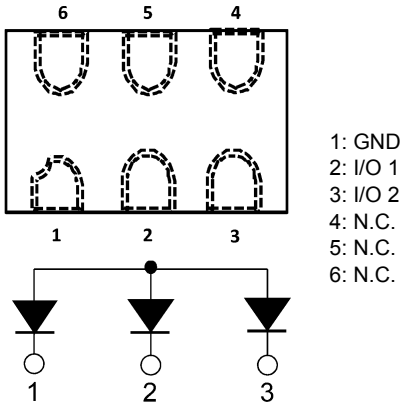
Fig. 9.5 S21 - f



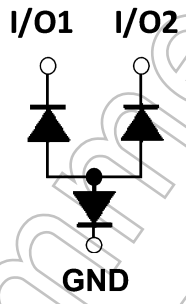
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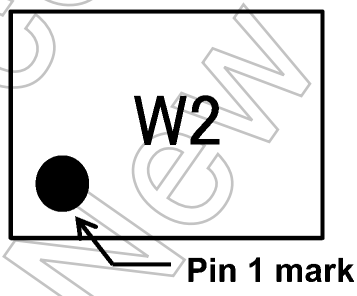
10. Internal Circuit



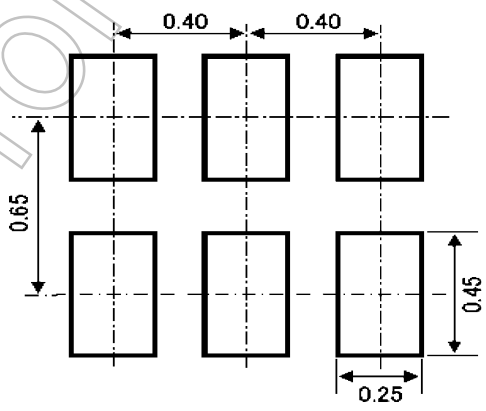
11. Equivalent Circuit (Top view)



12. Marking (Top view)



13. Land Pattern Dimensions (for reference only)

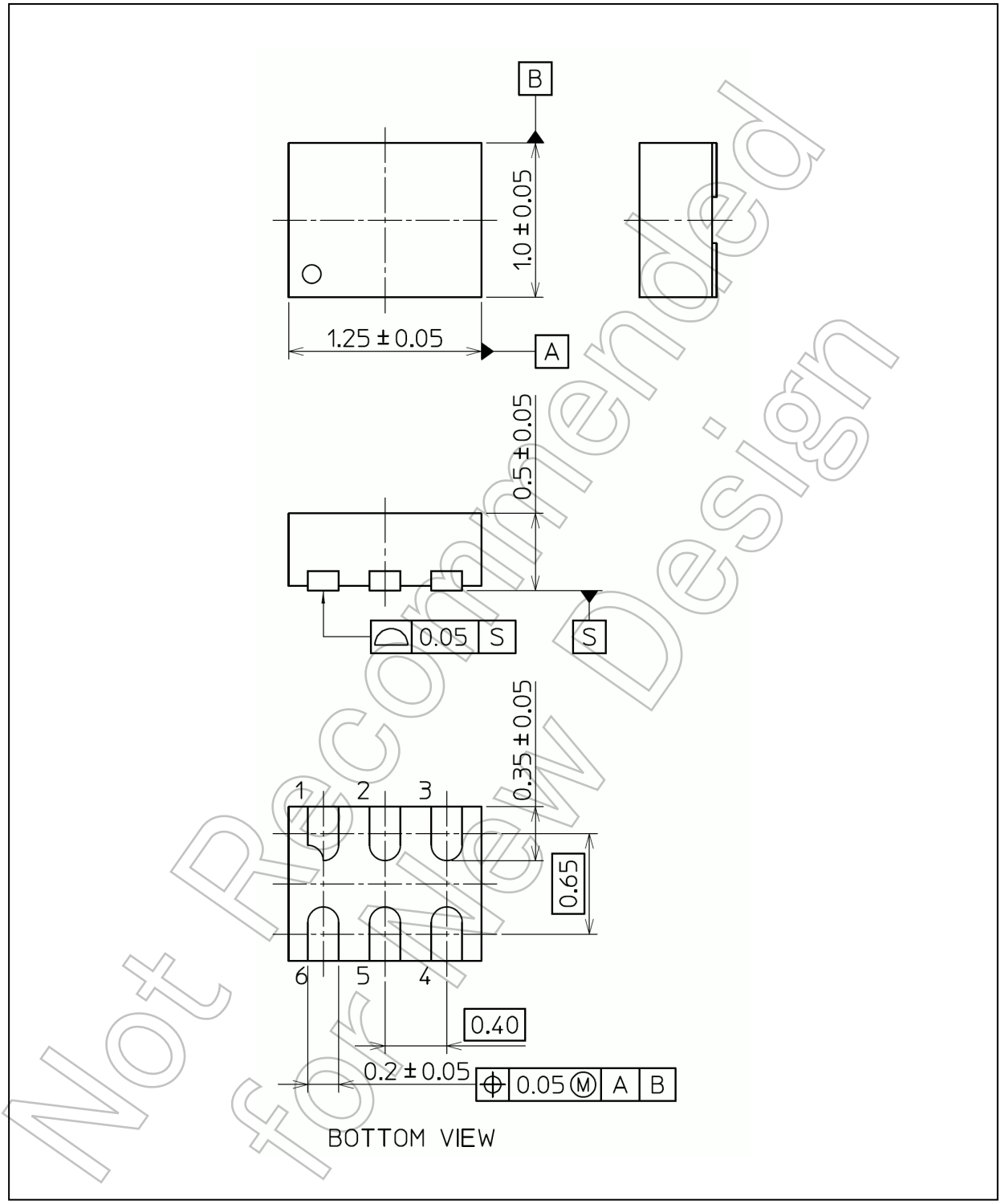


Unit: mm

Not Recommended for New Design

Package Dimensions

Unit: mm



Not Recommended for New Design

Weight: 0.0017 g (typ.)

Package Name(s)
Nickname: DFN6

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