

MOSFETs Silicon N-channel MOS (U-MOSIX-H)

## TK3R3A06PL

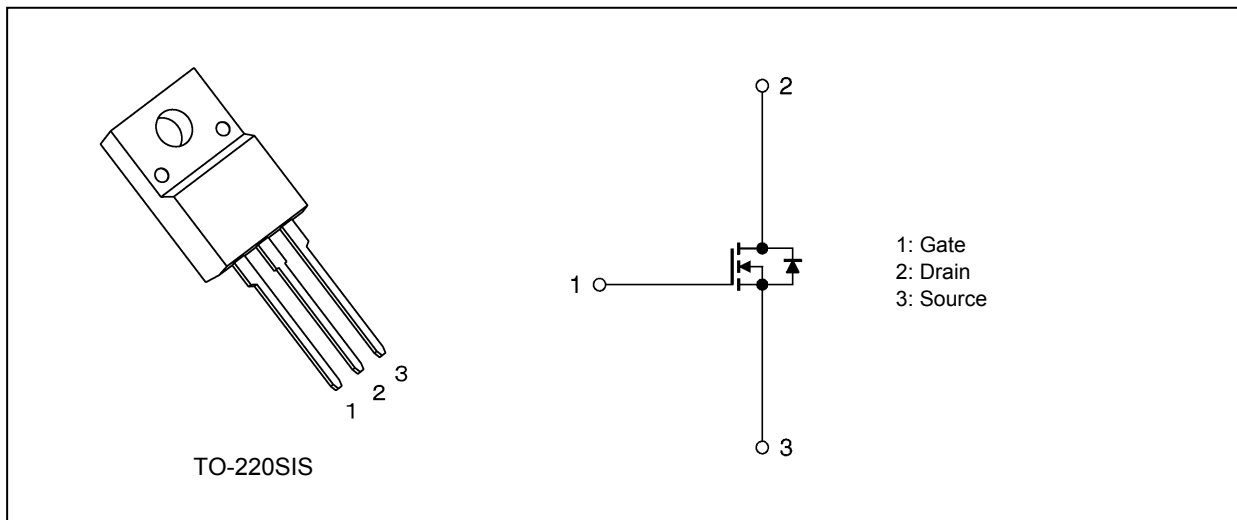
### 1. Applications

- High-Efficiency DC-DC Converters
- Switching Voltage Regulators
- Motor Drivers

### 2. Features

- (1) High-speed switching
- (2) Small gate charge:  $Q_{SW} = 21 \text{ nC (typ.)}$
- (3) Small output charge:  $Q_{OSS} = 66 \text{ nC (typ.)}$
- (4) Low drain-source on-resistance:  $R_{DS(ON)} = 2.5 \text{ m}\Omega \text{ (typ.) (} V_{GS} = 10 \text{ V)}$
- (5) Low leakage current:  $I_{DSS} = 10 \text{ }\mu\text{A (max) (} V_{DS} = 60 \text{ V)}$
- (6) Enhancement mode:  $V_{th} = 1.5 \text{ to } 2.5 \text{ V (} V_{DS} = 10 \text{ V, } I_D = 0.7 \text{ mA)}$

### 3. Packaging and Internal Circuit



Start of commercial production

2017-06

## 4. Absolute Maximum Ratings (Note) ( $T_a = 25\text{ }^\circ\text{C}$ unless otherwise specified)

| Characteristics  | Symbol         | Rating     | Unit             |
|--|----------------|------------|------------------|
| Drain-source voltage   | $V_{DSS}$      | 60         | V                |
| Gate-source voltage  | $V_{GSS}$      | $\pm 20$   |                  |
| Drain current (DC) ( $T_c = 25\text{ }^\circ\text{C}$ ) (Note 1) | $I_D$          | 80         | A                |
| Drain current (DC) (Silicon limit) (Note 1), (Note 2)            | $I_D$          | 88         | A                |
| Drain current (pulsed) ( $t = 100\text{ }\mu\text{s}$ ) (Note 1) | $I_{DP}$       | 400        | A                |
| Power dissipation ( $T_c = 25\text{ }^\circ\text{C}$ )           | $P_D$          | 42         | W                |
| Single-pulse avalanche energy (Note 3)                           | $E_{AS}$       | 76         | mJ               |
| Single-pulse avalanche current (Note 3)                          | $I_{AS}$       | 80         | A                |
| Channel temperature  | $T_{ch}$       | 175        | $^\circ\text{C}$ |
| Storage temperature  | $T_{stg}$      | -55 to 175 | $^\circ\text{C}$ |
| Isolation voltage (RMS) ( $t = 1.0\text{ s}$ )                   | $V_{ISO(RMS)}$ | 2000       | V                |
| Mounting torque  | TOR            | 0.6        | N · m            |

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

## 5. Thermal Characteristics

| Characteristics  | Symbol         | Max  | Unit                      |
|--|----------------|------|---------------------------|
| Channel-to-case thermal resistance ( $T_c = 25\text{ }^\circ\text{C}$ )    | $R_{th(ch-c)}$ | 3.57 | $^\circ\text{C}/\text{W}$ |
| Channel-to-ambient thermal resistance ( $T_a = 25\text{ }^\circ\text{C}$ ) | $R_{th(ch-a)}$ | 62.5 |                           |

Note 1: Ensure that the channel temperature does not exceed  $175\text{ }^\circ\text{C}$ .

Note 2: Limited by silicon chip capability.

Note 3:  $V_{DD} = 48\text{ V}$ ,  $T_{ch} = 25\text{ }^\circ\text{C}$  (initial),  $L = 9.2\text{ }\mu\text{H}$ ,  $I_{AS} = 80\text{ A}$

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.

### 6. Electrical Characteristics

#### 6.1. Static Characteristics ( $T_a = 25\text{ }^\circ\text{C}$ unless otherwise specified)

| Characteristics                         | Symbol        | Test Condition                                  | Min | Typ. | Max       | Unit             |
|---|---------------|---|-----|------|-----------|------------------|
| Gate leakage current                    | $I_{GSS}$     | $V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$ | —   | —    | $\pm 0.1$ | $\mu\text{A}$    |
| Drain cut-off current                   | $I_{DSS}$     | $V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}$     | —   | —    | 10        |                  |
| Drain-source breakdown voltage          | $V_{(BR)DSS}$ | $I_D = 10\text{ mA}, V_{GS} = 0\text{ V}$       | 60  | —    | —         | V                |
| Drain-source breakdown voltage (Note 4) | $V_{(BR)DSX}$ | $I_D = 10\text{ mA}, V_{GS} = -20\text{ V}$     | 45  | —    | —         |                  |
| Gate threshold voltage                  | $V_{th}$      | $V_{DS} = 10\text{ V}, I_D = 0.7\text{ mA}$     | 1.5 | —    | 2.5       |                  |
| Drain-source on-resistance              | $R_{DS(ON)}$  | $V_{GS} = 4.5\text{ V}, I_D = 34\text{ A}$      | —   | 3.3  | 4.9       | $\text{m}\Omega$ |
|   |               | $V_{GS} = 10\text{ V}, I_D = 40\text{ A}$       | —   | 2.5  | 3.3       |                  |

Note 4: If a reverse bias is applied between gate and source, this device enters  $V_{(BR)DSX}$  mode. Note that the drain-source breakdown voltage is lowered in this mode.

#### 6.2. Dynamic Characteristics ( $T_a = 25\text{ }^\circ\text{C}$ unless otherwise specified)

| Characteristics                | Symbol    | Test Condition  | Min | Typ. | Max | Unit        |
|--------------------------------|-----------|---|-----|------|-----|-------------|
| Input capacitance              | $C_{iss}$ | $V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$ | —   | 5000 | —   | $\text{pF}$ |
| Reverse transfer capacitance   | $C_{rss}$ |   | —   | 55   | —   |             |
| Output capacitance             | $C_{oss}$ |   | —   | 950  | —   |             |
| Gate resistance                | $r_g$     | —   | —   | 1.5  | —   | $\Omega$    |
| Switching time (rise time)     | $t_r$     | See Fig. 6.2.1  | —   | 7    | —   | ns          |
| Switching time (turn-on time)  | $t_{on}$  |   | —   | 25   | —   |             |
| Switching time (fall time)     | $t_f$     |   | —   | 16   | —   |             |
| Switching time (turn-off time) | $t_{off}$ |   | —   | 66   | —   |             |

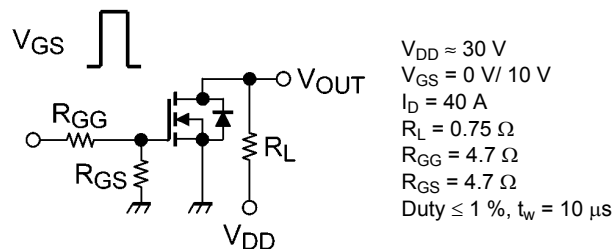


Fig. 6.2.1 Switching Time Test Circuit

#### 6.3. Gate Charge Characteristics ( $T_a = 25\text{ }^\circ\text{C}$ unless otherwise specified)

| Characteristics                                 | Symbol    | Test Condition   | Min | Typ. | Max | Unit |
|---|-----------|--|-----|------|-----|------|
| Total gate charge (gate-source plus gate-drain) | $Q_g$     | $V_{DD} \approx 30\text{ V}, V_{GS} = 10\text{ V}, I_D = 40\text{ A}$  | —   | 71   | —   | nC   |
|   |           | $V_{DD} \approx 30\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 40\text{ A}$ | —   | 35   | —   |      |
| Gate-source charge 1                            | $Q_{gs1}$ | $V_{DD} \approx 30\text{ V}, V_{GS} = 10\text{ V}, I_D = 40\text{ A}$  | —   | 19   | —   |      |
| Gate-drain charge                               | $Q_{gd}$  |  | —   | 13   | —   |      |
| Gate switch charge                              | $Q_{SW}$  |  | —   | 21   | —   |      |
| Output charge                                   | $Q_{oss}$ | $V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$          | —   | 66   | —   |      |

## 6.4. Source-Drain Characteristics ( $T_a = 25\text{ }^\circ\text{C}$ unless otherwise specified)

| Characteristics                         | Symbol  | Test Condition   | Min | Typ. | Max  | Unit |
|---|---|--|-----|------|------|------|
| Reverse drain current (pulsed) (Note 5) | $I_{DRP}$<br>( $t = 100\text{ }\mu\text{s}$ ) | —  | —   | —    | 400  | A    |
| Diode forward voltage                   | $V_{DSF}$                                     | $I_{DR} = 80\text{ A}$ , $V_{GS} = 0\text{ V}$   | —   | —    | -1.5 | V    |
| Reverse recovery time                   | $t_{rr}$                                      | $I_{DR} = 20\text{ A}$ , $V_{GS} = 0\text{ V}$ ,<br>$-di_{DR}/dt = 100\text{ A}/\mu\text{s}$ | —   | 55   | —    | ns   |
| Reverse recovery charge                 | $Q_{rr}$                                      |  | —   | 72   | —    | nC   |

Note 5: Ensure that the channel temperature does not exceed  $175\text{ }^\circ\text{C}$ .

## 7. Marking (Note)

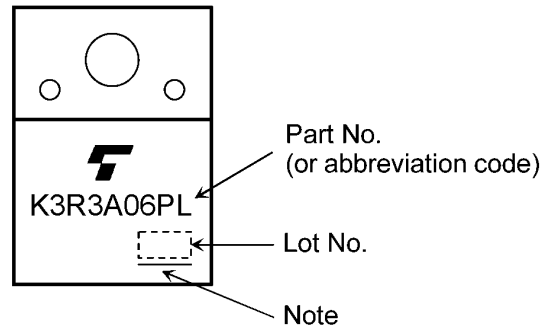


Fig. 7.1 Marking

Note: A line under a Lot No. identifies the indication of product Labels.

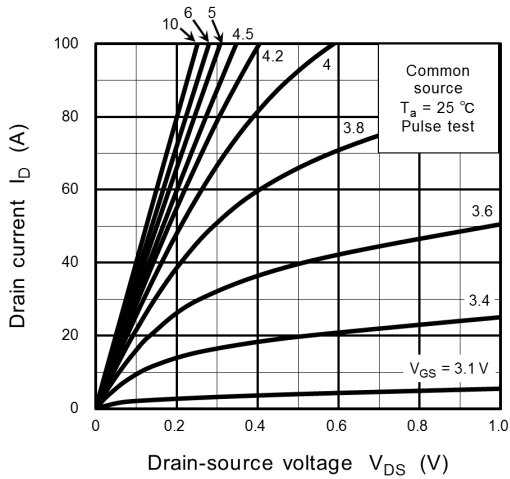
Not underlined: [[Pb]]/INCLUDES > MCV

Underlined: [[G]]/RoHS COMPATIBLE or [[G]]/RoHS [[Pb]]

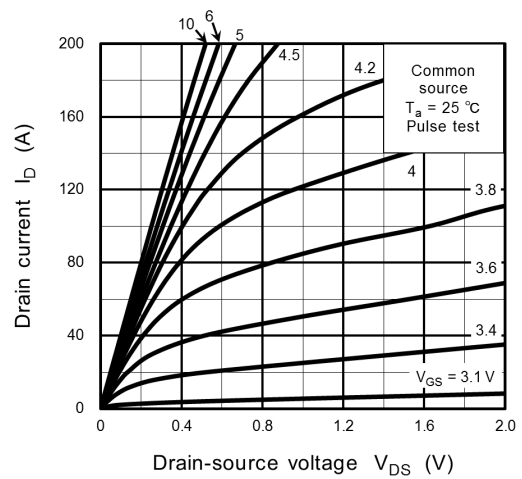
Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product.

The RoHS is the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

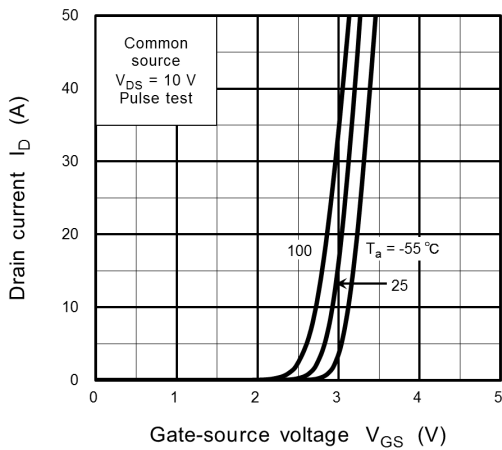
## 8. Characteristics Curves (Note)



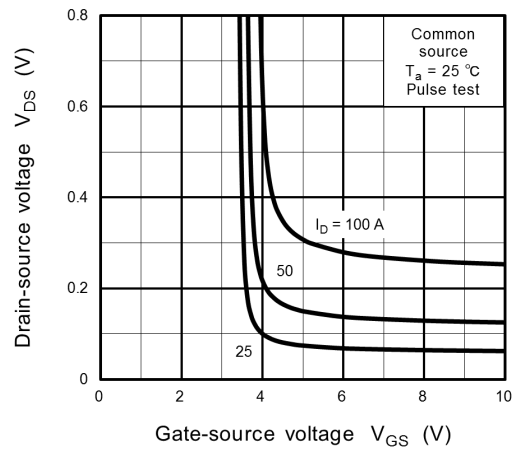
**Fig. 8.1  $I_D - V_{DS}$**



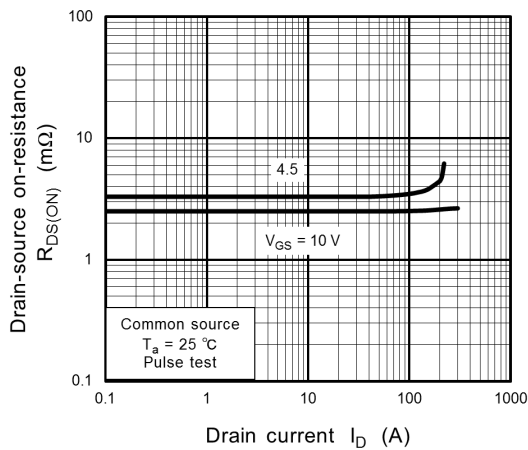
**Fig. 8.2  $I_D - V_{DS}$**



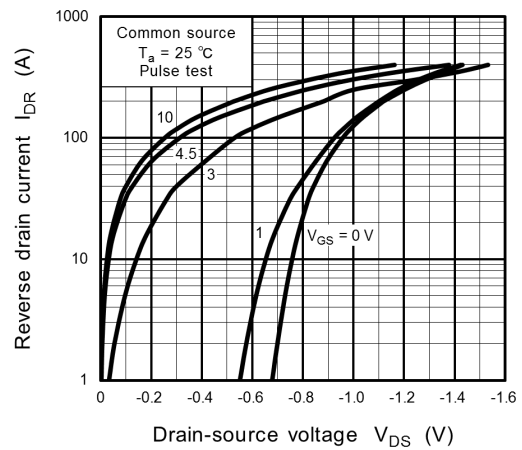
**Fig. 8.3  $I_D - V_{GS}$**



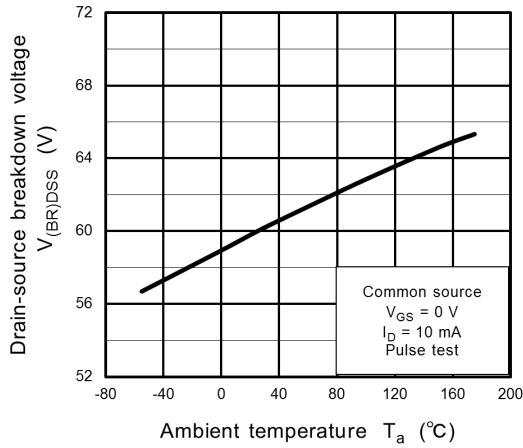
**Fig. 8.4  $V_{DS} - V_{GS}$**



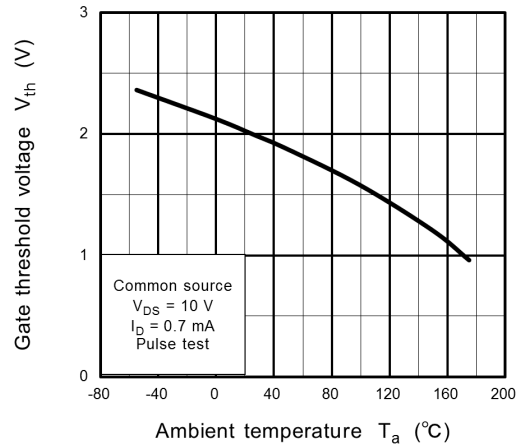
**Fig. 8.5  $R_{DS(ON)} - I_D$**



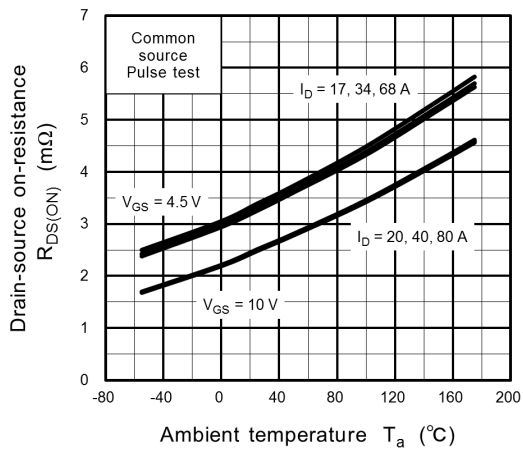
**Fig. 8.6  $I_{DR} - V_{DS}$**



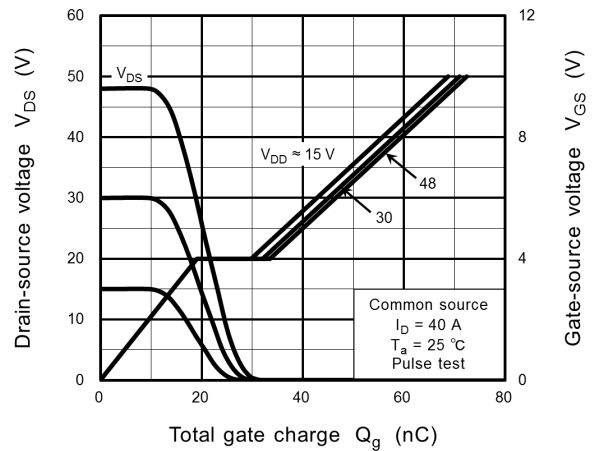
**Fig. 8.7**  $V_{(BR)DSS} - T_a$



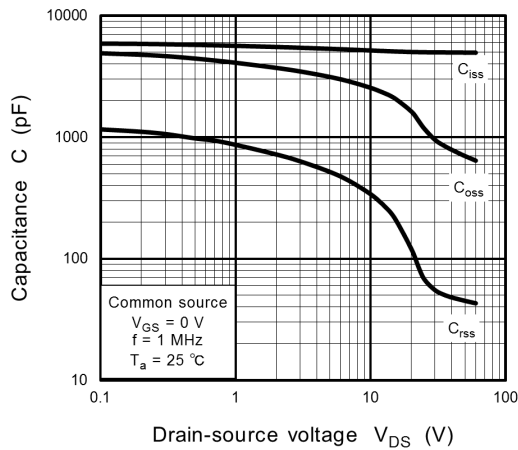
**Fig. 8.8**  $V_{th} - T_a$



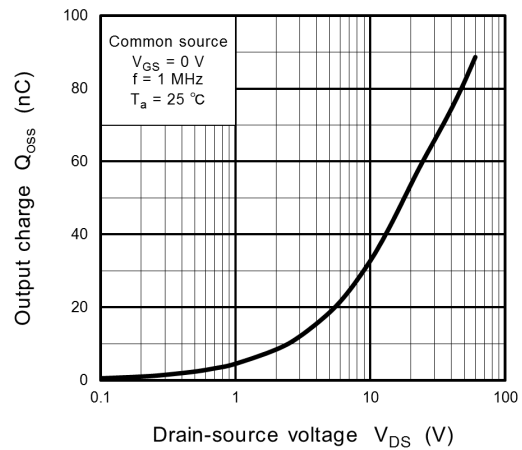
**Fig. 8.9**  $R_{DS(ON)} - T_a$



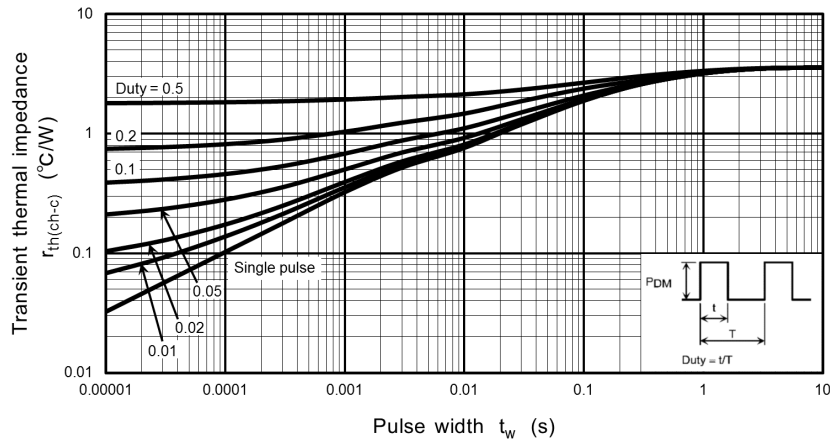
**Fig. 8.10** Dynamic Input/Output Characteristics



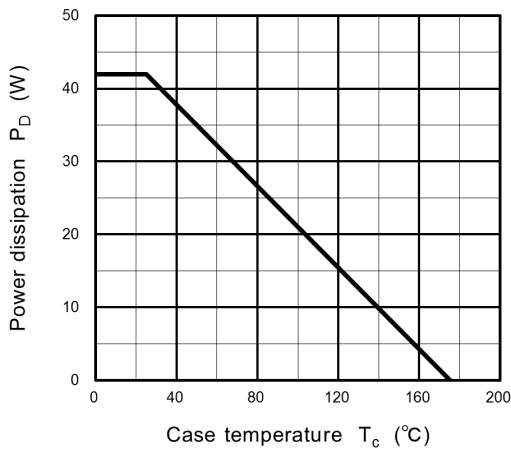
**Fig. 8.11** Capacitance -  $V_{DS}$



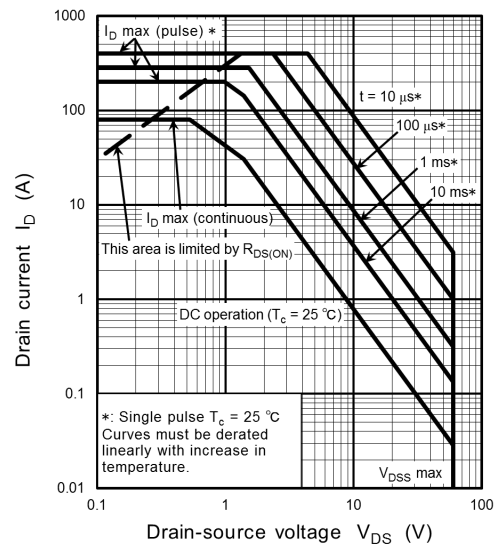
**Fig. 8.12**  $Q_{oss} - V_{DS}$



**Fig. 8.13  $r_{th} - t_w$**   
(Guaranteed Maximum)



**Fig. 8.14  $P_D - T_c$**   
(Guaranteed Maximum)



**Fig. 8.15 Safe Operating Area**  
(Guaranteed Maximum)

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

## Package Dimensions

Unit: mm



Weight: 1.7 g (typ.)

| Package Name(s)     |
|---------------------|
| TOSHIBA: 2-10U1S    |
| Nickname: TO-220SIS |



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