

SiC Schottky Barrier Diode

TRS2E65F

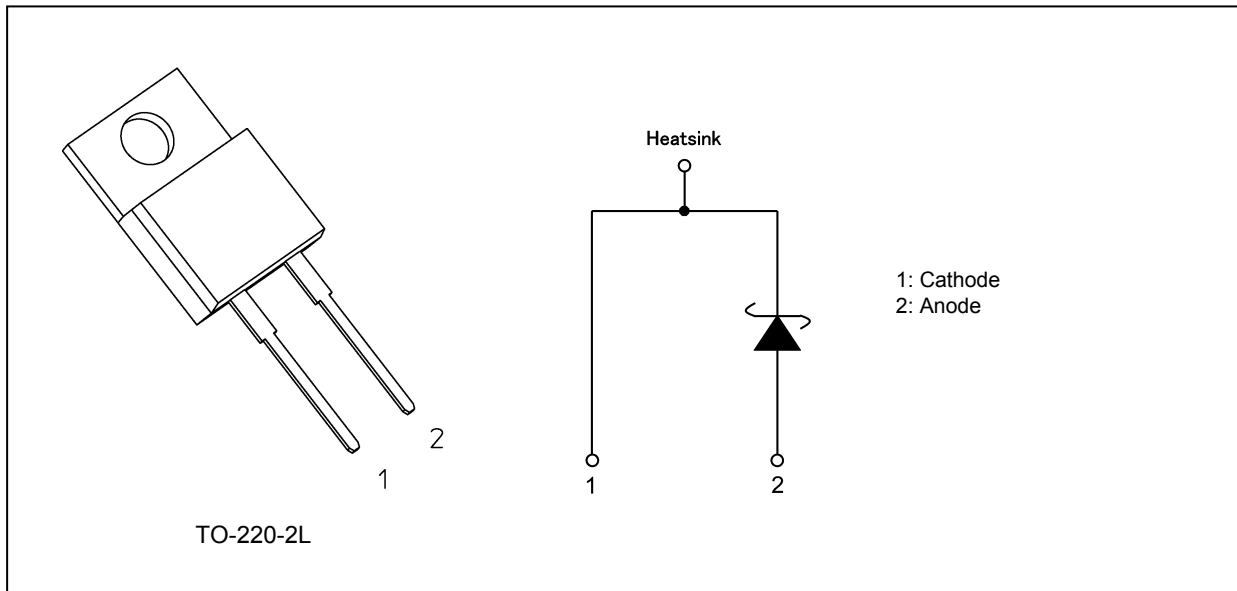
1. Applications

- Power Factor Correction
- Solar Inverters
- Uninterruptible Power Supplies
- DC-DC Converters

2. Features

- (1) Chip design of 2nd generation.
- (2) High surge current capability : $I_{FSM} = 21A$ (Max)
- (3) The junction capacitance is small : $C_j = 8.7pF$ (Typ.)
- (4) The reverse current is small. : $I_R = 0.2 \mu A$ (Typ.)

3. Packaging and Internal Circuit



Start of commercial production
2017-06

4. Absolute Maximum Ratings (Note) (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$)

Characteristics	Symbol	Note	Rating	Unit
Repetitive peak reverse voltage	V_{RRM}		650	V
Forward DC current	$I_{F(DC)}$		2	A
Forward pulse current	I_{FP}	(Note 1)	20	A
Non-repetitive peak forward surge current	I_{FSM}	(Note 2)	21	A
Junction temperature	T_j		175	$^\circ\text{C}$
Storage temperature	T_{stg}		-55 to 175	$^\circ\text{C}$
Mounting torque	TOR		0.6	N · m

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: $t = 50\text{ }\mu\text{s}$

Note 2: $f = 50\text{ Hz}$ (half-sine wave $t = 10\text{ ms}$)

5. Thermal Characteristics

Characteristics	Symbol	Test Condition	Max	Unit
Thermal resistance (junction-to-case)	$R_{th(j-c)}$	—	3.6	$^\circ\text{C/W}$
Thermal resistance (junction-to-ambient)	$R_{th(j-a)}$	—	89	$^\circ\text{C/W}$

6. Electrical Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Forward voltage	V_F (1)	$I_F = 1\text{ A}$ (pulse measurement)	—	1.2	—	V
Forward voltage	V_F (2)	$I_F = 2\text{ A}$ (pulse measurement)	—	1.45	1.6	V
Reverse current	I_R	$V_R = 650\text{ V}$ (pulse measurement)	—	0.2	20	μA
Junction capacitance	C_j	$V_R = 650\text{ V}$, $f = 1\text{ MHz}$	—	8.7	—	pF

7. Marking

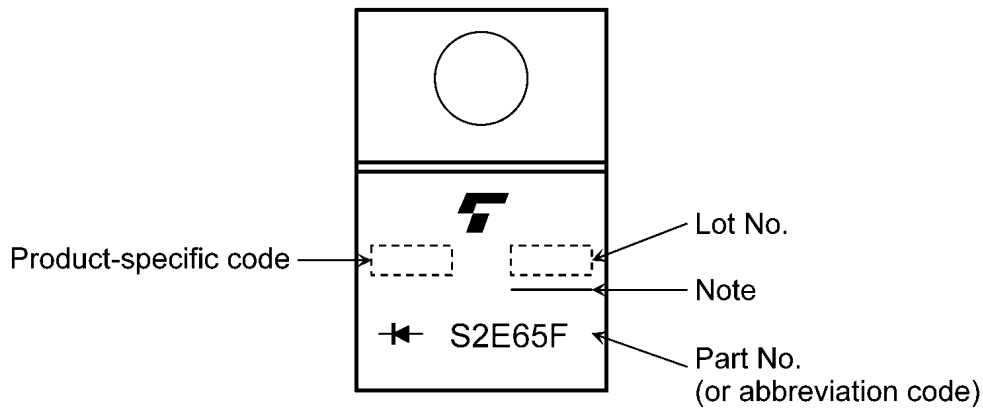


Fig. 7.1 Marking

Note: A line under a Lot No. identifies the indication of product Labels.

[[G]]/RoHS COMPATIBLE or [[G]]/RoHS [[Pb]]

Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product.

The RoHS is the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

Abbreviation Code	Part Number
S2E65F	TRS2E65F

8. Usage Considerations

- (1) The absolute maximum ratings are rated values that must not be exceeded during operation, even for an instant.

The following are the recommended general derating methods for designing a circuit board using this device.

V_{RRM} : V_{RRM} has a temperature coefficient of 0.1 %/°C.

Take this coefficient into account when designing a circuit board that will be operated in a low-temperature environment.

$I_{F(DC)}$: We recommend that the worst-case current be no greater than 80 % of the absolute maximum rating of $I_{F(DC)}$.

I_{FP} : We recommend that the worst-case current be no greater than 80 % of the absolute maximum rating of I_{FP} .

I_{FSM} : This rating specifies a non-repetitive limit value.

This only applies to an abnormal operation, which seldom occurs during the lifespan of a device.

T_j : Derate device parameters in proportion to this rating in order to ensure high reliability.

We recommend that the junction temperature (T_j) of a device be kept below 140 °C.

- (2) For other design considerations, see the Toshiba Semiconductor website.

9. Characteristics Curves (Note)

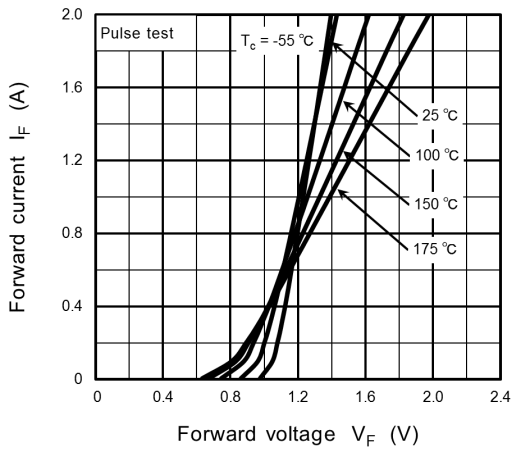


Fig. 9.1 $I_F - V_F$

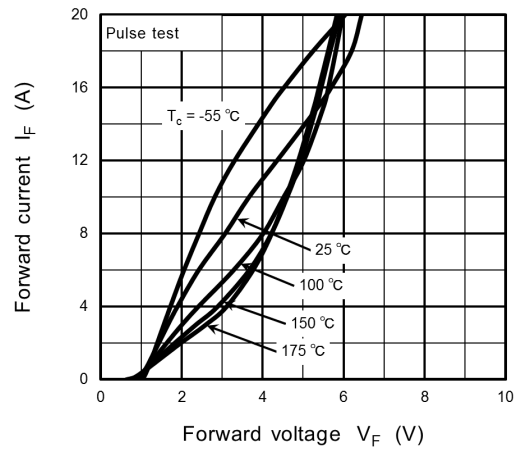


Fig. 9.2 $I_F - V_F$

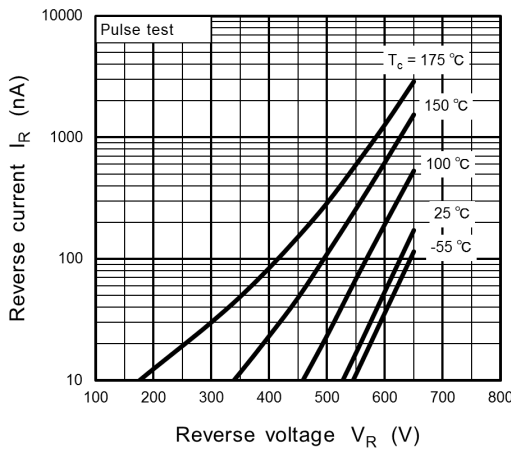


Fig. 9.3 $I_R - V_R$

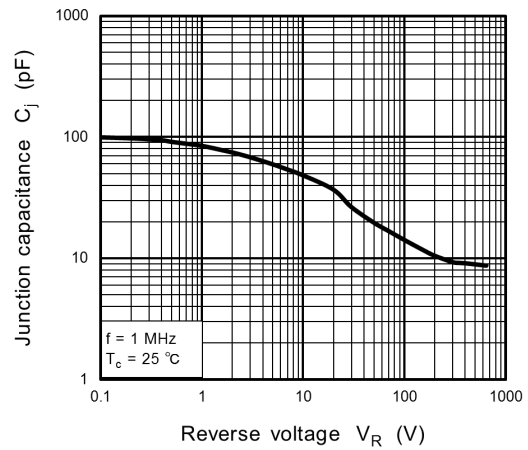
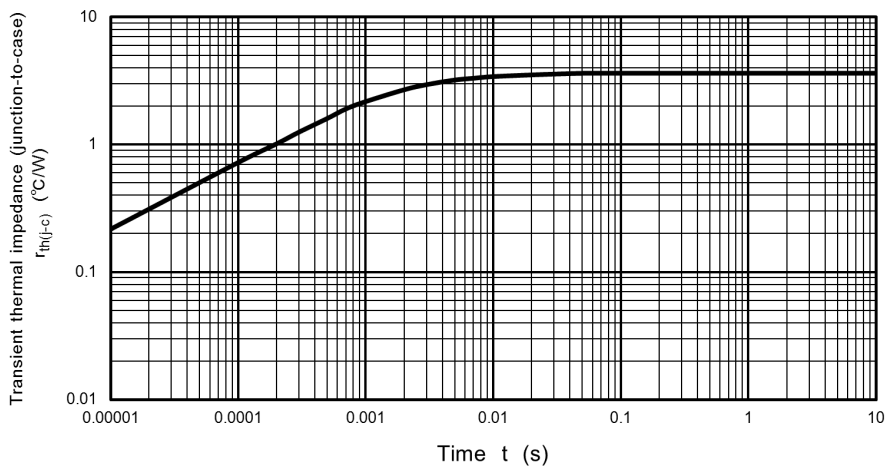


Fig. 9.4 $C_j - V_R$



**Fig. 9.5 $r_{th(j-c)} - t$
(Guaranteed Maximum)**

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

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