32-bit RISC Microcontroller

TXZ Family

Reference Manual
Debug Interface
(DEBUG-A)

Revision 1.3

2019-07

TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

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Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 – Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 – It is possible to omit the "0b" when the number of bit can be distinctly
  understood from a sentence.

- "_N" is added to the end of signal names to indicate low active signals.

- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.

- When two or more signal names are referred, they are described like as [m: n].
  Example: S[3:0]   shows four signal names S3, S2, S1 and S0 together.

- The characters surrounded by *[ ]* defines the register.
  Example: *[ABCD]*

- "n" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: *[XYZ1], [XYZ2], [XYZ3] → [XYZn]*

- "x" substitutes suffix number or character of units and channels in the Register List.
  In case of unit, "x" means A, B, and C …
  Example: *[ADACR0], [ADBCR0], [ADCCR0] → [ADxCR0]*
  In case of channel, "x" means 0, 1, and 2…
  Example: *[T32A0RUNA], [T32A1RUNA], [T32A2RUNA] → [T32AxRUNA]*

- The bit range of a register is written like as [m: n].
  Example: Bit[3:0] expresses the range of bit 3 to 0.

- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: *[ABCD]*<EFG> = 0x01 (hexadecimal), *[XYZn]*<VW> = 1 (binary)

- Word and Byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits

- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and Write are possible

- Unless otherwise specified, register access supports only word access.

- The register defined as reserved must not be rewritten. Moreover, do not use the read value.

- The value read from the bit having default value of "-" is unknown.

- When a register containing both of writable bits and read-only bits is written, read-only bits should be
  written with their default value, In the cases that default is "-", follow the definition of each register.

- Reserved bits of the Write-only register should be written with their default value. In the cases that default is
  "-", follow the definition of each register.

- Do not use read-modified-write processing to the register of a definition which is different by writing and
  read out.

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Terms and Abbreviations

Some of abbreviations used in this document are as follows:

SWJ-DP	Serial Wire JTAG Debug Port
ETM	Embedded Trace Macrocell^{TM}
TPIU	Trace Port Interface Unit
JTAG	Joint Test Action Group
SW	Serial Wire
SWV	Serial Wire Viewer

1. Outlines

The Serial Wire JTAG Debug Port (SWJ-DP) unit for interfacing with the debugging tools and the Embedded Trace Macrocell (ETM) unit for instruction trace output are built-in. Trace data is output to the dedicated pins(TRACEDATA[3:0], SWV) for the debugging via the on-chip Trace Port Interface Unit (TPIU).

Table 1.1   Features

Function Classification	Function	Operation
SWJ-DP	JTAG	It is possible to connect the JTAG support debugging tools.
	SW	It is possible to connect the Serial Wire debugging tools.
ETM	Trace	It is possible to connect the ETM Trace support debugging tools.

For details about SWJ-DP, ETM and TPIU, refer to "Arm documentations set".

2. Configuration

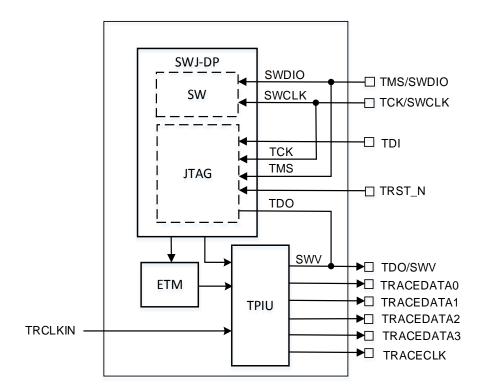Figure 2.1 shows the block diagram of the debug interface.

Figure 2.1   DEBUG block diagram

Table 2.1 List of Signals

No.	Symbol	Signal Name	I/O	Related Reference Manual
1	TRCLKIN	Trace function Clock	Input	Clock Control and Operation Mode
2	TMS	JTAG Test Mode Selection	Input	Input/Output Ports, Product Information
3	SWDIO	Serial Wire Data Input/Output	Input/Output	Input/Output Ports, Product Information
4	TCK	JTAG Serial Clock input	Input	Input/Output Ports, Product Information
5	SWCLK	Serial Wire Clock	Input	Input/Output Ports, Product Information
6	TDO	JTAG Test Data Output	Output	Input/Output Ports, Product Information
7	SWV	Serial Wire Viewer Output	Output	Input/Output Ports, Product Information
8	TDI	JTAG Test Data Input	Input	Input/Output Ports, Product Information
9	TRST_N	JTAG Test RESET_N	Input	Input/Output Ports, Product Information
10	TRACEDATA0	Trace Data 0	Output	Input/Output Ports, Product Information
11	TRACEDATA1	Trace Data 1	Output	Input/Output Ports, Product Information
12	TRACEDATA2	Trace Data 2	Output	Input/Output Ports, Product Information
13	TRACEDATA3	Trace Data 3	Output	Input/Output Ports, Product Information
14	TRACECLK	Trace Clock	Output	Input/Output Ports, Product Information

● SWJ-DP

SWJ-DP supports the Serial Wire Debug Port (SWCLK, SWDIO), the JTAG Debug Port (TDI, TDO, TMS, TCK, TRST_N) and trace output from Serial Wire Viewer(SWV).

When you use the SWV, please set an applicable clock enable bit to 1 (clock supply) in Clock supply and stop register (*[CGSPCLKEN]*<TRCKEN>). For details, see the "Clock Control and Operation Mode" and "Input/Output Ports" of the reference manual.

The JTAG Debug Port or TRST_N pin does not exist depending on the product. For details, see the "Product Information" of the reference manual.

● ETM

ETM supports data signal to four pins(TRACEDATA) and one clock signal pin (TRACECLK).

When you use the ETM, please set an applicable clock enable bit to 1 (clock supply) in Clock supply and stop register (*[CGSPCLKEN]*<TRCKEN>). For details, see the "Clock Control and Operation Mode" and "Input/Output Ports" of the reference manual.

ETM is not supported depending on the product. For details, see the "Product Information" of the reference manual.

3. Function and Operation

3.1. Clock Supply

When you use the Trace or SWV, please set an applicable clock enable bit to 1 (clock supply) in ADC Trace Clock supply stop register (*[CGSPCLKEN]*<TRCKEN>). For details, see the "Clock Control and Operation Mode" of the reference manual.

3.2. Connection with debug tool

Concerning a connection with debug tools, refer to manufactures recommendations. Debug interface pins contain a pull-up resistor and a pull-down resistor. When debug interface pins are connected with external pull-up or pull-down, please pay attention to input level.

When the security function is enabled, the CPU cannot connect to debug tool.

3.3. Peripheral Functions in Halt Mode

The hold mode means that the state where the CPU is stopped (break) on the debugging tool

When the CPU enters in the halt mode, the watchdog timer (WDT) automatically stops. Other peripheral functions continue to operate.

4. Usage Example

The debug interface pins can also be used as general-purpose ports.

After releasing reset, the particular pins of the debug interface pins are initialized as the debug interface pins. The other debug interface pins should be changed to the debug interface pins if needed.

Table 4.1   Debug Interface usage example

Debug Interface		Debug interface pins						
	JTAG	TRST_N	TDI	TDO	TCK	TMS	TRACEDATA [3:0]	TRACECLK
	SW	-	-	SWV	SWCLK	SWDIO		
Debug pins status after releasing reset		Valid	Valid	Valid	Valid	Valid	Invalid	Invalid
JTAG (With TRST_N)		✓	✓	✓	✓	✓	N/A	N/A
JTAG (without TRST_N)		N/A	✓	✓	✓	✓	N/A	N/A
JTAG+TRACE		✓	✓	✓	✓	✓	✓	✓
SW		N/A	N/A	N/A	✓	✓	N/A	N/A
SW+TRACE		N/A	N/A	N/A	✓	✓	✓	✓
SW+SWV		N/A	N/A	✓	✓	✓	N/A	N/A
Debug function Disable		N/A	N/A	N/A	N/A	N/A	N/A	N/A

✓: Usage   N/A: Not Available

5. Precaution

5.1. Important points of using debug interface pins used as general-purpose ports

After releasing reset, if the debug interface pins are used as the general I/O ports by the user program, the debug tool cannot be connected.

If the debug interface pins are used to other function, please pay attention of the settings.

If the debug tool cannot be connected, it can recover debug connection to erase the flash memory using single BOOT mode from external. For details, please refer reference manual of "Flash Memory".

6. Revision History

Table 6.1   Revision History

Revision	Date	Description
1.0	2017-09-04	First release

1.1	2018-06-19	- Contents
		   Modified Table of Contents to Contents
		-1 Outline
		   Modified ARM to Arm.
		-2. Configuration
		   Reference "reference manual" is added to SWJ-DP
		   Reference "reference manual" is added to SWJ-ETM

1.2	2018-10-22	- Conventions
		   Modified explanation of trademark
		- 4. Usage Example
		   Added example for SW+TRACE in Table4.1
		- Replaced RESTRICTIONS ON PRODUCT USE

1.3	2019-07-26	- Figure 2.1 revised - 2 Added clock setting for using SWV function. - 3.1 Added clock setting for using SWV function. modified from "ETM" to "Trace". - 3.3 Added description of Hold mode.

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