32-bit RISC Microcontroller

TXZ/TXZ+ Family

Reference Manual

Clock Selective Watchdog Timer (SIWDT-A)

Revision 3.2

2023-09

TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

Contents

List of Figures

List of Tables

Preface

Related document

Document name
Clock Control and Operation Mode
Exception
Power Supply and Reset Operation
Product Information

Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 – Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 – It is possible to omit the "0b" when the number of bit can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m: n].
  Example: S[3: 0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- "n" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1], [XYZ2], [XYZ3] → [XYZn]***
- "x" substitutes suffix number or character of units and channels in the Register List.
  In case of unit, "x" means A, B, and C …
  Example: ***[ADACR0], [ADBCR0], [ADCCR0] → [ADxCR0]***
  In case of channel, "x" means 0, 1, and 2…
  Example: ***[T32A0RUNA], [T32A1RUNA], [T32A2RUNA] → [T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> = 0x01 (hexadecimal), ***[XYZn]***<VW> = 1 (binary)
- Word and Byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and Write are possible
- Unless otherwise specified, register access supports only word access.
- The register defined as reserved must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "-" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is "-", follow the definition of each register.
- Reserved bits of the Write-only register should be written with their default value. In the cases that default is "-", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

Terms and Abbreviations

Some of abbreviations used in this document are as follows:

SIWDT	Clock Selective Watchdog Timer

1. Outlines

When the CPU executes mal function (a runaway) caused by a noise or others, the watchdog timer detects it and gives a trigger to the CPU to resume the correct function.

Function Classification	Function	Operation
Timer Control	Clock selection	It is possible to select the source clock of runaway detection from "fsys/4","fIHOSC1","fIHOSC2".
	Detection time control	It is possible to select the detection time between 2^{15} to 2^{29} count of the selection clock.
Decision Control	Window selection	It is possible to select the clear window of runaway detection from "No settings", "Later 1/2" and "Last 1/4".
Detection Control	Detection behavior	It is possible to select behavior of the runaway detection from "Interrupt" and "Reset".
Protection Control	Mode selection	It is possible to select the "Protection A mode" which cannot be released except for RESET, and "Protection B mode" which can be released by ***[SIWDxPRO]***<PROTECT>.
	Control of modification of the oscillation clock control bit of the internal high-speed oscillator (IHOSC2)	It is possible to control modification of the oscillation clock control bit of the internal high-speed oscillator (IHOSC2).

2. Configuration

Figure 2.1 shows the block diagram of the watchdog timer.

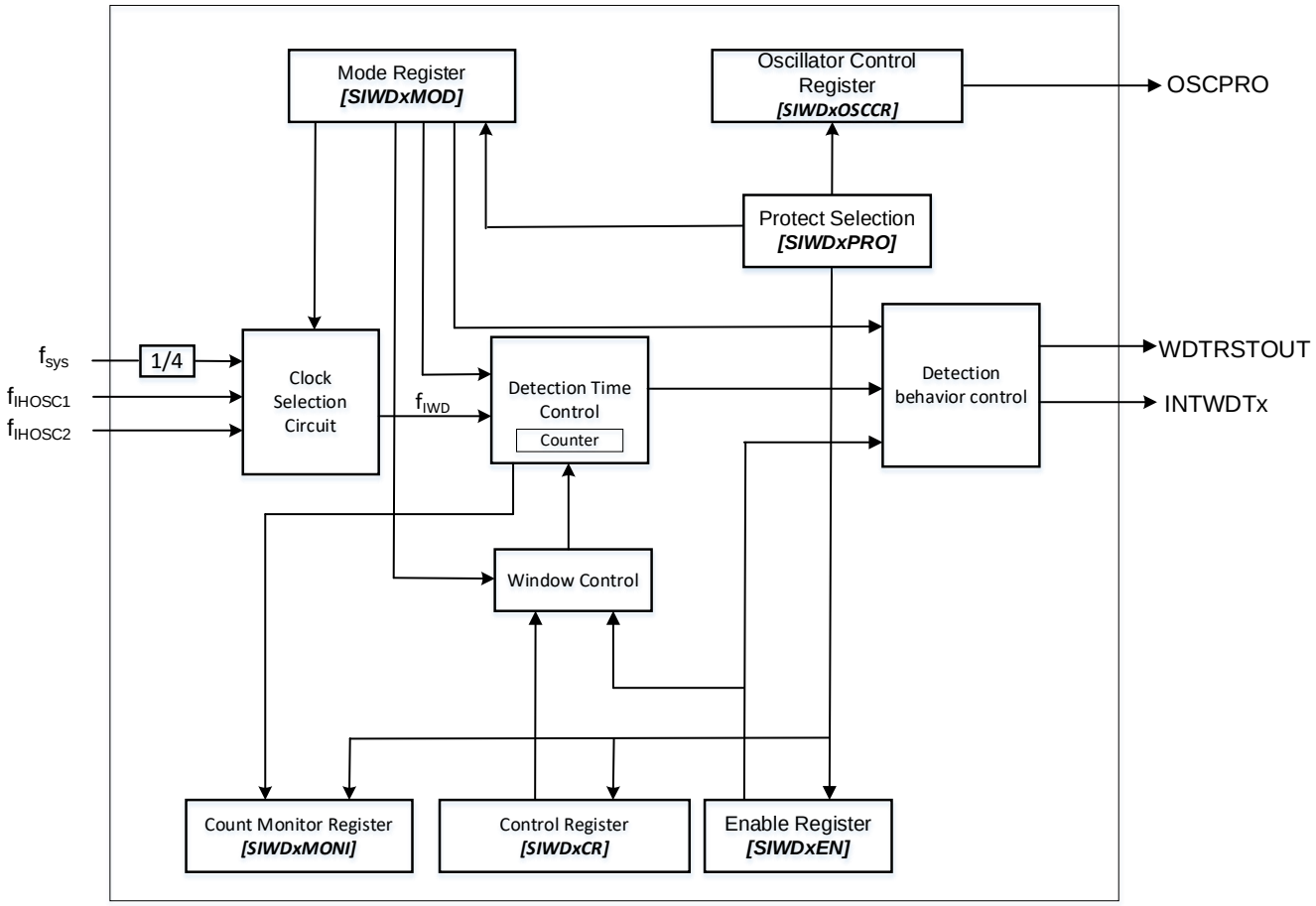

Figure 2.1 SIWDT block diagram

Table 2.1 List of Signals

No.	Symbol	Signal Name	I/O	Related Reference Manual
1	fsys	System Clock	Input	Clock Control and Operation Mode
2	f_{IHOSC1}	Internal Oscillator 1	Input	Clock Control and Operation Mode
3	f_{IHOSC2}	Internal Oscillator 2	Input	Clock Control and Operation Mode
4	INTWDTx	Watchdog Timer Interrupt	Output	Exception
5	WDTRSTOUT	Watchdog Timer Reset	Output	Clock Selective Watchdog Timer Clock Control and Operation Mode (Note)
6	OSCPRO	Control of modification of the oscillation clock control bit of the internal high-speed oscillator (IHOSC2)	Output	Product Information

Note: Refer to " Clock Selective Watchdog Timer" for TXZ family and " Clock Control and Operation Mode" for TXZ+ family.

3. Function and Operation

3.1. Basic Operation

The watchdog timer (WDT) is for detecting malfunctions (runaway) of the CPU caused by noises or other disturbances and remedying them to return the CPU to normal operation.

If the watchdog timer detects a runaway, it generates a INTWDTx interrupt or reset. When the clear code (0x4E) is written to the ***[SIWDxCR]*** register, the counter is cleared and re-starts the count.

3.2. Clock Supply

The SIWDT starts the count immediately after the reset is deasserted. The selected clock is "the system clock (fsys) of 4 division" at that time. If the watchdog timer is not used, it should be disabled. When the setting is changed, it should be disabled, too.

3.3. Clock Selection Circuit

3.3.1. Clock Selection

The clock which is selected from "the system clock (fsys) of 4 division", "internal oscillation clock 1 (f_{IHOSC1})", and "internal oscillation clock 2 (f_{IHOSC2})" by ***[SIWDxMOD]***<WDCLS>, is used as input clock.

3.3.2. Clock Run and Stop

If you want to stop the count clock, you should confirm that the SIWDT is stopping.

The operation of SIWDT set to “1” to ***[SIWDxEN]***<WDTE>.

The ***[SIWDxCR]*** register should be set to disable code(0xB1) after the ***[SIWDxEN]***<WDTE> set to “0” for stopping SIWDT. The SIWDT is disabled, and counter is cleared.

3.4. Detection Time Control

The detection time is selected from among 2^{15},2^{17},2^{19},2^{21},2^{23},2^{25},2^{27} and 2^{29} by ***[SIWDxMOD]***<WDTP[2:0]>.

3.5. Detection Behavior Control

The generator which is selected by the ***[SIWDxMOD]***<RESCR> after the elapse of detection time, is "watchdog timer interrupt(INTWDTx)", or "reset".

3.6. Window Control

3.6.1. Clear Window Setting

The clear window is selected with ***[SIWDxMOD]***<WDCWD> from among none specified, the latter half of the detection interval, and the last quarter of the detection interval.

If the clear code is written during the clear window interval, the counter is cleared and re-starts the count.

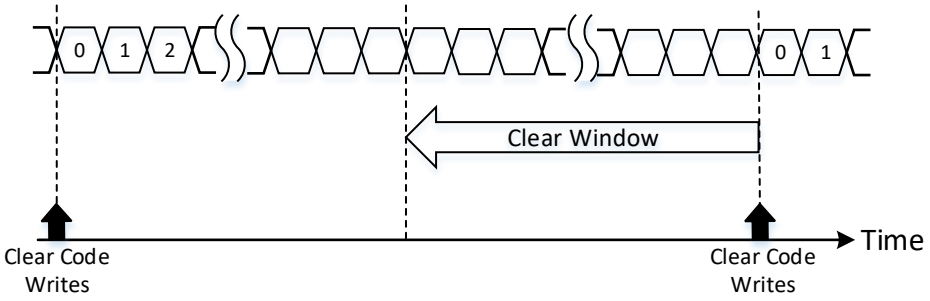

Figure 3.1 Clear code writes during the clear window interval

If the clear code is written before the clear window, the operation is as follows according to the setting of ***[SIWDxMOD]***<RESCR>.

When ***[SIWDxMOD]***<RESCR> = 1 and the reset generation is enabled, the reset is asserted and the SIWDT becomes the initialization state.

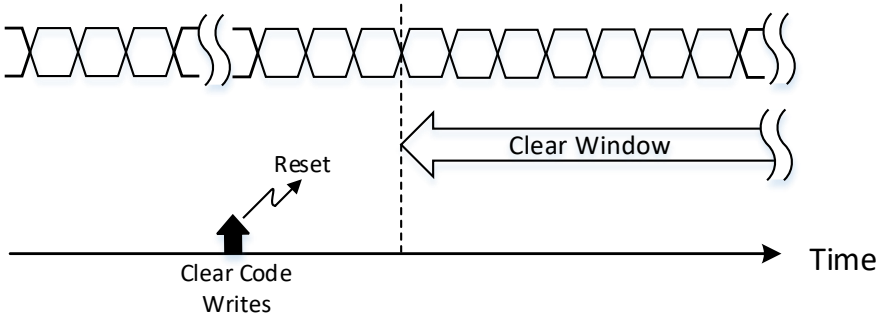

Figure 3.2 Clear code writes before the clear window (1)

When ***[SIWDxMOD]***<RESCR> = 0 or the INTWDTx generation is enabled, the INTWDTx is generated and ***[SIWDxMOD]***<INTF> is set to 1 every write of the clear code. The counter continues the count and the INTWDTx is generated at the detection time, again.

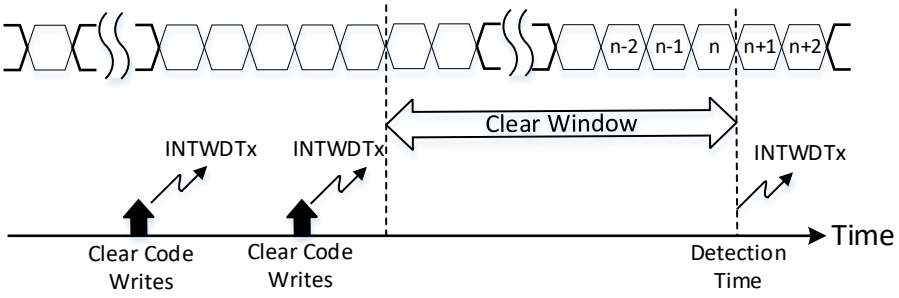

Figure 3.3 Clear code writes before the clear window (2)

3.7. Protection Control

3.7.1. Protection Mode

There are two types of protection modes to prevent from unexpected writing. Its setting should be done while ***[SIWDxEN]***<WDTE> is "1".

(a) Protection A mode

[SIWDxPRO]<PROTECT> should be set to 0xA9 to select the protection A mode.

Only 0x4E (Clear code) can be written to ***[SIWDxCR]***<WDCR> in this mode. Other code write is ignored.

The protection A mode can be cleared only by the reset initialization.

(b) Protection B mode

[SIWDxPRO]<PROTECT> should be set to 0x74 to select the protection B mode.

Only 0x4E (Clear code) can be written to ***[SIWDxCR]***<WDCR> and only 0x1E (protection B mode clear) can be written to ***[SIWDxPRO]*** <PROTECT>. Other code write to the fields is ignored.

3.7.2. Oscillation Clock Control Bit of Internal High-speed Oscillator (IHOSC2)

When ***[SIWDxOSCCR]***<OSCPRO> is set to "1", the write is inhibited to the oscillation clock control bit of the internal high-speed oscillator (IHOSC2).

For the internal oscillation clock control bit, refer to Reference Manual "Product Information".

3.8. Monitor Register Control

The ***[SIWDxMONI]***<MONI[29:0]> should be read multiple times. When the read value is different. it is shown that the counter is working.

3.9. Operation Status of Counter

In debug halt, the counter of SIWDT is stopped.

Refer to Reference Manual "Clock Control and Operation Mode" for each operation mode.

4. Registers

4.1. List of Registers

The control registers and their addresses are shown as follows:

Peripheral function		Channel /Unit	Base address		
			TYPE 1	TYPE 2	TYPE 3
Watchdog Timer	SIWDT	ch0	0x400BB400	0x400A0600	0x40040600
		ch1	-	0x400A0700	0x40040700

Note: The channel/unit and base address type are different by products. Please refer to "Products Information" of the reference manual for the details.

Register Name		Address (Base+)
Protection Register	***[SIWDxPRO]***	0x0000
Enable Register	***[SIWDxEN]***	0x0004
Control Register	***[SIWDxCR]***	0x0008
Mode Register	***[SIWDxMOD]***	0x000C
Count Monitor Register	***[SIWDxMONI]***	0x0010
Oscillator Control Register	***[SIWDxOSCCR]***	0x0014

4.2. Details of Registers

4.2.1. *[SIWDxPRO]* (Protection Register)

Bit	Bit Symbol	After Reset	Type	Function
31:8	-	0	R	Read as “0”
7:0	PROTECT[7:0]	0x1E	R/W	Protection mode 0x1E: No protection 0xA9: Protection A mode setting 0x74: Protection B mode setting The other settings are ignored.

Note: When ***[SIWDxEN]***<WDTF> is “Operating,” this field can be written except in the protection A mode.

4.2.2. *[SIWDxEN]* (Enable Register)

Bit	Bit Symbol	After Reset	Type	Function
31:2	-	0	R	Read as “0”
1	WDTF	1	R	Operation flag 0: Stop 1: Operating SIWDT operation status is shown.
0	WDTE	1	R/W	Enable or Disable control 0: Disabled. 1: Enabled. When the watchdog timer is disabled, it is necessary to disable that this bit should be set to 0 and then the disable code (0xB1) should be written to ***[SIWDxCR]***<WDCR>. ***[SIWDxEN]***<WDTE> should be set to 1 to return to the enable state.

4.2.3. *[SIWDxCR]* (Control Register)

Bit	Bit Symbol	After Reset	Type	Function
31:8	-	0	R	Read as “0”
7:0	WDCR[7:0]	Undefined	W	Disable code and Clear code 0xB1: Disable code 0x4E: Clear code The other code writes are ignored.

4.2.4. *[SIWDxMOD]* (Mode Register)

Bit	Bit Symbol	After Reset	Type	Function
31:14	-	0	R	Read as “0”
13:12	WDCLS[1:0]	00	R/W	Clock selection 00: fsys/4 01: internal oscillation clock (IHOSC1) 10: internal oscillation clock (IHOSC2) 11: Reserved.
11	-	0	R	Read as “0”
10:8	WDTP[2:0]	000	R/W	Detection time selection (f_{IWD} = The clock which is selected by <WDCLS>) 000: $2^{15}/f_{IWD}$ 001: $2^{17}/f_{IWD}$ 010: $2^{19}/f_{IWD}$ 011: $2^{21}/f_{IWD}$ 100: $2^{23}/f_{IWD}$ 101: $2^{25}/f_{IWD}$ 110: $2^{27}/f_{IWD}$ 111: $2^{29}/f_{IWD}$
7:6	-	0	R	Read as “0”
5:4	WDCWD[1:0]	00	R/W	Clear window setting 00: No settings 01: Latter 1/2 10: Last 1/4 11: Reserved.
3:2	-	0	R	Read as “0”
1	INTF	0	R	INTWDTx generation by the clear code write before the clear window 0: Not generated. 1: Generated.
			W	The clear set of flag 0: don’t care 1: clear to “0”
0	RESCR	1	R/W	Operation after the runaway detection 0: INTWDTx interrupt request is generated. 1: Reset is asserted to MCU.

Note: This can be written when ***[SIWDxEN]***<WDTF> is “Stop” except in the protection setting state.

4.2.5. *[SIWDxMONI]* (Count Monitor Register)

Bit	Bit Symbol	After Reset	Type	Function
31:30	-	0	R	Read as “0”
29:0	MONI[29:0]	Undefined	R	Counter monitor This register should be read multiple times. When the read values are different, it is shown that the counter is working. The read value is not precisely correct. It should be used as a reference value.

4.2.6. *[SIWDxOSCCR]* (Oscillation Enable Register)

Bit	Bit Symbol	After Reset	Type	Function
31:1	-	0	R	Read as “0”
0	OSCPRO	0	R/W	Write protection for the oscillation clock control bit of the internal high-speed oscillator (IHOSC2). (Note2) 0: Disable 1: Enable

Note1: When ***[SIWDxEN]***<WDTF> is “Stop”, this bit can be written except in the protection setting state.

Note2: For the oscillation clock control bit of the internal high-speed oscillator (IHOSC2), refer to Reference Manual “Product Information”.

5. Precaution

- When ***[SIWDxPRO]*** is “0x1E”(No protection) or “0x74” (Protection B mode)
  Before CPU transfer low-power consumption mode (STOP1/STOP2/IDLE) from Normal mode, the watchdog timer should be disabled. For details of setting procedure, refer to the Reference Manual “Clock Control and Operation Mode”.

- When ***[SIWDxPRO]*** is “ 0x9A” (Protection A mode)
  The count clock operation in each low-power consumption mode is shown in Table 5.1. For the oscillation clock control bit of the internal high-speed oscillator (IHOSC2), refer to the Reference Manual “Product Information”.

Table 5.1 Count Clock Operation in Each Low-power Consumption Mode

Count clock		IDLE mode	STOP1 mode
fsys/4		Keep up	Stopped
f_{IHOSC1}		Keep up	Stopped
f_{IHOSC2}	When oscillation clock control bit is ***[CGOSCCR]***<IHOSC2EN>	Keep up	Stopped
	When oscillation clock control bit is ***[RLMLOSCCR]***<POSCEN>	Keep up	Keep up

6. Revision History

Table 6.1 Revision History

Revision	Date	Description
1.0	2017-09-08	First release
2.0	2018-03-23	- 3.5 Detection Behavior Control Added INTWDTx in “watchdog timer interrupt” - 3.9 Operation Mode and Operation Status Added Table 3.1 - 4.1 List of Register Modified Note - 4.2.4 ***[SIWDxMOD]*** Modified INTWDT to INTWDTx of <INTF><RESCR> - Precaution Modified explanation
3.0	2018-06-19	- 1 Outlines Deleted Table title - 4.1 List of Registers Added base address of TYPE2(ch1) and TYPE3 - 4.2.3 ***[SIWDxCR]*** Modified after reset value of <WDCR[7:0]> to undefined - 4.2.5 ***[SIWDxMONI]*** Modified after reset value of <MONI[29:0]> to undefined
3.1	2023-06-14	- 1. Outlines Name and description of the 2nd function of “Protection Control” are changed. - Table 2.1 List of Signals Signal name and related reference manual of OSCPRO are changed. - 3.2. Clock Supply The description is changed. - 3.7.2. Oscillation Clock Control Bit of Internal High-speed Oscillator (IHOSC2) The description for the oscillation clock control bit of the internal high-speed oscillator (IHOSC2) is changed. - 3.9. Operation Status of Counter A table is deleted. The description for the counter is changed. - 4.2.6. ***[SIWDxOSCCR]*** (Oscillation Enable Register) The description for <OSCPRO> is changed. Note 2 is changed. - 5. Precaution The description is changed.
3.2	2023-09-15	- Table 2.1 List of Signals Corrected reference manual name for WDTRSTOUT.

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