32-bit RISC microcontroller

TMPM3H Group(1)

Reference Manual
Clock Control and Operation Mode
(CG-M3H(1)-D)

Revision2.1

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TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

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Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 – Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 – It is possible to omit the "0b" when the number of bit can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m: n].
  Example: S [3:0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- "n" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1], [XYZ2], [XYZ3] → [XYZn]***
- "x" substitutes suffix number or character of units and channels in the Register List.
  In case of unit, "x" means A, B, and C . . .
  Example: ***[ADACR0], [ADBCR0], [ADCCR0] →[ADxCR0]***
  In case of channel, "x" means 0, 1, and 2 . . .
  Example: [***T32A0RUNA], [T32A1RUNA], [T32A2RUNA] → [T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit [3:0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> = 0x01 (hexadecimal), ***[XYZn]***<VW> = 1 (binary)
- Word and Byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and Write are possible
- Unless otherwise specified, register access supports only word access.
- The register defined as reserved must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "-" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is "-", follow the definition of each register.
- Reserved bits of the Write-only register should be written with their default value. In the cases that default is "-", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

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Terms and Abbreviations

Some of abbreviations used in this document are as follows:

ADC	Analog to Digital Converter
A-ENC	Advanced Encoder input Circuit
CG	Clock control and Operation Mode
DAC	Digital to Analog Converter
DNF	Digital Noise Filter
ELOSC	External Low speed Oscillator
EHOSC	External High speed Oscillator
fsys	Frequency of SYSTEM Clock
IHOSCx	Internal High speed Oscillator X
INT	Interrupt
I^2C	Inter-Integrated Circuit
I2CS	I^2C wake up circuit from Standby mode
LVD	Voltage Detection Circuit
NMI	Non-Maskable Interrupt
OFD	Oscillation Frequency Detector
PMD+	Programmable Motor Control Circuit Plus
POR	Power On Reset Circuit
RMC	Remote control Signal Preprocessor
RLM	Reset LOSC<Low Power> Manager
SCOUT	Source Clock Output
SIWDT	Clock Selective Watchdog Timer
TPIU	Trace Port Interface Unit
TRGSEL	Trigger Selection circuit
TSPI	Toshiba Serial Peripheral Interface
T32A	32-bit Timer Event counter
UART	Universal Asynchronous Receiver Transmitter

1. Outlines

The clock/mode control block can select a clock gear or prescaler clock and set the warm up of oscillator.

Furthermore, it has Normal mode and a Low Power Consumption mode in order to reduce power consumption using mode transition.

There is the following as a function relevant to a clock.

- System clock controls
- Prescaler clock controls

2. Clock control

2.1. Clock type

This section shows a list of clocks:

EHCLKIN: The clock input from the external
f_{OSC} : A clock generated in the internal oscillation circuit or input from the X1 and X2 pins
f_{PLL} : A clock multiplied by PLL
fc : A clock selected by ***[CGOSCCR]*** <OSCSEL> (high speed clock)
fs : A clock output from an external low speed oscillator
fsys : A system clock selected by ***[CGSYSCR]*** <GEAR[2:0] >
ΦT0 : A clock selected by ***[CGSYSCR]*** <PRCK[3:0] > (prescaler clock)
f_{IHOSC1} : A clock generated with the internal high speed oscillator 1
f_{IHOSC2} : A clock generated with the internal high speed oscillator 2
ADCLK : A conversion clock for AD converters
TRCLKIN : A clock for tracing facilities of a debugging circuit (ETM)

2.2. The initial value by a reset action

A clock setup is initialized by the following states by a reset action.

External high speed oscillator	: Stop
Internal high speed oscillator 1	: Oscillation
Internal high speed oscillator 2	: Stop
External low speed oscillator	: Stop
PLL (multiplying circuit)	: Stop
Gear clock	: fc (no frequency dividing)

2.3. Clock System diagram

The figure below shows a clock system diagram.

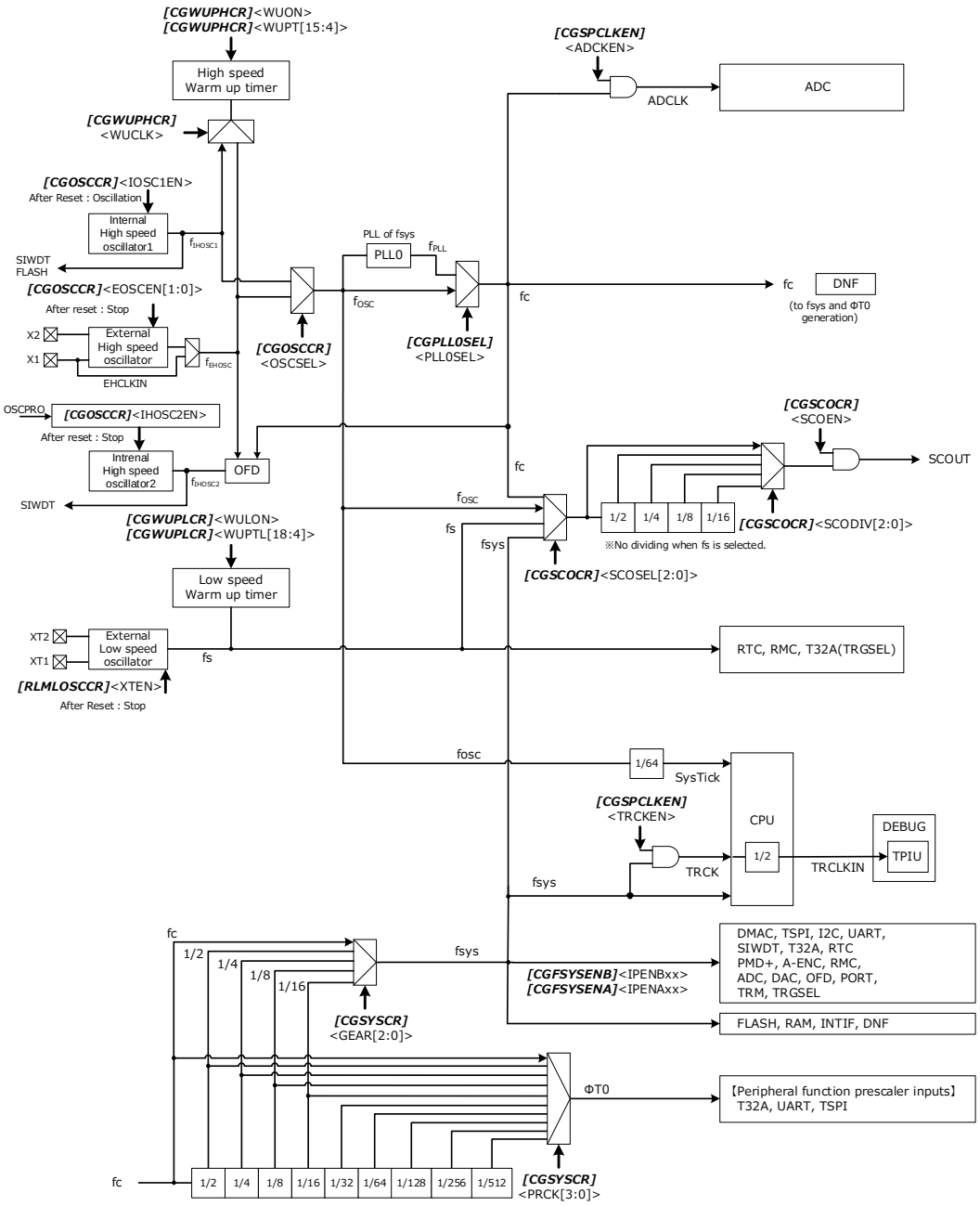

Figure 2.1 Clock system diagram

2.4. Warming up function

A function for a warming up function to secure the oscillation stable time at the time of the STOP1 mode release which starts the warming up counter for high speed oscillation automatically.

It is available also as a count up timer which uses the exclusive warming up counter of high speed oscillator/low speed oscillator for the waiting for the stability of an external oscillator or an internal oscillator.

This chapter explains the setting method to the register for warming up timers, and the case where it is used as a count up timer. The detailed explanation at the time of STOP1 mode release, refers to the "3.3.2. Warming up at the release of Low Power Consumption mode".

2.4.1. The warming up counter for a high speed oscillation

A 16-bit up counter is built in as a warming up counter only for a high speed oscillation. Also, when setting before changing to the STOP1 mode, it computes in the following formula, 4 bits of low ranks are omitted, and it sets to top 12 bits. A register will be set as ***[CGWUPHCR]*** <WUPT [15:4]>. 16 is subtracted in order to perform the count for 4 bits of low ranks, even when a set point is 0.

<Formula>

Warming up counter value (16 bits) = (warming up time (s) / clock period (s)) - 16

(Example) When 5 ms of warming time are set up with 10 MHz (100 ns of clock periods) of oscillators

Warming up counter value (16 bits) = (5ms / 100ns) - 16
= 50000 - 16
= 49984
= 0xC340

Since top 12 bits are set up, it sets to a register as follows.

[CGWUPHCR]<WUPT[15:4]> = 0xC34

In the case of 10 MHz, the Setting range is 0 ≤ <WUPT[15:4]> ≤ 0xFFF, Warming up time is set from 1.6μs to 6.5536ms.

2.4.2. The warming up counter for a low speed oscillation

A 19-bit rise counter is built in as a warming up counter only for a low speed oscillation. It computes in the following formula, 4 bits of low ranks are omitted, and it sets to top 15 bits. A register will be set as ***[CGWUPLCR]*** <WUPTL [18:4]>. 16 is subtracted in order to perform the count for 4 bits of low ranks, even when a set point is 0.

<Formula>

Warming up counter value (19 bits) = (warming up time (s) / clock period (s)) - 16

(Example) When 50 ms of warming time are set up with 32 kHz (clock period 31.25μs) of oscillators

Warming up counter value (19 bits) = (50ms / 31.25μs) - 16
=1600 - 16
=1584
=0x00630

Since top 15 bits are set up, it sets to a register as follows.

[CGWUPLCR]<WUPTL[18:4]> = 0x0063

In the case of 32 kHz, its setting range is 0 ≤ <WUPTL[18:4]> ≤ 0x7FFF, Warming up time is set from 500μs to 16.384s.

2.4.3. The directions for a warming up timer

The directions for a warming up function are explained.

(1) Selection of a clock
In a high speed oscillation, the clock classification (an internal oscillation / external oscillation) counted at a warming up counter is chosen by ***[CGWUPHCR]*** <WUCLK>.

(2) Calculation of a warming up counter set value
The warming up time can set any value to the counter for a high speed oscillation / for a low speed oscillation. Please compute and set up from each formula.

(3) The start of warming up, and a termination confirmation
When software (command) performs the start of warming up, and a termination Confirmation, a warming up count start is carried out by setting "1" to ***[CGWUPHCR]*** <WUON> (or ***[CGWUPLCR]*** <WULON>). Termination is ***[CGWUPHCR]*** <WUEF> (or ***[CGWUPLCR]*** <WULEF>). It distinguishes by becoming "1" to "0". "1" shows the inside of warming up and "0" shows termination. After a counting end, a counter is reset and returns to an initial state.
It does not become forced termination although "0" is written in during a counter operation to ***[CGWUPHCR]*** <WUON> (or ***[CGWUPLCR]*** <WULON>). "0" writing is disregarded.

Note1: Since it is operating with the oscillating clock, a warming up timer includes an error, when Oscillation frequency has fluctuation. Therefore, It serves as time of an outline.

2.5. Clock multiplying circuit (PLL) for fsys

The clock multiplying circuit outputs the f_{PLL} clock (maximum 40 MHz) multiplied by the optimum condition for the frequency (6 MHz to 12 MHz) of the output clock f_{OSC} of the high-speed oscillator.

So, it is possible to make input frequency to an oscillator low and to make an internal clock high speed by this circuit.

2.5.1. A PLL setup after reset release

The PLL is disable after reset release.

In order to use the PLL, set a multiplication value to ***[CGPLL0SEL]***<PPL0SET> while ***[CGPLL0SEL]***<PLL0ON> is "0". Then wait until approximately 100 μs has elapsed as a PLL initial stabilization time, and set "1" to <PLL0ON> to start PLL operation.

After that, to use f_{PLL} clock which is multiplied f_{OSC}, wait until approximately 400 μs has elapsed as a lock up time. Then set "1" to ***[CGPLL0SEL]***<PLL0SEL>.

Note that a warm up time is required until PLL operation becomes stable using the warm up function, etc.

2.5.2. The formula and the example of a set of a PLL multiplication value

The details of the items of ***[CGPLL0SEL]*** <PLL0SET [23:0]> which set up a PLL multiplication value are shown below.

Table 2.1 Details of a *[CGPLL0SEL]* <PLL0SET[23:0]>setup

The items of PLL0SET	Function		
[23:17]	Correction value setup	The quotient of f_{OSC}/450k (integer). For details, refer to the Table 2.2	
[16:14]	f_{OSC} setup	111: 20 < f_{OSC} ≤ 24 (unit: MHz) 011: 10 < f_{OSC} ≤ 20 010: Reserved 001: 6 ≤ f_{OSC} ≤ 10 000: Reserved	
[13:12]	Dividing setup	00: Reserved 01: 2 dividing (x1/2) 10: 4 dividing (x1/4) 11: 8 dividing (x1/8)	
[11:8]	Fraction part Multiplication setup	0000: 0.0000 0001: 0.0625 0010: 0.1250 0011: 0.1875 0100: 0.2500 0101: 0.3125 0110: 0.3750 0111: 0.4375	1000: 0.5000 1001: 0.5625 1010: 0.6250 1011: 0.6875 1100: 0.7500 1101: 0.8125 1110: 0.8750 1111: 0.9375
[7:0]	Integer part Multiplication setup	0x00: 0 0x01: 1 0x02: 2 : 0xFD: 253 0xFE: 254 0xFF: 255	

Note: A multiplication value is the total of <PLL0SET [7:0]> (integer part) and <PLL0SET [11:8]> (fractional part).

f_{PLL} is denoted by the following formulas.

f_{PLL}= f_{OSC} × (***[CGPLL0SEL]*** <PLL0SET[7:0]> + ***[CGPLL0SEL]*** <PLL0SET [11:8]>)×(***[CGPLL0SEL]*** <PLL0SET [13:12]>)

※ (f_{PLL} ≤ Maximum Operating Frequency)

Note1. The absolute value of frequency accuracy is not guaranteed.

Note2. There is no Linearity in the frequency by the Fraction part Multiplication setup.

Table 2.2 PLL correction (example)

f_{OSC} (MHz)	<PLL0SET[23:17]> (A decimal, an integral value)
6.00	14
8.00	18
10.00	23
12.00	27

A PLL correction can be calculated below.
f_{OSC} =6.0MHz, 6.0/0.45=13.33 → 14 ;
A decimal fraction revalues and round up.

The main examples of a setting of ***[CGPLL0SEL]*** <PLL0SET [23:0]> are shown below.

It multiplies by PLL, and dividing is carried out and the target Clock frequency (f_{PLL}) is generated for input frequency (f_{OSC}).

A dividing value is chosen from 1/2, 1/4, and 1/8.
Moreover, set up the frequency after multiplication in the following ranges.
200MHz ≤ (f_{OSC} x multiplication value) ≤ 320MHz

Table 2.3 PLL0SET set points (example)

f_{OSC} (MHz)	Multiplication value	Dividing value	f_{PLL} (MHz)	<PLL0SET[23:0]>
6.00	53.3125	1/8	39.98	0x1C7535
8.00	40.0000	1/8	40.00	0x247028
10.00	32.0000	1/8	40.00	0x2E7020
12.00	26.6250	1/8	39.94	0x36FA1A

2.5.3. Change of the PLL multiplication value under operation

It changes to a setup which sets "0" to ***[CGPLL0SEL]*** <PLL0SEL> first, and does not use a PLL multiplication clock during PLL multiplication clock operation when changing a multiplication value. And ***[CGPLL0SEL]*** <PLL0ST> =0 is read, after checking having changed to a setup which does not use a multiplication clock, ***[CGPLL0SEL]*** <PLL0ON> is set to "0", and PLL is stopped.

Then, the multiplication value of ***[CGPLL0SEL]*** <PLL0SET> is changed, as reset time of PLL, after about 100μs progress, ***[CGPLL0SEL]*** <PLL0ON> is set as "1", and operation of the PLL is started.

Then, ***[CGPLL0SEL]*** <PLL0SEL> is set as "1" after lock up time and about 400μs progress.

Finally, ***[CGPLL0SEL]***<PLL0ST> is read and it checks having changed.

2.5.4. PLL operation start / stop / switching procedure

2.5.4.1. fc setup (PLL stop >>> PLL start)

As an fc setup, the example of switching procedure from the PLL stop state to the PLL operation state is as follows.

<< The state before switching >>	
[CGPLL0SEL]<PLL0ON> = 0	Stops the PLL operation for fsys.
[CGPLL0SEL]<PLL0SEL> = 0	Selects the setting of the PLL for fsys to "PLL is unused (f_{OSC})".
[CGPLL0SEL]<PLL0ST> = 0	Selects the status of the PLL for fsys to "PLL is unused (f_{OSC})".

<< The example of switching procedure >>		
1	***[CGPLL0SEL]*** <PLL0SET> = 0xX	A PLL multiplication value setup is chosen.
2	100 μs or more. It waits.	Latency time after a multiplication setup
3	***[CGPLL0SEL]***<PLL0ON> = 1	PLL operation for fsys is carried out to an oscillation.
4	Wait 400 μs or more.	PLL Output clock stable latency time
5	***[CGPLL0SEL]***<PLL0SEL> = 1	PLL selection for fsys is carried out to PLL use (f_{PLL}).
6	Read ***[CGPLL0SEL]*** <PLL0ST>	It waits until the PLL selection status for fsys becomes PLL use (f_{PLL}) (= 1).

Note: 1 to 4 is unnecessary when the state before switching is ***[CGPLL0SEL]*** <PLL0ON> = 1.
When changing from the state where the PLL Output clock was stabilized, it can change to the conduct PLL state by execution of only 5 and 6.

2.5.4.2. fc setup (PLL operating >>> PLL stop)

As an fc setup, the example of switching procedure from the PLL operation state to a PLL stop state is as follows.

<< The state before switching >>	
[CGPLL0SEL]<PLL0ON> = 1	Sets the PLL oscillation for fsys.
[CGPLL0SEL]<PLL0SEL> = 1	Select the PLL for fsys to "PLL is used (f_{PLL})".
[CGPLL0SEL]<PLL0ST> = 1	Select the status of the PLL for fsys to "PLL is used (f_{PLL})".

<< The example of switching sequence >>		
1	***[CGPLL0SEL]***<PLL0SEL> = 0	Select the PLL for fsys to "PLL is unused (f_{OSC})".
2	***[CGPLL0SEL]*** <PLL0ST> It reads.	Waits until the status of the PLL for fsys becomes "PLL is unused (f_{OSC}) (=0)".
3	***[CGPLL0SEL]***<PLL0ON> =0	Sets the PLL oscillation for fsys to stop.

2.6. System clock

An internal high speed oscillation clock and external high speed oscillation clock (connected oscillator or clock input) can be used as a source of the system clock.

Dividing is possible for a system clock at ***[CGSYSCR]*** <GEAR [2:0]> (clock gear). Although a setup can be changed during operation, after register writing before a clock actually changes, a maximum of 16-clock time is required of fc. Check completion of a clock change by ***[CGSYSCR]*** <GEARST [2:0]>.

Note: Do not change a clock gear during operation of peripheral functions, such as a timer counter.

It is the following about the example of operation frequency by the clock gear ratio (1/1 to 1/16) to the frequency fc set up with an Oscillation frequency, a PLL multiplication value, etc.

Table 2.4 The example of operation frequency (unit: MHz)

External Oscillation (MHz)	External Clock input (MHz)	Built-in oscillation IHOSC1 (MHz)	PLL Multiplication value (After dividing)	Maximum Frequency (fc)(MHz)	Clock gear PLL=ON					Clock gear PLL=OFF				
					1/1	1/2	1/4	1/8	1/16	1/1	1/2	1/4	1/8	1/16
6	6	-	6.625	39.75	39.75	19.9	9.94	4.97	2.48	6	3	1.5	-	-
8	8	-	5	40	40	20	10	5	2.5	8	4	2	1	-
10	10	10	4	40	40	20	10	5	2.5	10	5	2.5	1.25	-
12	12	-	3.3125	39.75	39.75	19.9	9.94	4.97	2.48	12	6	3	1.5	-

2.6.1. The setting method of a system clock

2.6.1.1. f_{OSC} setup (internal oscillation >>> external oscillation)

As a f_{OSC} setup, the example of switching procedure to the external high speed oscillator (EHOSC) from an internal high speed oscillator 1 (IHOSC1) is shown below.

<< The state before switching >>	
[CGOSCCR]<IHOSC1EN> = 1	An internal high speed oscillator 1 oscillates.
[CGOSCCR]<OSCSEL> = 0	The high speed oscillation selection for f_{OSC} is an inside (IHOSC1).
[CGOSCCR]<OSCF> = 0	The high speed oscillation selection status for f_{OSC} is an inside (IHOSC1).
An oscillator is connected to X1 / X2 pin.	

Note: Do not connect except an oscillator

<< The example of switching procedure >>		
1	***[PHPDN]***<bit[1:0]> = 00 ***[PHIE]***<bit[1:0]> = 00	Disable the pull-down of X1 / X2 pin. Disable input control of X1 / X2 pin.
2	***[CGOSCCR]***<EOSCEN[1:0]> = 01	It is an external oscillation (EHOSC) about the selection of an external oscillation of operation.
3	***[CGWUPHCR]***<WUCLK> = 1 ***[CGWUPHCR]*** <WUPT[18:4]> = arbitrary value	It is the external (EHOSC) about high speed oscillation warming up clock selection. Oscillator stable time is set to a warming up counter set value.
4	***[CGWUPHCR]***<WUON> = 1	High speed oscillation warming up is started.
5	***[CGWUPHCR]*** <WUEF> is read.	It waits until it becomes the termination of high speed oscillation warming up (=0).
6	***[CGOSCCR]***<OSCSEL> = 1	It is high speed oscillation selection for f_{OSC} to the exterior (EHOSC).
7	***[CGOSCCR]*** <OSCF> is read.	It waits until the high speed oscillation selection status for f_{OSC} becomes outside (=1).
8	***[CGOSCCR]***<IHOSC1EN> = 0	An internal high speed oscillator 1 is suspended.

2.6.1.2. f_{OSC} setup (internal oscillation >>> external clock input)

As a f_{OSC} setup, the example of switching procedure to the external clock input (EHCLKIN) from an internal high speed oscillator 1(IHOSC1) is shown below.

<< The state before switching >>	
[CGOSCCR]<IHOSC1EN> = 1	An internal high speed oscillator 1 oscillates.
[CGOSCCR]<OSCSEL> = 0	The high speed oscillation selection for f_{OSC} is an inside (IHOSC1).
[CGOSCCR]<OSCF> = 0	The high speed oscillation selection status for f_{OSC} is an inside (IHOSC1).
Clock into to EHCLKIN	Input in the proper voltage ranges.

<< The example of switching procedure >>		
1	***[PHPDN]***<bit[0]> = 0 ***[PHIE]***<bit[0]> = 1	Disable the pull-down of X1 pin. Enable the input control of an X1 / EHCLKIN pin.
2	***[CGOSCCR]***<EOSCEN[1:0]> = 10	Selection of an external oscillation of operation is carried out to an external clock input (EHCLKIN).
3	***[CGOSCCR]***<OSCSEL> = 1	It is high speed oscillation selection for f_{OSC} to an external clock.
4	***[CGOSCCR]*** <OSCF> is read.	It waits until the high speed oscillation selection status for f_{OSC} becomes outside (=1).
5	***[CGOSCCR]***<IHOSC1EN> = 0	An internal high speed oscillator 1 is suspended.

2.6.1.3. f_{OSC} setup (an external oscillation / external clock input >>> internal oscillation)

As a f_{OSC} setup, the example of switching procedure to the internal high speed oscillator (IHOSC1) from an external high speed oscillator (EHOSC) Operation State or an external clock input (EHCLKIN) Operation State is shown below.

<< The state before switching >>	
[CGOSCCR]<EOSCEN[1:0]> = 01 or 10	Selection of an external oscillator of operation is an external oscillator (EHOSC) or external clock input.
[CGOSCCR]<OSCSEL> = 1	The high speed oscillation selection for f_{OSC} is the exterior (EHOSC).
[CGOSCCR]<OSCF> = 1	The high speed oscillation selection status for f_{OSC} is the exterior (EHOSC).

<< The example of switching procedure >>		
1	***[CGOSCCR]***<IHOSC1EN> = 1	An internal high speed oscillator 1 is oscillated.
2	***[CGOSCCR]*** <IHOSC1F> is read.	It waits until an internal high speed oscillation stable flag for IHOSC1F becomes oscillation stability (=1).
3	***[CGOSCCR]***<OSCSEL> = 0	It is a high speed oscillation selection for f_{OSC} to an internal clock (IHOSC1).
4	***[CGOSCCR]*** <OSCF> is read.	It waits until the high speed oscillation selection status for f_{OSC} becomes an inside (=0).
5	***[CGOSCCR]***<EOSCEN[1:0]> = 00	Set the selection of an external oscillator operation to unused.

2.7. Clock supply setting function

This CPU has the clock on/off function for the peripheral circuits. To reduce the power consumption, this CPU can stop supplying the clock to the peripheral functions that are not used.

Except some peripheral functions, clocks are not supplied after reset.

In order to supply the clock of the function to be used, set the bit of relevance of ***[CGFSYSENA]***, ***[CGFSYSENB]***, and ***[CGSPCLKEN]*** to "1".

For details, refer to "4. Explanation of a register".

2.8. The output function of a clock in the terminal

This CPU has the clock output function to the terminal. A low speed clock "fs", High speed oscillation clock "f_{OSC}", high speed clock "fc", system clock "fsys" can be output from the SCOUT pin.

For details, refer to "4.2.5. *[CGSCOCR]* (SCOUT Output control register)".

The below table shows the use propriety state of SCOUT pin in each operation mode.

Table 2.5 List of Use propriety in each operation mode

SCOUT selection	Operation mode		
	NORMAL/IDLE	STOP1	STOP2
f_{OSC}	Yes	N/A	N/A
fc	Yes	N/A	N/A
fs	Yes	Yes	N/A
fsys	Yes	N/A	N/A

2.9. Prescaler clock

Peripheral function each have a Prescaler circuit to divide the ΦT0 clock.

The ΦT0 clock inputted into the prescaler circuit can be divided by the ***[CGSYSCR]***<PRCK[3:0]>.

As for ΦT0 clock after reset, fc is chosen.

After register writing before a clock actually changes, a maximum of 512-clock time is required of fc.

To confirm the completion of the clock changed, check the status of ***[CGSYSCR]***<PRCKST[3:0]>.

Note: Do not change a prescaler clock during operation of peripheral functions, such as a timer counter.

3. Operation mode

There are NORMAL mode and a Low Power Consumption mode (IDLE, STOP1, STOP2) in this product as an Operation mode, and it can reduce power consumption by performing mode changes according to directions for use.

3.1. Details of an Operation mode

3.1.1. The feature in each mode

The feature in NORMAL, Low Power Consumption mode are follows.

- **NORMAL mode**

  They are a CPU core and the mode which operates a peripheral circuit with high frequency clocks. After the reset release serves as NORMAL mode.

The Low Power Consumption modes are the following 3 modes.

- **Low Power Consumption mode**

  – IDLE mode

  It is the mode which CPU stops.

  The peripheral function should perform operation/stop by the register of each peripheral function, a clock supply setting function, etc.

  Note: In IDLE mode ,the CPU cannot perform the clearance of the watchdog timer, it is careful of it.

  – The STOP1 mode

  It is the mode which all the internal circuits also including an internal oscillator stop.

  However, when an external low speed oscillator is oscillated and it shifts to the STOP1 mode, the RTC operates.

  If the STOP1 mode is canceled, an internal high speed oscillator1 (IHOSC1) will start an oscillation, and will return to NORMAL mode.

  Please disable interrupt which is not used for STOP1 release before shifting to the STOP1 mode.

  – The STOP2 mode

  It is the mode which holds a part of the function and cut off an internal electrical power source. STOP1 Consumption of electric power larger than the STOP2 mode can be held down. If the STOP2 mode is released, the power supply will be switched on to the Main power domain, a reset sequence will be performed, and it will return to NORMAL mode.

  As for the Main power domain, it is a function which does not supply a power supply in STOP2 mode.

  Before shifting to the STOP2 mode, STOP2 Forbid interruption which is not made into a release factor,

  Please be sure to set up ***[RLMSHTDNOP]*** <PTKEEP> =1 and to hold the state of each port.

  An Output/Pull up holds, and input permission holds a state when it sets as a port keeping function.

  In addition, external interrupt continues an input.

This product will be cut off the power except for the following circuit in STOP2 mode.

- External low speed oscillator (ELOSC)
- RTC
- Backup RAM
- Port pin status
- LVD
- RLM
- IA
- I^2C Wake up

Regarding a power supply cutoff in the Low Power Consumption mode, for details, refer to the "3.1.4. The peripheral function state in a Low Power Consumption mode".

3.1.2. Low Power Consumption mode

In order to shift to each Low Power Consumption mode, the IDLE/STOP1/STOP2 mode is chosen by standby control register ***[CGSTBYCR]*** <STBY[1:0] >, and a WFI command is executed. When it shifts to a Low Power Consumption mode by WFI command, the restart operation from a Low Power Consumption mode is performed by reset or interrupt generating. To return by an interrupt, it is necessary to set up. Please refer to "Interrupt" chapter of the "Exception" of a reference manual for details.

Note1: This product does not support a return by events; therefore, do not make a transition to low-power consumption mode triggered by WFE (Wait For Event).

Note2: This product does not support low-power consumption mode by SLEEPDEEP of the Cortex-M3 core. Do not use the <SLEEPDEEP> bit of the system control register.

3.1.3. Selection of a Low Power Consumption mode

Low Power Consumption mode selection is chosen by the setup of ***[CGSTBYCR]***<STBY [1:0]>.

Following table shows the mode chosen from a setup of <STBY [1:0]>.

Table 3.1 Low Power Consumption mode selection

Mode	***[CGSTBYCR]***<STBY[1:0]>
IDLE	00
STOP1	01
STOP2	10

Note: Do not use the settings other than the above.

3.1.4. The peripheral function state in a Low Power Consumption mode

The following Table 3.2 shows the Operation State of the peripheral function (block) in each mode.
In addition, after reset release it will be in the state where a clock is not supplied except for a part of blocks.
If needed, set up ***[CGFSYSENA]***, ***[CGFSYSENB]***, and ***[CGSPCLKEN]*** and enable clock supply.

Table 3.2 Block operation status in each Low Power Consumption mode

Block		NORMAL	IDLE	STOP1		STOP2(Note1)	
				ELOSC On	ELOSC Off	ELOSC On	ELOSC Off
Processor core		✓	-	-	-	x	x
DMAC		✓	✓	-	-	x	x
I/O port	Pin state	✓	✓	✓	✓	✓ (Note 4)	✓ (Note 4)
	Register	✓	✓	-	−	x	x
ADC		✓	✓	-	-	x	x
DAC		✓	✓	-	-	x	x
UART		✓	✓	-	-	x	x
I^2C		✓	✓	- (Note 3)	- (Note 3)	x(Note 3)	x(Note 3)
TSPI		✓	✓	-	-	x	x
PMD+		✓	✓	-	-	x	x
A-ENC		✓	✓	-	-	x	x
T32A		✓	✓	-	-	x	x
TRGSEL		✓	✓	-	-	x	x
RTC		✓	✓	✓	-	✓	-
RMC		✓	✓	✓	-	x	x
SIWDT		✓	✓ (Note 2)	-	-	x	x
LVD		✓	✓	✓	✓	✓	✓
OFD		✓	✓	-	-	x	x
TRM		✓	Unavailable	-	-	x	x
CG		✓	✓	✓	✓	x	x
PLL		✓	✓	-	-	x	x
External high speed oscillator (EHOSC)		✓	✓	-	-	x	x
Built-in high speed oscillator 1 (IHOSC1)		✓	✓	-	-	x	x
Built-in high speed oscillator 2 (IHOSC2)		✓	✓	-	-	x	x
External low speed oscillator (ELOSC)		✓	✓	✓	-	✓	-
RLM		✓	✓	✓	✓	✓	✓
Flash Code ROM		Access Possible	Access Possible (Note5)	Data hold	Data hold	Data hold	Data hold
Flash Data ROM							
RAM						x	x
Backup RAM						Data hold	Data hold

✓: operation is possible.

-: if it shifts to the object mode, the clock to a peripheral circuit will stop automatically.

x: If it shifts to the object mode, the electric supply source to a module intercepts automatically. When returning, initialized by the reset.

Note1: Check that the peripheral function is not running and change to STOP 2 mode.

Note2: It's in the protected mode A only. In other case, Stop SIWDT before shifting to the IDLE mode.

Note3: The address match wake up function can only be used.

Note4: A port state when the ***[RLMSHTDNOP]*** <PTKEEP> is set to "1" is held.

Note5: It becomes a data hold when peripheral functions (DMA etc.) except CPU which carry out data access (R/W) are not connected on the bus matrix.

3.2. Mode State Transition

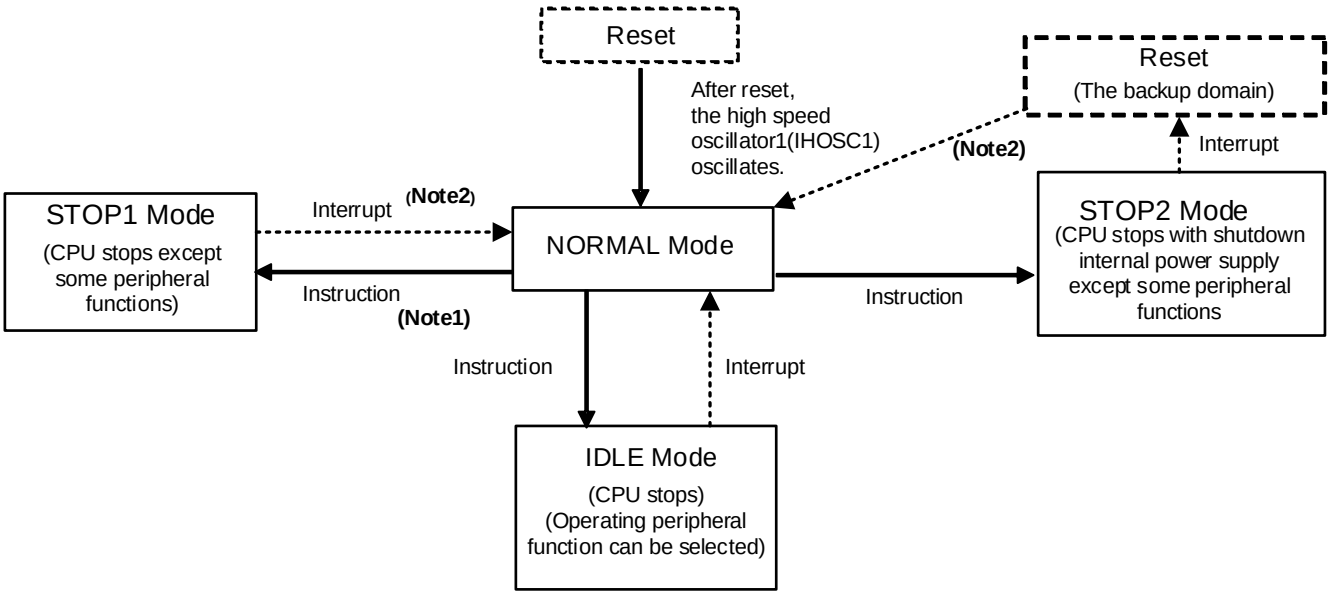

Figure 3.1 Mode State Transition

Note1: Warm up is required at returning. A warm up time must be set in the previous mode (NORMAL mode) before entering to STOP1 mode.

Note2: When the CPU returns from STOP2 mode, the CPU branches to the interrupt service routine triggered by reset. When the CPU returns from STOP1 mode, the CPU branches to the interrupt service routine triggered by interrupt events.

3.2.1. IDLE mode transition flow

Set up the following procedure at switching to IDLE mode.
Because IDLE mode is released by an interrupt, set the interrupt before switching to IDLE mode. For the interrupts that can be used to release the IDLE mode, refer to "3.3.1. The release source of a Low Power Consumption mode". Disable interrupts not used for release and interrupts that cannot be used.

Switching procedure (from Normal mode)		
1	***[SIWDxEN]***<WDTE>=0	Disable SIWDT.
2	***[SIWDxCR]***<WDCR[7:0]>=0xB1	Disable SIWDT.
3	***[FCSR0]*** <RDYBSY> is read.	It waits until Flash will be in a Ready state (=1).
4	***[CGSTBYCR]***<STBY[1:0]>=00	Low Power Consumption mode selection is set to IDLE.
5	***[CGSTBYCR]*** <STBY [1:0]> is read.	Check the 4th line register writing (=00).
6	WFI command execution	Switch to IDLE.

3.2.2. STOP1 mode transition flow

Set up the following procedure at switching to STOP1.

Because STOP1 mode is released by an interrupt, set the interrupt before switching to STOP1 mode. For the interrupts that can be used to release the STOP1 mode, refer to "3.3.1. The release source of a Low Power Consumption mode". Disable interrupts not used for release and interrupts that cannot be used.

Switching procedure (from Normal mode)		
1	***[SIWDxEN]***<WDTE>=0	Disable SIWDT.
2	***[SIWDxCR]***<WDCR[7:0]>=0xB1	Disable SIWDT.
3	***[FCSR0]*** <RDYBSY> is read	It waits until Flash will be in a Ready state (=1).
4	***[CGWUPHCR]*** <WUEF> is read.	It waits until it becomes the termination of high speed oscillation warming up (=0).
5	***[CGWUPHCR]***<WUCLK>=0	High speed oscillation warming up clock selection is made into an inside (IHOSC1).
	[CGWUPHCR] <WUPT[15:4]> =" arbitrary value "	A high speed oscillation warming up counter set value is set as the time required for STOP1 restart operation.
6	***[CGSTBYCR]***<STBY[1:0]>=01	Low Power Consumption mode selection is set to STOP1.
7	***[CGPLL0SEL]***<PLL0SEL>=0	Set PLL of fsys to f_{OSC} (= PLL no use)
8	***[CGPLL0SEL]*** <PLL0ST> is read.	Wait for the PLL status of fsys until off state (=0).
9	***[CGPLL0SEL]***<PLL0ON>=0	Stop PLL for fsys
10	***[CGOSCCR]***<IHOSC1EN>=1	Enable the internal high speed oscillator 1.
11	***[CGOSCCR]***<OSCSEL>=0	High speed oscillation selection for f_{OSC} is made into an inside (IHOSC1).
12	***[CGOSCCR]*** <OSCF> is read.	It waits until the high speed oscillation selection status for f_{OSC} becomes an inside (IHOSC1) (=0).
13	***[CGOSCCR]***<EOSCEN[1:0]>=00	Selection of an external oscillation of operation is unused.
14	***[CGOSCCR]***<IHOSC2EN>=0	The internal high speed oscillator 2 for OFD (IHOSC2) is stopped.
15	***[CGOSCCR]*** <EOSCEN [1:0]> is read.	The register writing of above 13th is checked (=00).
16	***[CGOSCCR]*** <IHOSC2F> is read.	Wait for the status flag of IHOSC2 of OFD until off "0"
17	WFI command execution	Switch to STOP1.

Note: When using the A mode of SIWDT, 1,2,14 and 16 steps are not required.

3.2.3. STOP2 mode transition flow

Set up the following procedure at switching to STOP2.

Because STOP2 mode is released by an interrupt, set the interrupt before switching to STOP2 mode. For the interrupts that can be used to release the STOP2 mode, refer to "3.3.1. The release source of a Low Power Consumption mode". Disable interrupts not used for release and interrupts that cannot be used.

Switching procedure (from Normal mode)		
1	***[SIWDxEN]***<WDTE>=0	Disable SIWDT.
2	***[SIWDxCR]***<WDCR[7:0]>=0xB1	Disable SIWDT.
3	***[FCSR0]*** <RDYBSY> is read.	It waits until Flash will be in a Ready state (=1).
4	***[RLMSHTDNOP]***<PTKEEP>=1	The IO control signal is made to hold.
5	***[CGSTBYCR]***<STBY[1:0]>=10	Low Power Consumption mode selection is set to STOP2.
6	***[CGPLL0SEL]***<PLL0SEL>=0	The PLL selection for fsys is set to PLL unused (f_{OSC})
7	***[CGPLL0SEL]*** <PLL0ST> is read	It waits until the PLL selection status for fsys is PLL un-using it. (=0).
8	***[CGPLL0SEL]***<PLL0ON>=0	Stop PLL for fsys.
9	***[CGOSCCR]***<IHOSC1EN>=1	Enable the internal high speed oscillator.
10	***[CGOSCCR]***<OSCSEL>=0	High speed oscillation selection for f_{OSC} is set to the inside (IHOSC1).
11	***[CGOSCCR]*** <OSCF> is read	It waits until the high speed oscillation selection status for f_{OSC} becomes zero (IHOSC1) (=0).
12	***[CGOSCCR]***<EOSCEN[1:0]>=00	Selection of an external oscillation of operation is set to stop.
13	***[CGOSCCR]***<IHOSC2EN>=0	The internal high speed oscillator2 for OFD is suspended.
14	***[CGOSCCR]*** <EOSCEN [1:0]> is read.	The register writing of 12 is checked (=00).
15	***[CGOSCCR]*** <IHOSC2F> is read.	It waits until the internal oscillation stable flag for IHOSC2 become zero.
16	***[RLMRSTFLG0]***<STOP2RSTF>=0 ***[RLMRSTFLG0]***< PINRSTF>=0	A STOP2 reset flag / reset pin flag is cleared (Note1).
17	WFI command execution	Switch to STOP2.
18	Jump instruction	Return to 17.

Note1: Refer to the "Exception" of a reference manual for a reset flag register ***[RLMRSTFLG0].***

Note2: When using the A mode of SIWDT, 1,2,13 and 15 steps are not required.

3.3. The return operation from a Low Power Consumption mode

3.3.1. The release source of a Low Power Consumption mode

Interruption, Non-Maskable Interrupt, and reset can perform release from a Low Power Consumption mode. The standby release source which can be used is decided by a Low Power Consumption mode.

It shows the following table about details.

Table 3.3 Release source list

Low Power Consumption mode			IDLE	STOP1	STOP2
Release Source	Interruption	INT00, INT01, INT02 (Note1)	✓	✓	✓
		INT03 to INT15 (Note1)	✓	✓	×
		INTI2CWUP	✓	✓	✓
		INTRTC	✓	✓	✓
		INTEMG0, INTOVV0, INTPMD0	✓	×	×
		INTENC00, INTENC01	✓	×	×
		INTADAPDA, INTADAPDB	✓	×	×
		INTADACP0, INTADACP1,INTADATRG	✓	×	×
		INTADASGL, INTADACNT	✓	×	×
		INTTxRX, INTTxTX, INTTxERR	✓	×	×
		INTI2Cx, INTI2CxAL, INTI2CxBF, INTI2CxNA	✓	×	×
		INTUARTxRX, INTUARTxTX, INTUARTxERR	✓	×	×
		INTT32AxA, INTT32AxACAP0, INTT32AxACAP1 INTT32AxB, INTT32AxBCAP0, INTT32BxBCAP1 INTT32AxC, INTT32AxCCAP0, INTT32CxCCAP1	✓	×	×
		INTDMAATC, INTDMAAERR	✓	×	×
		INTRMC	✓	✓	×
		INTFLCRDY,INTFLDRDY	✓	×	×
	SysTick interrupt		✓	×	×
	Non-Maskable interrupt (INTWDT)		✓ (Note2)	×	×
	Non-Maskable interrupt (INTLVD)		✓	✓	✓
	Reset (SIWDT)		✓ (Note2)	×	×
	Reset (LVD)		✓	✓	✓
	Reset (OFD)		✓	×	×
	Reset (RESET_N pin)		✓	✓	✓

✓: After release, an interrupt processing will start.

×: It cannot be used for release.

Note1: INT00 to INT15(External Interrupt 00 to 15) can select one of falling edge, rising edge and level. For details, please refer to “Exception” of reference manual.

Note2: It’s in the protected mode A only. In other case, Stop SIWDT before shift to IDLE mode.

- Released by an interrupt request

  When an interrupt cancels a Low Power Consumption mode, it is necessary to prepare so that interrupt may be detected by the CPU. The interrupt used for release in STOP1 and the STOP2 mode needs to interrupt by INTIF other than a setup of CPU, and needs to set up detection.

- Released by Non-Maskable Interrupt (NMI)

  The factor of NMIs are WDT interrupt (INTWDT, protected mode A only) and LVD interrupt (INTLVD).

- Released by reset

  The reset can perform release from all the Low Power Consumption modes.
  When released by reset, all the registers will be initialized in NORMAL mode after release.

- Released by SysTick interrupt

  SysTick interrupt is available only in IDLE mode.

Refer to "Interrupt" chapter of a reference manual of "Exception" about the details of interrupt.

3.3.2. Warming up at the release of Low Power Consumption mode

Warming up may be required because of the stability of an internal oscillator at the time of mode transition.

When moving from STOP1 mode to a NORMAL mode, an internal oscillation is chosen automatically and the warming up counter is started. The Output of a system clock is started after warming up time progress.

For this reason, before executing the command which moves to the STOP1 mode, set up warming up time by ***[CGWUPHCR]***<WUPT[15:4]>. For the setting method, refer to the "2.4.1. The warming up counter for a high speed oscillation".

The following table shows the existence of a warming up setup at the time of each Operation mode transition.

Table 3.4 Warming up

Operation mode transition	Warming up setup
NORMAL → IDLE	Not required
NORMAL → STOP1	Not required
NORMAL → STOP2	Not required
IDLE → NORMAL	Not required
STOP1 → NORMAL	Required
STOP2 → NORMAL	Not required

3.3.3. The restart operation from the STOP2 mode

The restart operation flow from STOP2 mode release factor interrupt generating is as follows.

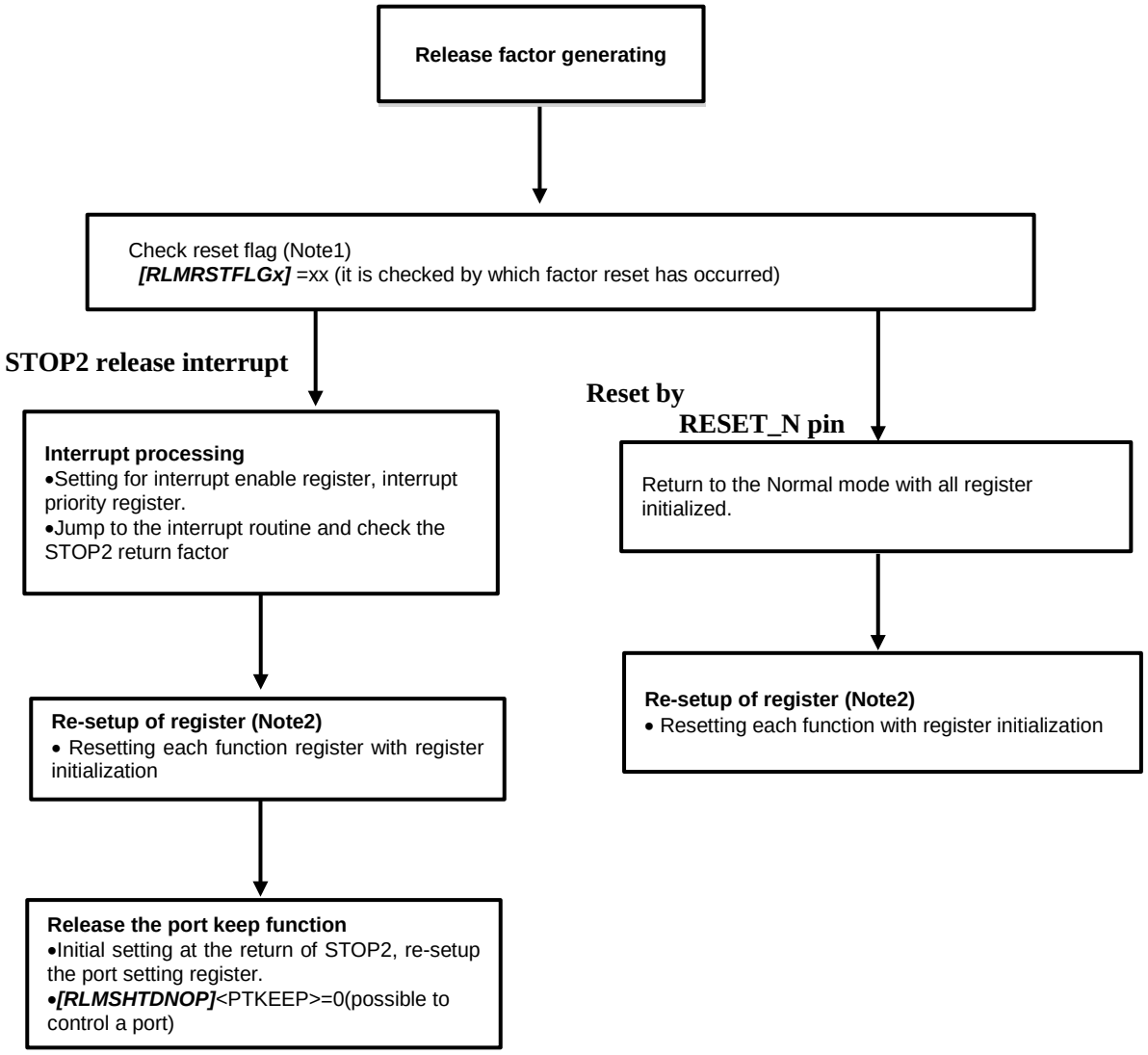

Figure 3.2 STOP2 mode restart the operation flow

Note1: When STOP2 released by a reset pin, as for a reset flag, both "STOP2 reset flag" and "reset pin flag" are materialized.

Note2: Register reset area in STOP2 Release differs by the case of an interrupt and a reset pin. Refer to the reference manual "Power Supply and Reset Operation " for the details of each reset area.

3.4. Clock operation by mode transition

The clock operation in case of mode transition is shown below.

3.4.1. NORMAL >>> IDLE >>> NORMAL Operation mode transition

The CPU stops at IDLE mode. The clock supply to a peripheral function holds a setting state. Please perform the operation/stop by the register of each peripheral function, a clock supply setting function, etc., If needed. Execution of Warming up operation is not performed at the time of the restart operation in NORMAL mode from IDLE state.

After the command (WFI) execution which switches to IDLE mode, a program counter will show the next point and will be in a CPU idle state. With a release source, it becomes a CPU reboot and, in the case of an enable interrupt state, the shift to the next point by transition command (WFI) will be done, after the interrupt processing by release source.

3.4.2. NORMAL >>> STOP1 >>> NORMAL Operation mode transition

When returning to NORMAL mode from the STOP1 mode, warming up is started automatically.

Please set warming up time (24μs, Min) to ***[CGWUPHCR]*** <WUPT [15:4]> before moving to the STOP1 mode.

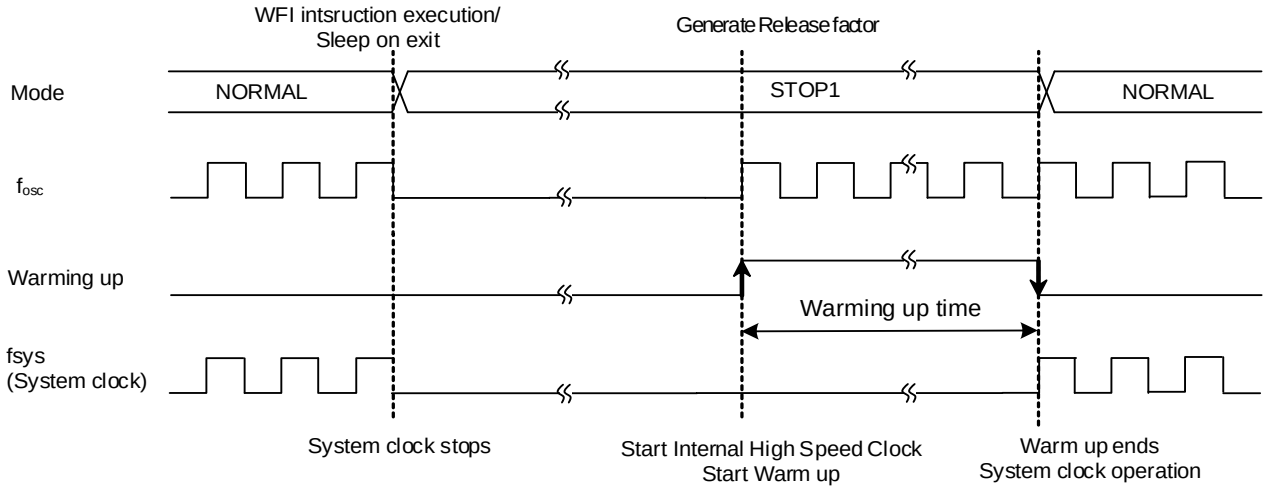

Figure 3.3 NORMAL >>> STOP1 >>> NORMAL Operation mode transition

3.4.3. NORMAL >>> STOP2 >>> RESET >>> NORMAL Operation mode transition

Warming up is not performed when returning to NORMAL mode by reset.

Even when returning to NORMAL mode except for RESET, it branches to the interrupt routine of reset.

A reset operation is performed to an internal Main power domain after STOP2 mode released. However, RESET is not performed to the Backup domain which is keeping power supply.

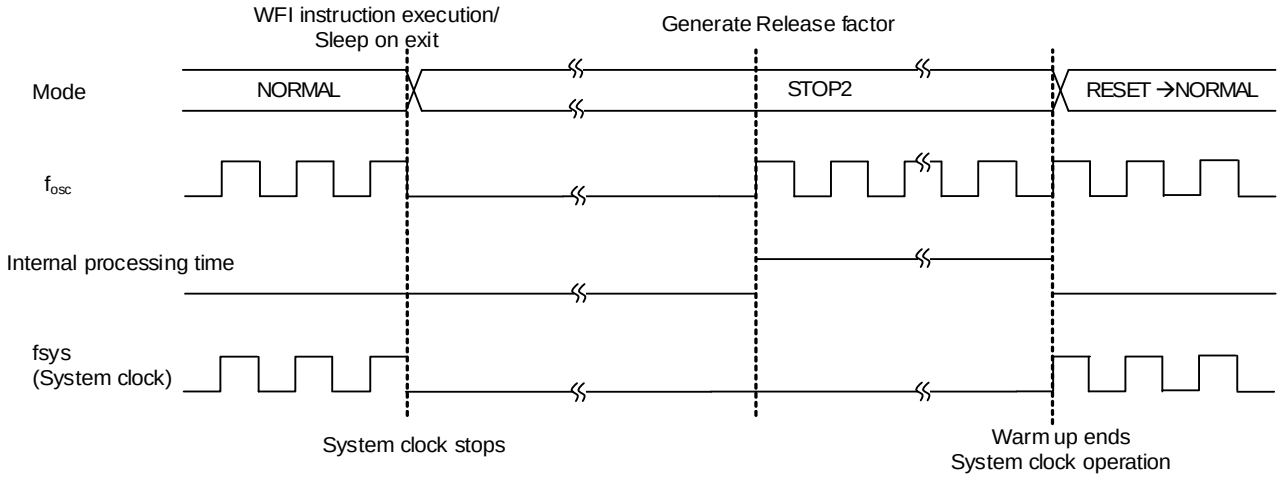

Figure 3.4 NORMAL >>> STOP2 >>> RESET >>> NORMAL Operation mode transition

4. Explanation of a register

4.1. Register list

The register related to CG and its address information is shown below.

Function		Channel/unit	Base address
Clock Control and operation mode	**CG**	-	0x400F3000
A low speed oscillation / power control	**RLM**	-	0x4003E400

A Clock and mode control

Register name		Address (Base+)
CG write protection register	***[CGPROTECT]***	0x0000
Oscillation control register	***[CGOSCCR]***	0x0004
System clock control register	***[CGSYSCR]***	0x0008
Standby control register	***[CGSTBYCR]***	0x000C
SCOUT output control register	***[CGSCOCR]***	0x0010
PLL select register for fsys	***[CGPLL0SEL]***	0x0020
High speed oscillation warming up register	***[CGWUPHCR]***	0x0030
Low speed oscillation warming up register	***[CGWUPLCR]***	0x0034
Clock supply and stop register A for fsys	***[CGFSYSENA]***	0x0050
Clock supply and stop register B for fsys	***[CGFSYSENB]***	0x0054
Clock supply for ADC and Trace Register	***[CGSPCLKEN]***	0x005C
Reserved	-	0x0060

Low speed oscillation / power control(Note)

Register name		Address (Base+)
Low speed oscillation control register	***[RLMLOSCCR]***	0x0000
Power supply cut off control register	***[RLMSHTDNOP]***	0x0001
RLM write protection register	***[RLMPROTECT]***	0x000F

Note: Byte accessible registers. Bit band access cannot be performed.

4.2. Register description

4.2.1. *[CGPROTECT]* (CG write protection register)

Bit	Bit Symbol	After reset	Type	Function
31:8	-	0	R	Read as “0”.
7:0	PROTECT[7:0]	0xC1	R/W	Control write protection for the CG register (all registers included except this register) 0xC1: CG Registers are write enabled. (No Protection) Other than 0xC1: Sets write protection (Protect enable)

4.2.2. *[CGOSCCR]* (oscillation control register)

Bit	Bit Symbol	After reset	Type	Function
31:20	-	0	R	Read as "0".
19	IHOSC2F	0	R	Indicates the stability flag of internal oscillation for IHOSC2. 0: Stopping or being in warm up 1: Stable oscillation
18:17	-	0	R	Read as "0".
16	IHOSC1F	1	R	Indicates the stability flag of internal oscillation for IHOSC1. 0: Stopping or being in warm up 1: Stable oscillation
15:10	-	0	R	Read as "0".
9	OSCF	0	R	Indicates a high speed oscillator for f_{OSC} selection status. 0: Internal high speed oscillator 1 (IHOSC1) 1: External high speed oscillator (EHOSC)
8	OSCSEL	0	R/W	Selects a high speed oscillation for f_{OSC}. (Note 1) 0: Internal high speed oscillator 1 (IHOSC1) 1: External high speed oscillator (EHOSC)
7:4	-	0	R	Read as "0".
3	IHOSC2EN	0	R/W	Enables the internal high speed oscillator 2 for OFD (IHOSC2).(Note 2) 0: Stop 1: Oscillation
2:1	EOSCEN[1:0]	00	R/W	Selects the operation of the external high speed oscillator. (EHOSC) (Note 3) 00: External oscillator is not used. 01: Uses the external high speed oscillator. (EHOSC) 10: Uses the external clock. (EHCLKIN). 11: Reserved
0	IHOSC1EN	1	R/W	Internal high speed oscillator 1 (IHOSC1) 0: Stop 1: Oscillation

Note1: When the setting is modified, confirm whether the written value has been reflected to the ***[CGOSCCR]***<OSCF> bit before executing the next operation.

Note2: Setting cannot be changed, when it is ***[SIWDxOSCCR]***<OSCPRO>=1 (write protection of SIWDT is effective).

Note3: When an external high speed clock (oscillator connection) is used, set “01” to this bit.

4.2.3. *[CGSYSCR]* (system clock control register)

Bit	Bit Symbol	After reset	Type	Function
31:28	-	0	R	Read as "0".
27:24	PRCKST[3:0]	0000	R	Indicates a prescaler clock (ΦT0) selection. 0000: fc 0100: fc/16 1000: fc/256 0001: fc/2 0101: fc/32 1001: fc/512 0010: fc/4 0110: fc/64 1010 to 1111: Reserved 0011: fc/8 0111: fc/128
23:19	-	0	R	Read as "0".
18:16	GEARST[2:0]	000	R	Indicates selection status of the gear ratio of the system clock (fsys). 000: fc 100: fc/16 001: fc/2 101 to 111: Reserved 010: fc/4 011: fc/8
15:12	-	0	R	Read as "0".
11:8	PRCK[3:0]	0000	R/W	Selects a prescaler clock (ΦT0). 0000: fc 0100: fc/16 1000: fc/256 0001: fc/2 0101: fc/32 1001: fc/512 0010: fc/4 0110: fc/64 1010 to 1111: Reserved 0011: fc/8 0111: fc/128 Selects a prescaler clock for the peripheral functions.
7:3	-	0	R	Read as "0".
2:0	GEAR[2:0]	000	R/W	Selects a gear ratio of the system clock (fsys). 000: fc 100: fc/16 001: fc/2 101 to 111: Reserved 010: fc/4 011: fc/8

4.2.4. *[CGSTBYCR]* (standby control register)

Bit	Bit Symbol	After reset	Type	Function
31:2	-	0	R	Read as "0".
1:0	STBY[1:0]	00	R/W	Selects a Low Power Consumption mode. 00: IDLE 01: STOP1 10: STOP2 11: Reserved

4.2.5. *[CGSCOCR]* (SCOUT Output control register)

Bit	Bit Symbol	After reset	Type	Function
31:7	-	0	R	Read as "0".
6:4	SCODIV[2:0]	000	R/W	Selects a SCOUT division ratio. (Note1)(Note2) 000: No dividing 100: Divide by 16 001: Divide by 2 101 to 111: Reserved 010: Divide by 4 011: Divide by 8
3:1	SCOSEL[2:0]	000	R/W	SCOUT base clock selection (Note1) 000:f_{OSC} 100 to 111:Reserved 001:fc 010:fs 011:fsys
0	SCOEN	0	R/W	Enable SCOUT output. 0: Disable 1: Enable

Note1: When the "011: fsys" is selected by <SCOSEL [2:0]>, Selection of the “000: No dividing” by <SCODIV[2:0]> is inhibit.

Note2: When the “010: fs” is selected by <SCOSEL[2:0]>, it force selection that is without clock dividing.

4.2.6. *[CGPLL0SEL]* (PLL selection register for fsys)

Bit	Bit Symbol	After reset	Type	Function
31:8	PLL0SET[23:0]	0x000000	R/W	PLL multiplication setup About a multiplication setup, refer to the “2.5.2. The formula and the example of a set of a PLL multiplication value”
7:3	-	0	R	Read as "0".
2	PLL0ST	0	R	Indicates PLL for fsys selection status. 0: f_{OSC} 1: f_{PLL}
1	PLL0SEL	0	R/W	Indicates Clock selection for fsys 0: f_{OSC} 1: f_{PLL}
0	PLL0ON	0	R/W	Indicates PLL operation for fsys 0: Stop 1: Oscillation

4.2.7. *[CGWUPHCR]* (high speed oscillation warming up register)

Bit	Bit Symbol	After reset	Type	Function
31:20	WUPT[15:4]	0x800	R/W	Sets the upper 12 bits of the 16 bits of calculated values of the warm up timer. About a setup of a warming up timer, refer to the “2.4.1. The warming up counter for a high speed oscillation”
19:16	WUPT[3:0]	0000	R	Sets the lower 4 bits of the 16 bits of calculated values of the warm up timer. It is fixed by “0000”.
15:9	-	0	R	Read as "0".
8	WUCLK	0	R/W	Warming up clock selection (Note1) 0: Built-in high speed oscillator (IHOSC1) 1: External high speed oscillator (EHOSC)
7:2	-	0	R	Read as "0".
1	WUEF	0	R	Indicates the status of the Warming up timer.(Note2) 0: The end of Warming up 1: In warming up operation
0	WUON	0	W	Control the Warming up timer. 0: don't care 1: Warming up operation start.

Note1: Use the internal oscillator for warm up when the CPU returns from the STOP1 mode. Do not use an external oscillator when the CPU returns from the STOP1 mode.

Note2: Do not modify the registers during the warm up (<WUEF>=1). Set the registers when <WUEF>=0.

4.2.8. *[CGWUPLCR]* (low speed oscillation warming up register)

Bit	Bit Symbol	After reset	Type	Function
31:27	-	0	R	Read as "0".
26:12	WUPTL[18:4]	0x4000	R/W	Sets the upper 15 bits of 19 bits of calculated values of the warm up timer. About a setup of a warming up timer, refer to the “2.4.2. The warming up counter for a low speed oscillation “.
11:8	WUPTL[3:0]	0000	R	Sets the lower 4 bits of the 19 bits of calculated values of the warm up timer. It is fixed by “0000”.
7:2	-	0	R	Read as "0".
1	WULEF	0	R	Indicates a status of the Warming up timer (Note1) 0: The end of Warming up 1: In warming up operation
0	WULON	0	W	Control the Warming up timer control 0: don't care. 1: Warming up operation start.

Note1: Do not modify the registers during the warm up (<WULEF>=1). Set the registers when <WULEF>=0.

4.2.9. *[CGFSYSENA]* (Clock supply and stop register A for fsys)

Bit	Bit Symbol	After reset	Type	Function
31	IPENA31	0	R/W	Clock enable of T32A ch5 0: Clock stop 1: Clock supply
30	IPENA30	0	R/W	Clock enable of T32A ch4 0: Clock stop 1: Clock supply
29	IPENA29	0	R/W	Clock enable of T32A ch3 0: Clock stop 1: Clock supply
28	IPENA28	0	R/W	Clock enable of T32A ch2 0: Clock stop 1: Clock supply
27	IPENA27	0	R/W	Clock enable of T32A ch1 0: Clock stop 1: Clock supply
26	IPENA26	0	R/W	Clock enable of T32A ch0 0: Clock stop 1: Clock supply
25	IPENA25	0	R/W	Clock enable of UART ch2 0: Clock stop 1: Clock supply
24	IPENA24	0	R/W	Clock enable of UART ch1 0: Clock stop 1: Clock supply
23	IPENA23	0	R/W	Clock enable of UART ch0 0: Clock stop 1: Clock supply
22	IPENA22	0	R/W	Clock enable of I^2C ch2 0: Clock stop 1: Clock supply
21	IPENA21	0	R/W	Clock enable of I^2C ch1 0: Clock stop 1: Clock supply
20	IPENA20	0	R/W	Clock enable of I^2C ch0 0: Clock stop 1: Clock supply
19	IPENA19	0	R/W	Clock enable of TSPI ch1 0: Clock stop 1: Clock supply
18	IPENA18	0	R/W	Clock enable of TSPI ch0 0: Clock stop 1: Clock supply
17	IPENA17	0	R/W	Clock enable of A-ENC ch0 0: Clock stop 1: Clock supply
16	IPENA16	0	R/W	Clock enable of PMD+ ch0 0: Clock stop 1: Clock supply
15	IPENA15	0	R/W	Clock enable of DMAC Unit A 0: Clock stop 1: Clock supply
14	IPENA14	0	R/W	Clock enable of PORT R 0: Clock stop 1: Clock supply
13	IPENA13	0	R/W	Clock enable of PORT P 0: Clock stop 1: Clock supply

12	IPENA12	0	R/W	Clock enable of PORT N 0: Clock stop 1: Clock supply
11	IPENA11	0	R/W	Clock enable of PORT M 0: Clock stop 1: Clock supply
10	IPENA10	0	R/W	Clock enable of PORT L 0: Clock stop 1: Clock supply
9	IPENA09	0	R/W	Clock enable of PORT K 0: Clock stop 1: Clock supply
8	IPENA08	0	R/W	Clock enable of PORT J 0: Clock stop 1: Clock supply
7	IPENA07	0	R/W	Clock enable of PORT H 0: Clock stop 1: Clock supply
6	IPENA06	0	R/W	Clock enable of PORT G 0: Clock stop 1: Clock supply
5	IPENA05	0	R/W	Clock enable of PORT F 0: Clock stop 1: Clock supply
4	IPENA04	0	R/W	Clock enable of PORT E 0: Clock stop 1: Clock supply
3	IPENA03	0	R/W	Clock enable of PORT D 0: Clock stop 1: Clock supply
2	IPENA02	0	R/W	Clock enable of PORT C 0: Clock stop 1: Clock supply
1	IPENA01	0	R/W	Clock enable of PORT B 0: Clock stop 1: Clock supply
0	IPENA00	0	R/W	Clock enable of PORT A 0: Clock stop 1: Clock supply

Note1: Even if the initial value of a register is set to stop of the clock, the clock is supplied to the register during the reset.

Note2: Write “0” for bit of function that does not exist in TMPM3H5,TMPM3H4,TMPM3H3,TMPM3H2, TMPM3H1 and TMPM3H0. For details, refer to "5. Information according to product".

4.2.10. *[CGFSYSENB]* (Clock supply and stop register B for fsys)

Bit	Bit Symbol	After reset	Type	Function
31	IPENB31	1	R/W	Clock enable of SIWDT 0: Clock stop 1: Clock supply
30	IPENB30	1	R/W	Write as “1”
29	IPENB29	1	R/W	Write as “1”
28	IPENB28	1	R/W	Write as “1”
27	IPENB27	0	R/W	Write as “0”
26	IPENB26	0	R/W	Write as “0”
25	IPENB25	0	R/W	Write as “0”
24	IPENB24	0	R/W	Write as “0”
23	IPENB23	0	R/W	Write as “0”
22	IPENB22	0	R/W	Write as “0”
21	IPENB21	0	R/W	Write as “0”
20	IPENB20	0	R/W	Write as “0”
19	IPENB19	0	R/W	Write as “0”
18	IPENB18	0	R/W	Write as “0”
17	IPENB17	0	R/W	Write as “0”
16	IPENB16	0	R/W	Write as “0”
15	IPENB15	0	R/W	Write as “0”
14	IPENB14	0	R/W	Write as “0”
13	IPENB13	0	R/W	Write as “0”
12	IPENB12	0	R/W	Write as “0”
11	IPENB11	0	R/W	Write as “0”
10	IPENB10	0	R/W	Write as “0”
9	IPENB09	0	R/W	Write as “0”
8	IPENB08	0	R/W	Write as “0”
7	IPENB07	0	R/W	Clock enable of TRGSEL 0: Clock stop 1: Clock supply
6	IPENB06	0	R/W	Clock enable of TRM 0: Clock stop 1: Clock supply
5	IPENB05	0	R/W	Clock enable of OFD 0: Clock stop 1: Clock supply
4	IPENB04	0	R/W	Clock enable of RMC ch0 0: Clock stop 1: Clock supply
3	IPENB03	0	R/W	Clock enable of RTC 0: Clock stop 1: Clock supply
2	IPENB02	0	R/W	Clock enable of DAC ch1 0: Clock stop 1: Clock supply
1	IPENB01	0	R/W	Clock enable of DAC ch0 0: Clock stop 1: Clock supply
0	IPENB00	0	R/W	Clock enable of ADC Unit A 0: Clock stop 1: Clock supply

Note1: Even if the initial value of a register is set to stop of the clock, the clock is supplied to the register during the reset.

Note2: Write “0” for bit of function that does not exist in TMPM3H5,TMPM3H4,TMPM3H3,TMPM3H2, TMPM3H1 and TMPM3H0. For details, refer to "5. Information according to product".

4.2.11. *[CGSPCLKEN]* (Clock Supply and stop register for ADC and Trace)

Bit	Bit Symbol	After reset	Type	Function
31:17	-	0	R	Read as "0".
16	ADCKEN	0	R/W	Enable the clock for ADC. 0: Clock stop 1: Clock supply
15:1	-	0	R	Read as "0".
0	TRCKEN	0	R/W	Clock Enable of the Debug circuit (Trace/SWV). 0: Clock stop 1: Clock supply

4.2.12. *[RLMLOSCCR]* (low speed oscillation control register)

Bit	Bit Symbol	After reset	Type	Function
7:2	-	0	R	Read as "0".
1	-	0	R/W	Write as "0".
0	XTEN	0	R/W	Selection of an external low speed oscillator of operation 0: Stop 1: Oscillation

Note1: It is initialized only by a Power On Reset.

Note2: It is a register accessed per byte. Bit band access is not allowed.

Note3: When you rewrite, please read the register and check rewriting.

4.2.13. *[RLMSHTDNOP]* (power supply cut off control register)

Bit	Bit Symbol	After reset	Type	Function
7:1	-	0	R	Read as "0".
0	PTKEEP	0	R/W	The I/O control signal in the STOP2 mode is held. 0: Control by Port 1: Hold the state when it changes into 1 from 0. A setup is required in front at the time of STOP2 mode changes.

Note1: It is a register accessed per byte. Bit band access is not allowed.

Note2: When you rewrite, please read the register and check rewriting.

4.2.14. *[RLMPROTECT]* (RLM write protection register)

Bit	Bit Symbol	After reset	Type	Function
7:0	PROTECT	0xC1	R/W	RLM register write protection control 0xC1: Write enable to an RLM register (protection release) except 0xC1: Write disable to an RLM register (protection effective) The writing to ***[RLMLOSCCR]*** and the ***[RLMSHTDNOP]*** register. It becomes impossible.

Note1: It is a register accessed per byte. Bit band access is not allowed.

Note2: When you rewrite, please read the register and check rewriting.

5. Information according to product

The information about CG which is different according to each product is shown below.

5.1. *[CGFSYSENA]*

Table 5.1 *[CGFSYSENA]* per product allocation

Bit	Bit Symbol	Connection destination	Channel number/ Unit name/ I/O port name	M3H6	M3H5	M3H4	M3H3	M3H2	M3H1	M3H0
31	IPENA31	T32A	5	✓	✓	✓	✓	✓	✓	✓
30	IPENA30		4	✓	✓	✓	✓	✓	✓	✓
29	IPENA29		3	✓	✓	✓	✓	✓	✓	✓
28	IPENA28		2	✓	✓	✓	✓	✓	✓	✓
27	IPENA27		1	✓	✓	✓	✓	✓	✓	✓
26	IPENA26		0	✓	✓	✓	✓	✓	✓	✓
25	IPENA25	UART	2	✓	✓	✓	✓	✓	✓	-
24	IPENA24		1	✓	✓	✓	✓	✓	✓	✓
23	IPENA23		0	✓	✓	✓	✓	✓	✓	✓
22	IPENA22	I^2C	2	✓	✓	✓	✓	-	-	-
21	IPENA21		1	✓	✓	✓	✓	✓	✓	-
20	IPENA20		0	✓	✓	✓	✓	✓	✓	✓
19	IPENA19	TSPI	1	✓	✓	✓	✓	✓	✓	-
18	IPENA18		0	✓	✓	✓	✓	✓	✓	✓
17	IPENA17	A-ENC	0	✓	✓	✓	✓	✓	✓	✓
16	IPENA16	PMD+	0	✓	✓	✓	✓	✓	✓	✓
15	IPENA15	DMAC	A	✓	✓	✓	✓	✓	✓	✓
14	IPENA14	PORT	R	✓	-	-	-	-	-	-
13	IPENA13		P	✓	✓	-	-	-	-	-
12	IPENA12		N	✓	✓	✓	-	-	-	-
11	IPENA11		M	✓	✓	✓	-	-	-	-
10	IPENA10		L	✓	✓	✓	✓	-	-	-
9	IPENA09		K	✓	✓	✓	✓	✓	✓	✓
8	IPENA08		J	✓	✓	✓	✓	✓	✓	✓
7	IPENA07		H	✓	✓	✓	✓	✓	✓	✓
6	IPENA06		G	✓	✓	✓	✓	✓	-	-
5	IPENA05		F	✓	-	-	-	-	-	-
4	IPENA04		E	✓	✓	✓	✓	✓	✓	✓
3	IPENA03		D	✓	✓	✓	✓	✓	✓	✓
2	IPENA02		C	✓	✓	✓	✓	✓	✓	✓
1	IPENA01		B	✓	✓	✓	✓	✓	✓	✓
0	IPENA00		A	✓	✓	✓	✓	✓	✓	✓

5.2. *[CGFSYSENB]*

Table 5.2 *[CGFSYSENA]* per product allocation

Bit	Bit Symbol	Connection destination	Channel number/ Unit name/ I/O port name	M3H6	M3H5	M3H4	M3H3	M3H2	M3H1	M3H0
31	IPENB31	SIWDT	-	✓	✓	✓	✓	✓	✓	✓
30	IPENB30	-	-	-	-	-	-	-	-	-
29	IPENB29	-	-	-	-	-	-	-	-	-
28	IPENB28	-	-	-	-	-	-	-	-	-
27	IPENB27	-	-	-	-	-	-	-	-	-
26	IPENB26	-	-	-	-	-	-	-	-	-
25	IPENB25	-	-	-	-	-	-	-	-	-
24	IPENB24	-	-	-	-	-	-	-	-	-
23	IPENB23	-	-	-	-	-	-	-	-	-
22	IPENB22	-	-	-	-	-	-	-	-	-
21	IPENB21	-	-	-	-	-	-	-	-	-
20	IPENB20	-	-	-	-	-	-	-	-	-
19	IPENB19	-	-	-	-	-	-	-	-	-
18	IPENB18	-	-	-	-	-	-	-	-	-
17	IPENB17	-	-	-	-	-	-	-	-	-
16	IPENB16	-	-	-	-	-	-	-	-	-
15	IPENB15	-	-	-	-	-	-	-	-	-
14	IPENB14	-	-	-	-	-	-	-	-	-
13	IPENB13	-	-	-	-	-	-	-	-	-
12	IPENB12	-	-	-	-	-	-	-	-	-
11	IPENB11	-	-	-	-	-	-	-	-	-
10	IPENB10	-	-	-	-	-	-	-	-	-
9	IPENB09	-	-	-	-	-	-	-	-	-
8	IPENB08	-	-	-	-	-	-	-	-	-
7	IPENB07	TRGSEL	-	✓	✓	✓	✓	✓	✓	✓
6	IPENB06	TRM	-	✓	✓	✓	✓	✓	✓	✓
5	IPENB05	OFD	-	✓	✓	✓	✓	✓	✓	✓
4	IPENB04	RMC	0	✓	✓	✓	✓	✓	✓	✓
3	IPENB03	RTC	-	✓	✓	✓	✓	✓	-	-
2	IPENB02	DAC	1	✓	✓	-	-	-	-	-
1	IPENB01		0	✓	✓	✓	✓	✓	-	-
0	IPENB00	ADC	A	✓	✓	✓	✓	✓	✓	✓

6. Revision history

Table 6.1 Revision history

Revision	Date	Description
1.0	2017-09-04	First release
2.0	2018-03-07	Conventions: Revised Terms and Abbreviations: Revised 2.4. Warming up function Corrected: “ high frequency / each low frequency” ->”high speed oscillator / low speed oscillator” 2.6. System clock Corrected: “oscillation clock, external”->“oscillation clock and external” 3.1.1. The feature in each mode Corrected: “▪ Port setting status”->“▪ Port pin status” Added: “▪ RLM” 3.1.2. Transition to and Return from Low Power Consumption mode Corrected: “3.1.2. Low Power Consumption mode” ->” 3.1.2. Transition to and Return from Low Power Consumption mode” Deleted: “There are the IDLE mode, --------- in a Low Power Consumption mode.” 3.1.4. The peripheral function state in a Low Power Consumption mode Corrected: Table 3.2 “ O ” -> ” ✓ ” RMC STOP2(ELOSC:Off) “ - ” -> ” × ” Note1: “Check that the peripheral function・・・・” Note2: “WDT”->”SIWDT” 3.2. Transition to and return from a Low Power Consumption mode Corrected: “3.2. Switch to and return from a Low Power Consumption mode” -> “3.2. Transition to and return from a Low Power Consumption mode” Corrected: Figure 3.1 3.2.1. IDLE mode transition flow Corrected: “Because IDLE mode・・・・” Corrected: Table “WDT”->”SIWDT” 3.2.2. STOP1 mode transition flow Corrected: “Because STOP1 mode・・・・” Corrected Table “WDT”->”SIWDT” 3.2.3. STOP2 mode transition flow Corrected: “Because STOP2 mode・・・・” Corrected: Table “WDT”->”SIWDT” Corrected: Note2 “1,2,14 and 16 steps”->” 1,2,13 and 15 steps” 3.3.1. The release source of a Low Power Consumption mode Added: Table 3.3 “(Note1)” (2 places) , “(Note2)” (2 places) Corrected: Table 3.3 “INT00、01、02”->” INT00、INT01、INT02” “INTI2C0WUP”->” INTI2CWUP” ”INTENC00,01 “”->”INTENC00, INTENC01” “INTADPDA”->”INTADAPDA”,“INTADPDB”->”INTADAPDB” “INTADCPA”->”INTADACP0”,“INTADCPB”->”INTADACP1” “INTADTRG”->”INTADATRG”,“INTADSGL”->”INTADASGL” “INTADCNT”->”INTADACNT”,“WDT”->”SIWDT” Corrected: Table 3.3 Reset(OFD) STOP1 “ ✓ ” -> ” × ” Added: Table 3.3 Note1, Note2 Corrected: ● Released by Non-Maskable Interrupt (NMI)

		"WDT interrupt (INTWDT) " -> " SIWDT interrupt (INTWDT, protected mode A only) " 3.3.2. Warming up at the release of Low Power Consumption mode Corrected: "<WUPT[15:0]>"->" <WUPT[15:4]>" 3.3.3.The restart operation from the STOP2 mode Corrected: Figure 3.2 3.4.1. NORMAL >>> IDLE >>> NORMAL Operation mode transition Corrected: "The CPU stops IDLE mode."->" The CPU stops at IDLE mode." 4.1. Register list Corrected: "(Note1,Note2)" ->"(Note)" Deleted: Note2 Deleted: "In addition, when you write into ---------- write the initial value." 4.2.9. ***[CGFSYSENA]*** (Clock supply and stop register A for fsys) Corrected: Function column Added: Note2 4.2.10. ***[CGFSYSENB]*** (Clock supply and stop register B for fsys) Corrected: Function column Added: Note2 4.2.11. ***[CGSPCLKEN]*** (Clock Supply for ADC and Trace Register) Corrected: "4.2.11. [CGSPCLKEN] (Clock Supply for ADC and Trace Register)" -> " 4.2.11. ***[CGSPCLKEN]*** (Clock Supply and stop register for ADC and Trace)" 4.2.12. ***[RLMLOSCCR]*** (low speed oscillation control register) Added: Bit 1 4.2.13. ***[RLMSHTDNOP]*** (power supply cut off control register) Corrected: Function column 5. Information according to product Revised: Change the table from product to register.
2.1	2019-7-23	- Revised Toshiba Logo. -Terms and Abbreviations modified CG, added TPIU -2.3 Figure 2,1 modified about DEBUG block -2.4.1 revised the value of <WUPT[15:4]> from 0xFF to 0xFFF. -3.1.1 revised the sentence from "IDLE, STOP1, and the STOP2 mode" to " Low ower Consumption mode". revised from "forbid" to "disable". added "IA" and "I^2C Wake up" as the STOP2 Area. -3.1.2 Revised the section title. -3.2 Revised the section title. -3.2.1 Revised from "led" to "read". -3.3.3. Revised from "Reset by STOP2" to "STOP2 release interrupt". revised from "check the TOP2 return factor" to "Jump to the interrupt routine and check the STOP2 return factor". -4.1 Revised CG Function from "A clock and mode control" to " Clock Control and operation mode". -4.2.1 Revised description of POTTECT[7:0]. -4.2.5 Revised from "impossible" to "inhibit". -4.2.11 Revised the function of TRCKEN.(added "SWV"). -5.1 Revised from "✓" to "×" of TSPI CH0 in M3H0. Revised from "✓" to "×" of PORT L in M3H2. Revised "RESTRICTIONS ON PRODUCT USE".

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