32-bit RISC Microcontroller

TXZ Family

Reference manual
8-bit Digital to Analog Converter
(DAC-A)

Revision 1.0
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## Preface

Related document

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<tr>
<th>Document name</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock Control and Operation Mode</td>
</tr>
<tr>
<td>Product Information</td>
</tr>
</tbody>
</table>
Conventions

- Numeric formats follow the rules as shown below:
  - Hexadecimal: 0xABC
  - Decimal: 123 or 0d123 – Only when it needs to be explicitly shown that they are decimal numbers.
  - Binary: 0b111 – It is possible to omit the "0b" when the number of bit can be distinctly understood from a sentence.
- ".N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m: n].
  - Example: S[3: 0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by [] defines the register.
  - Example: [ABCD]
- "n" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  - Example: [XYZ1], [XYZ2], [XYZ3] -> [XYZn]
- "x" substitutes suffix number or character of units and channels in the Register List.
  - In case of unit, "x" means A, B, and C ...
  - Example: [ADACR0], [ABCR0], [ADCCR0] -> [ADxCR0]
  - In case of channel, "x" means 0, 1, and 2 ...
  - Example: [T32A0RUNA], [T32A1RUNA], [T32A2RUNA] -> [T32AxRUNA]
- The bit range of a register is written like as [m: n].
  - Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  - Example: [ABCD]<EFG> =0x01 (hexadecimal), [XYZn]<VW> =1 (binary)
- Word and Byte represent the following bit length.
  - Byte: 8 bits
  - Half word: 16 bits
  - Word: 32 bits
  - Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  - R: Read only
  - W: Write only
  - R/W: Read and Write are possible
- Unless otherwise specified, register access supports only word access.
- The register defined as reserved must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of ".-" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is ".-", follow the definition of each register.
- Reserved bits of the Read-only register should be written with their default value.
  - In the cases that default is ".-", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.
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Terms and Abbreviations

Some of abbreviations used in this document are as follows:

DAC      Digital to Analog Converter
1. Outlines

8-bit digital / analog converter (DAC) builds in the DAC output circuit of one channel (DACx) per 1 unit. The main functions are as follows.

<table>
<thead>
<tr>
<th>Function Classification</th>
<th>Function</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>DAC output</td>
<td>Conversion system</td>
<td>R-2R Resistance rudder type</td>
</tr>
<tr>
<td></td>
<td>Resolution</td>
<td>8 bits</td>
</tr>
<tr>
<td></td>
<td>Buffer amplifier</td>
<td>Un-built-in</td>
</tr>
</tbody>
</table>

2. Configuration

![Diagram](image)

**Figure 2.1** 8-bit DAC configuration

**Table 2.1 List of signals**

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>DACx</td>
<td>DAC Output terminal</td>
<td>Output</td>
<td>Product Information</td>
</tr>
<tr>
<td>2</td>
<td>VREFH</td>
<td>Analog reference power supply terminal</td>
<td>Input</td>
<td>Product Information</td>
</tr>
<tr>
<td>3</td>
<td>VREFL</td>
<td>Analog reference GND terminal</td>
<td>Input</td>
<td>Product Information</td>
</tr>
</tbody>
</table>
3. Function and Operation

3.1. Setting

When you use DAC, please set an applicable clock enable bit to "1" (clock supply) in fsys supply stop register A (/CGFSYSENA/, /CGFSYSMENA/), fsys supply stop register B (/CGFSYSENB/, /CGFSYSMENB/), and fc supply stop register (/CGFCEN/). Please refer to "Clock Control and Operation Mode" of the reference manual for the details.

The voltage corresponding to the preset value is outputted to the DACx terminal by setting /DAxCR/<EN> to "1" and setting the conversion value to the /DAxREG/ register.

By setting /DAxCR/<EN> to "0", DAC stops operation and the DAC output becomes Hi-Z.
4. Registers

4.1. List of Registers

<table>
<thead>
<tr>
<th>Peripheral function</th>
<th>Function name</th>
<th>Channel/Unit</th>
<th>Base address TYPE 1</th>
<th>Base address TYPE 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>8-bit Digital to Analog Converter</td>
<td>DAC</td>
<td>ch0</td>
<td>0x40054000</td>
<td>0x400BC800</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ch1</td>
<td>0x40055000</td>
<td>0x400BC900</td>
</tr>
</tbody>
</table>

Note: The Channel/Unit and Base address type are different by products. Please refer to "Product Information" of the reference manual for the details.

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Address(Base+)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Control Register</td>
<td>[DAxCR] 0x0000</td>
</tr>
<tr>
<td>Converted Value Setting Register</td>
<td>[DAxREG] 0x0004</td>
</tr>
</tbody>
</table>

4.2. [DAxCR] (Control Register)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Symbol</th>
<th>After Reset</th>
<th>Type</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:1</td>
<td>-</td>
<td>0</td>
<td>R</td>
<td>Read as &quot;0&quot;</td>
</tr>
<tr>
<td>0</td>
<td>EN</td>
<td>0</td>
<td>R/W</td>
<td>DAC operation</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0: Stop</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1: Operating</td>
</tr>
</tbody>
</table>

4.3. [DAxREG] (Converted Value Setting Register)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Symbol</th>
<th>After Reset</th>
<th>Type</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>-</td>
<td>0</td>
<td>R</td>
<td>Read as &quot;0&quot;</td>
</tr>
<tr>
<td>7:0</td>
<td>DAC[7:0]</td>
<td>0x00</td>
<td>R/W</td>
<td>Converted value setting: Digital value corresponding to the analog output voltage value is set. The output voltage is calculated with the following formula. DACx = &lt;DAC&gt; x (VREFH - VREFL) / 256</td>
</tr>
</tbody>
</table>
5. Revision History

Table 5.1 Revision History

<table>
<thead>
<tr>
<th>Revision</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.0</td>
<td>2017-09-04</td>
<td>First release</td>
</tr>
</tbody>
</table>
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