# 32-bit RISC microcontroller

# TXZ Family

## Reference Manual
## DMA Controller
## (DMAC-B)

## Revision2.0

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**TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION**

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# Preface

**Related document**

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| Clock control and Operation mode |

## Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal:   0xABC
  Decimal:          123 or 0d123 – Only when it needs to be explicitly shown that they are decimal numbers.
  Binary:      0b111 – It is possible to omit the "0b" when the number of bit can be distinctly understood from a sentence.

- "_N" is added to the end of signal names to indicate low active signals.

- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.

- When two or more signal names are referred, they are described like as [m: n].
  Example: S[3:0] shows four signal names S3, S2, S1 and S0 together.

- The characters surrounded by *[ ]* defines the register.
  Example:   *[ABCD]*

- "n" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example:   *[XYZ1], [XYZ2], [XYZ3]* ➔   *[XYZn]*

- "x" substitutes suffix number or character of units and channels in the Register List.

  In case of unit, "x" means A, B, and C . . .
  Example:   *[ADACR0], [ADBCR0], [ADCCR0]*➔*[ADxCR0]*
  In case of channel, "x" means 0, 1, and 2 . . .
  Example: [*T32A0RUNA], [T32A1RUNA], [T32A2RUNA]* ➔*[T32AxRUNA]*

- The bit range of a register is written like as [m: n].
  Example:   Bit[3: 0] expresses the range of bit 3 to 0.

- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example:   *[ABCD]*<EFG> = 0x01 (hexadecimal), *[XYZn]*<VW> = 1 (binary)

- Word and Byte represent the following bit length.
  Byte:          8 bits
  Half word:        16 bits
  Word:        32 bits
  Double word:    64 bits

- Properties of each bit in a register are expressed as follows:
  R:          Read only
  W:          Write only
  R/W:        Read and Write are possible

- Unless otherwise specified, register access supports only word access.

- The register defined as reserved must not be rewritten. Moreover, do not use the read value.

- The value read from the bit having a default value of "-" is unknown.

- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is "-", follow the definition of each register.

- Reserved bits of the Write-only register should be written with their default value. In the cases that default is "-", follow the definition of each register.

- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

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**Terms and Abbreviations**

Some of the abbreviations used in this document are as follows:

DMA  Direct Memory Access

# 1. Outline

The main functions of the DMA controller (DMAC) per one unit are explained below.

| Function classification | Function | Functional Description |
|---|---|---|
| Transmission request and type | Start Trigger | Starting of DMA by peripheral or software |
| | Single transmission | It waits for the next transmission request, after carrying out data transfer once. |
| | Burst transmission | Data transfer is carried out once or two or more times. |
| Transfer mode | Normal transmission | There are the following two kinds of normal transmission.<br>- Unit normal transmission: Data is transmitted for every unit by one transmission request.<br>- Continuation normal transmission: All the data is transmitted by one transmission request. |
| | Repeat transmission | Repeat transmission repeats and carries out unit normal transmission continuously.<br>Repeating infinitely by soft processing is possible. |
| | Chain transmission | Chain transmission transmits data dispersed based on the transmission list.<br>There are the following two kinds of a normal transmission.<br>- Unit chain transmission: Data is transmitted for every unit by one transmission request.<br>- Continuation chain transmission: All the data is transmitted by one transmission request. |
| Channel control | Transmission address | The address of the source and a destination address shall be set up. |
| | Transmission data size | 8 bits, 16 bits, 32 bits |
| | Priority | The priority of run time is decided by the channel designator and two steps of priority setup. |
| | Arbitration | DMA transmission is arbitrated for every channel.<br>It is possible to set up the existence of arbitration (nothing, 1 to 512 times).<br>It is possible to carry out burst transmission efficiently by this setup. |
| Number of transfer times | Normal transmission | A maximum of 1024 times |
| | Repeat transmission | Infinity (however, soft processing is required) |
| | Chain transmission | A maximum of 256x1024 times |
| Interrupt function | End of Transmission | Completion of data transfer will generate a transmission end interrupt. |
| | Error interrupt | When a bus error and a memory protection error occur during data transfer, an error interrupt will be generated. |

# 2. Configuration
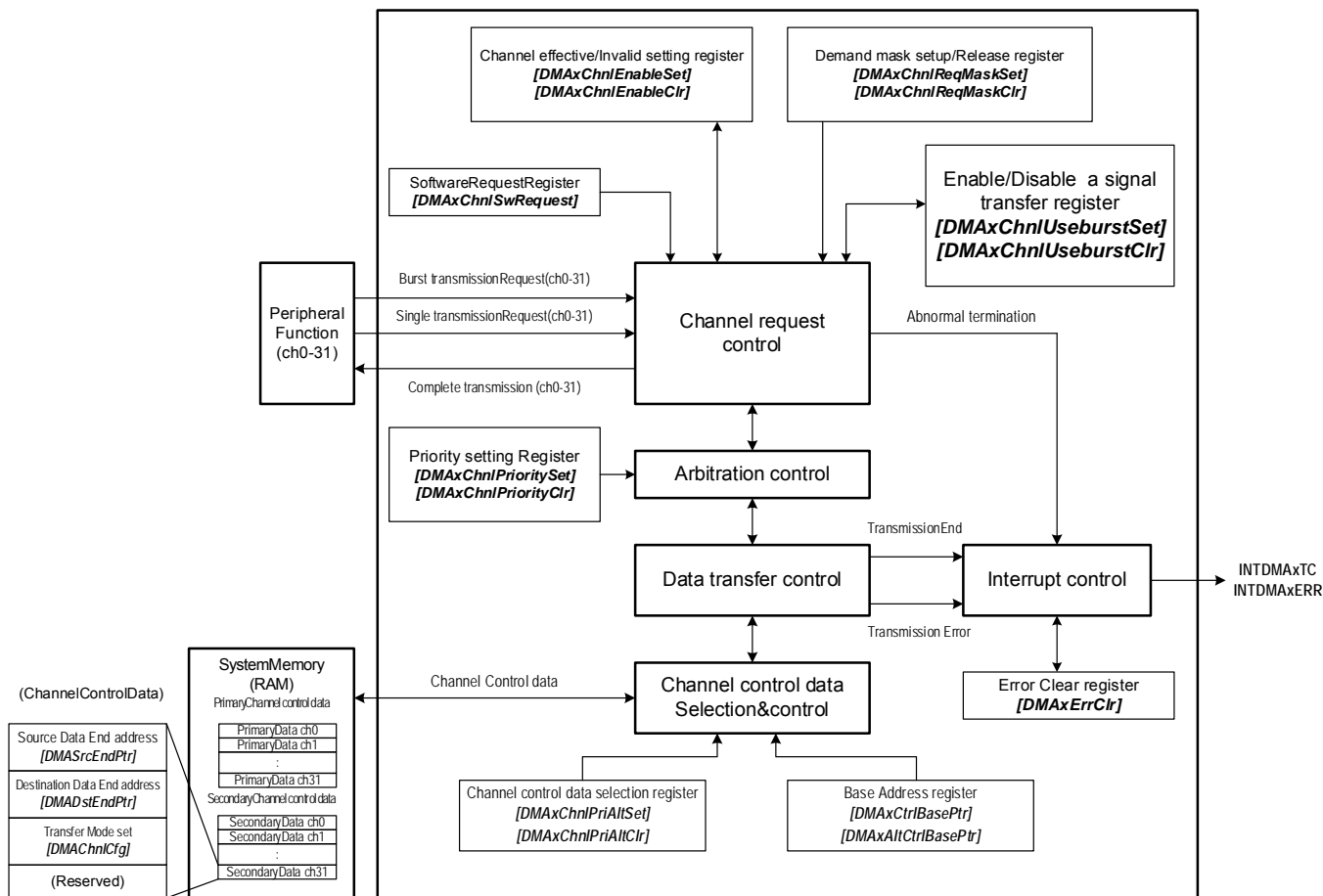


**Figure 2.1    DMAC Block Diagrams (common unit)**

**Table 2.1    List of Signals**

| No. | Symbol | Signal name | I/O | Related Reference manual |
|-----|--------|-------------|-----|--------------------------|
| 1 | INTDMAxTC | DMAC transmission end interrupt | Output | Exception |
| 2 | INTDMAxERR | DMAC transmission error interrupt | Output | Exception |
| 3 | - | Single transmission request | Input | Product Information |
| 4 | - | Burst transmission request | Input | Product Information |
| 5 | - | Channel control data | Input/output | This manual |

# 3. Detail of Function and Operation

This DMAC is controlled by a DMA register and channel control data. Although channel control data is arranged in a memory. For the structure of data, refer to the "3.2. Channel control data".
There are primary data and secondary data in channel control data, and it may use the case where only either is used by an Operation mode and both.

## 3.1. Transfer mode

Each transfer mode is explained.

### 3.1.1. Normal transmission

The Normal transmission uses one channel control data (either primary data or secondary data are available).
There are the following two with the disposal method for a transmission request.

- Unit normal transmission

    The Data transfer is carried out for every unit by one transmission request.

    Then, it waits for the next transmission request.

- Continuation normal transmission:

    All the data transfer is carried out by one transmission request.

    It does not wait for the next transmission request.

#### 3.1.1.1. Unit normal transmission

DMA will transmit data for every unit, if a transmission request is received. An arbitration is performed after that and it waits for the next transmission request. Interrupt of transmission End is generated for this operation after the transmission implementation for the total number of times of transmission.
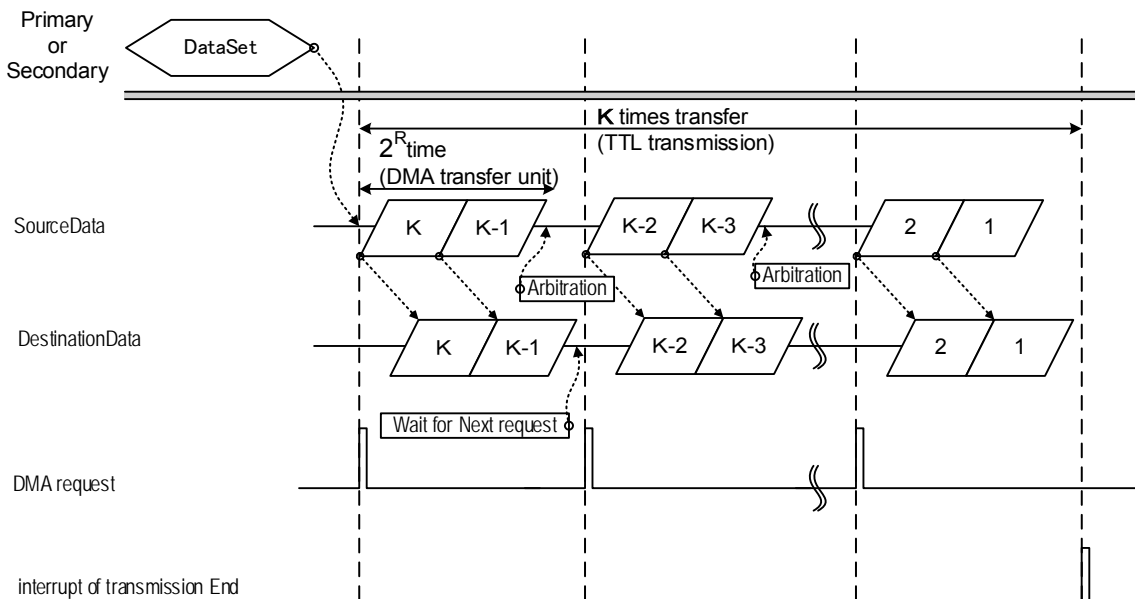


**Figure 3.1    Unit normal transmission**

### 3.1.1.2. Continuous normal transmission

Although the basic operation is the same as unit normal transmission, in continuous normal transmission, it does not wait for the next transmission request after arbitration enforcement.
Interrupt of transmission End is generated for this operation after the transmission implementation for the total number of times of transmission.
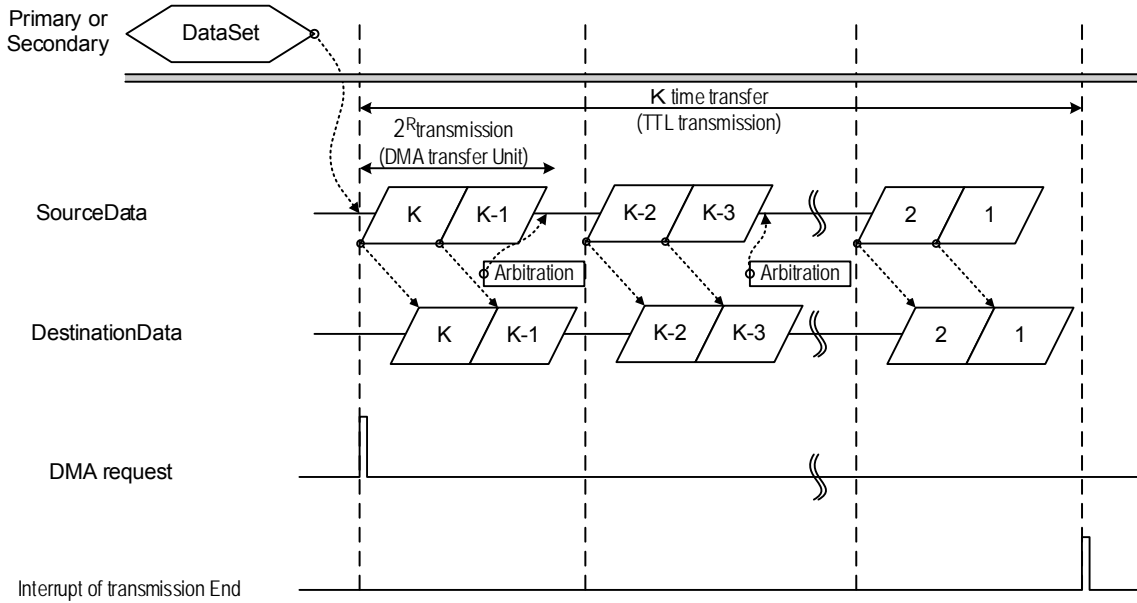


**Figure 3.2    Continuous normal transmission**

## 3.1.2. Repeat transmission

Repeat transmission uses two channel control data. The start can be either primary data or secondary data, but the consecutive unit normal transmission is performed while alternately using both channel control data. A transmission end interrupt occurs after completing the data transfer of one channel control, and it changes to the data transfer of the channel control of another side. Please reset the completed channel control data by interrupt processing. By repeating this, data transfer is infinitely continuable.
DMA transmission is terminated by setting DMA invalid to the control data of the channel.
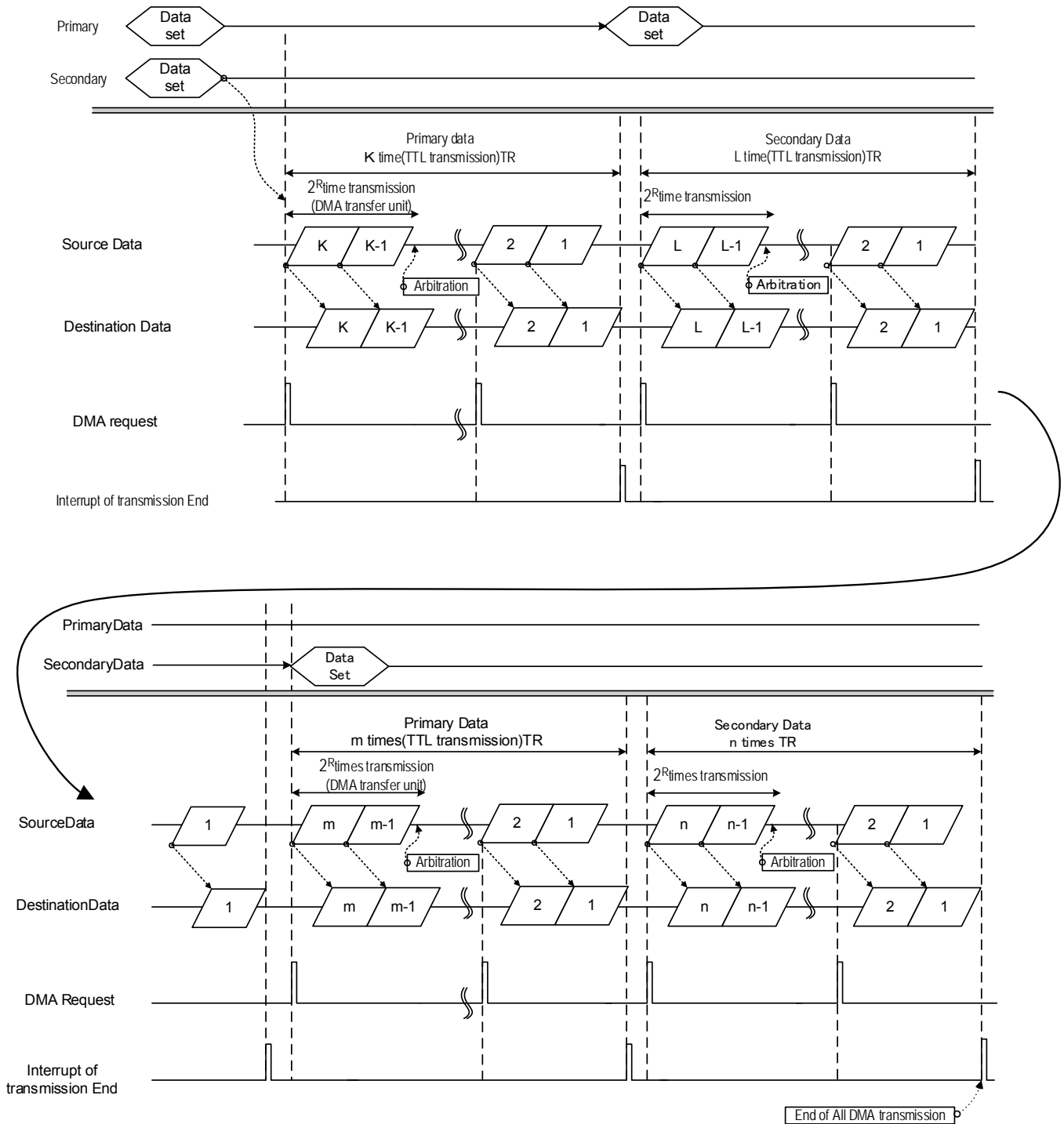
**Figure 3.3    Repeat transmission**

### 3.1.3. Chain transmission

Chain transmission uses two channel control data, it carries out normal transmission two or more times.
When the number of times of transmission runs short in normal transmission mode, or when the source or a destination address is a discontinuous area, it is used for data transfer. For example, it is possible to extract only real data excluding the header from packet information and to store continuously in the memory domain area.
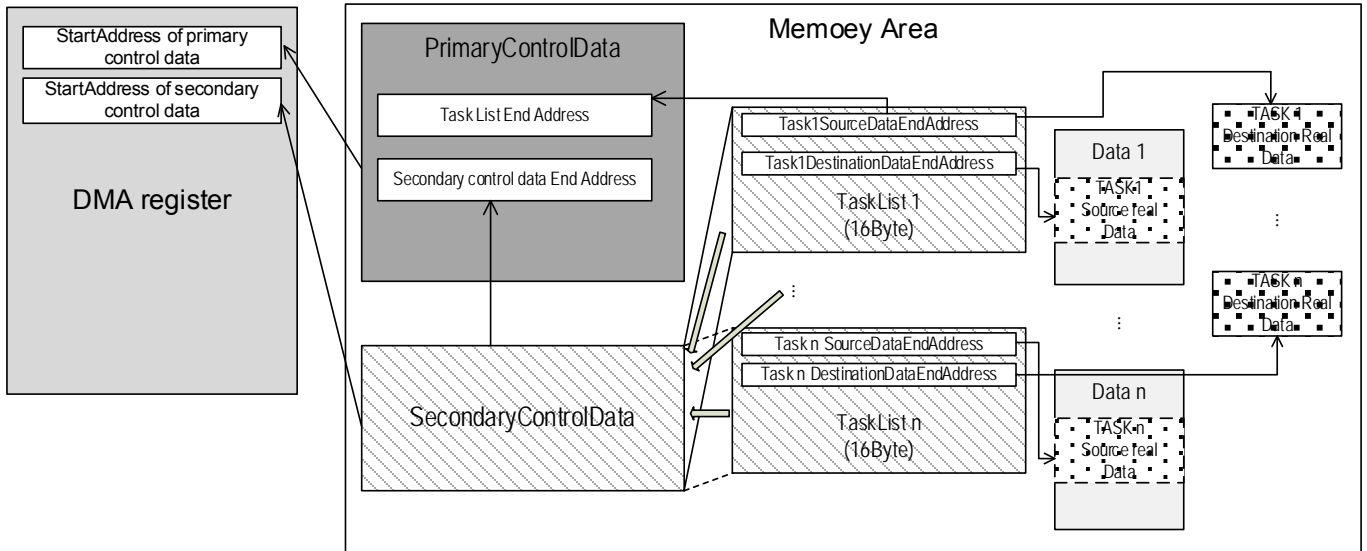


**Figure 3.4    The channel control data on the chain transmission, the role of a task list**

In addition to the primary or secondary channel control data, a task list is needed in order to use chain transmission. The role of the primary and secondary channel control data and a task list is explained as follows.

– Task list
4 words of the same composition as channel control data shall be one set, and it prepares this two or more sets. The end address of the real data of a source, the end address of destination real data, and transfer mode are, and each set describes a setup of DMA transmission to actually transmit.

– Primary channel control data
It is used in order to carry out DMA transmission of the task list to the secondary control data area. In order to transmit by 4 word units, 1024/4= 256 task becomes the maximum number of transfer times.

– Secondary channel control data
It is used in order to perform a task list. Since each operation becomes a normal transmission, 1024 times becomes the maximum number of transfer times.

Normal transmission is carried out two or more times, rewriting secondary channel control data by primary channel control data. There are two kinds of chain transmission as well as normal transmission.

▪ Unit chain transmission
The Data transfer is carried out for every unit by one transmission request. Then, it waits for the next transmission request.

▪ Continuation chain transmission
All the data transfer is carried out by one transmission request. Then, it does not wait for the next transmission request.

### 3.1.3.1. Unit chain transmission

After receiving a DMA transfer request and performing transmission to the secondary control data area of the task list by primary control data, and real data transfer by a task list, once it stops till the next transmission request. The same transmission is repeated by the next transmission request, and a DMA transfer is performed to the task list of the last set as DMA transfer invalidity.

End interrupt of transmission is generated after the end of transmission by the last task list.
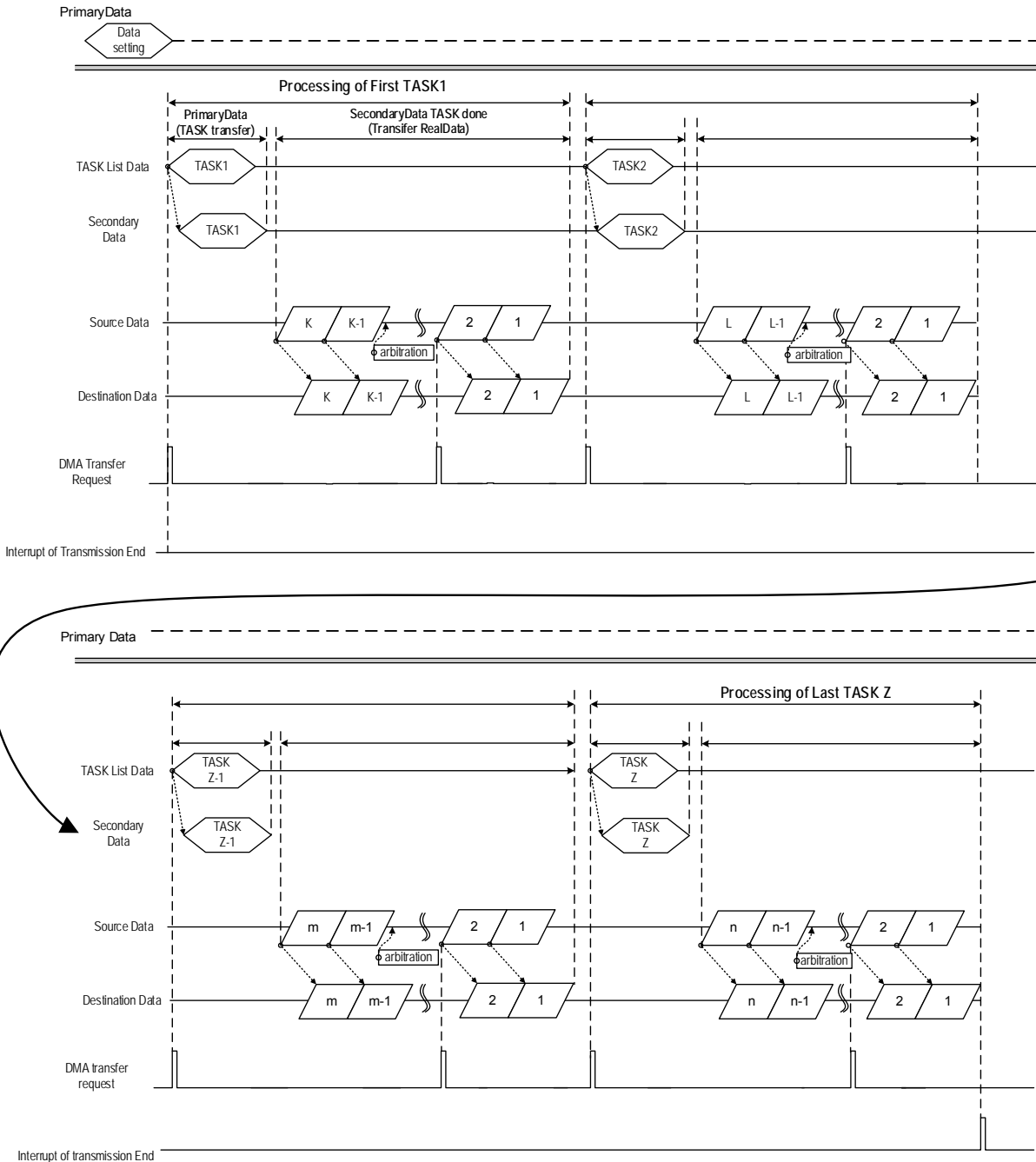
**Figure 3.5    Unit chain transmission**

### 3.1.3.2. Continuation chain transmission

In unit chain transmission, it once stops after the end of transmission of each task list and waits for the next transmission request. In continuation chain transmission, without waiting for the next transmission request, the next transmission is started and it transmits till the completion of transmission by the last task list in which DMA transfer invalidity was set up. Interruption is generated after the end of transmission by the last task list.
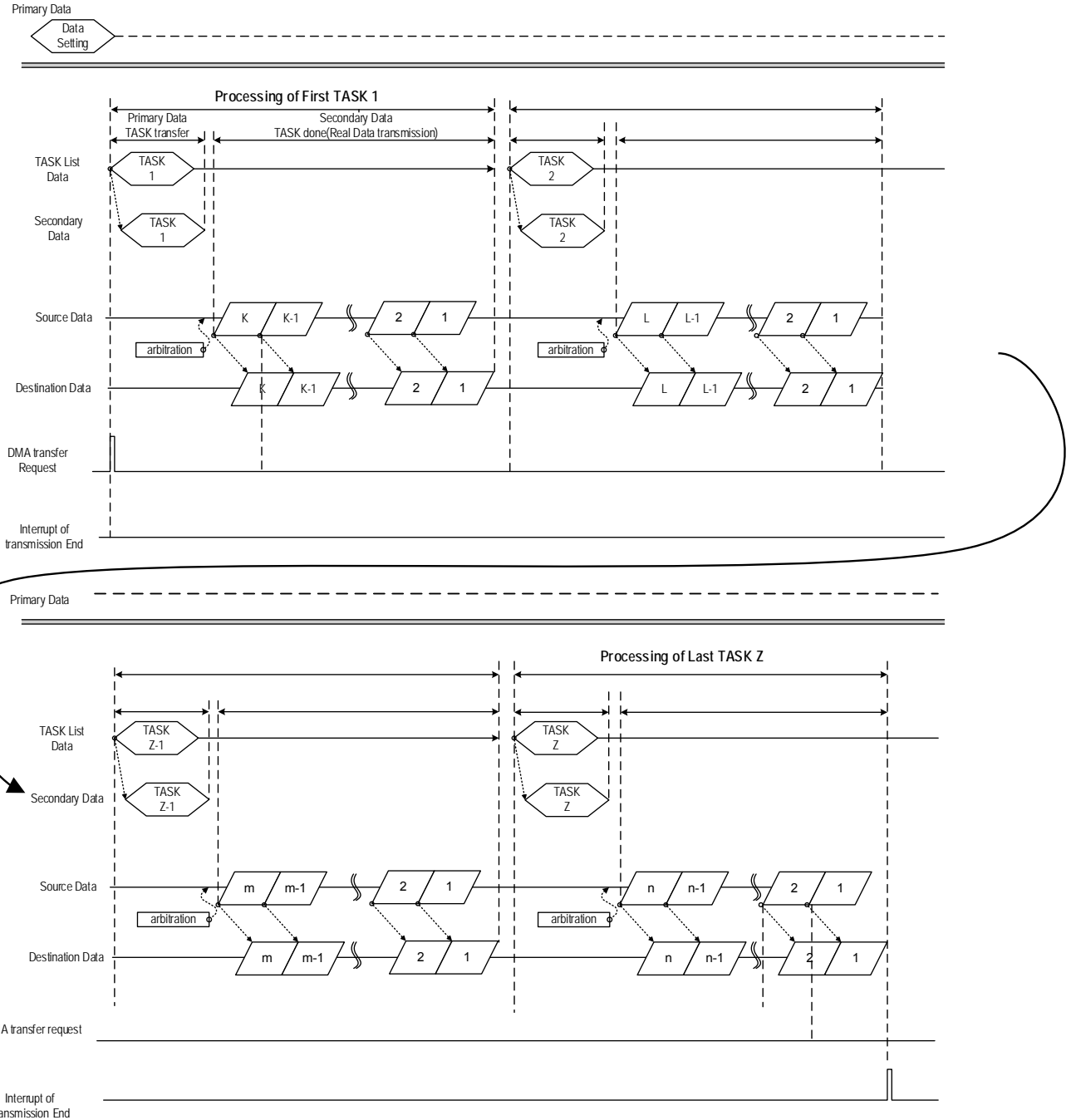
**Figure 3.6　Continuation chain transmission**

## 3.2. Channel control data

DMA controller, it is controlled by channel control data and the table of channel control data on a memory. By transfer mode, each DMA channel has one channel control data (primary data or secondary data) or two channel control data (primary data and secondary data) in a table. The End address of source data, the End address of destination data, and a transfer mode setup is included in channel control data.

### 3.2.1. Channel control data memory map

Figure3.7 The memory map of a control data table shows the example of a memory map of channel control data. As channel control data, 4 words per channel data is arranged to the space continuous by the channel number, and 1 KB (maximum) of the domain is used. For this reason, it is necessary to arrange the start address of channel control data so that an address [9:0] may become 0x000.
The start address for primary data is set as *[DMAxCtrlBasePtr]*, and the start address for secondary data is returned to *[DMAxAltCtrlBasePtr]*.

| The contents of channel control data | Address |
|---|---|
| The End address of source data | 0x000 |
| The End address of destination data | 0x004 |
| Transfer mode setup | 0x008 |
| Reserved | 0x00C |

| | | Channel control data table | | |
|---|---|---|---|---|
| Primary data | Address | Secondary data | Address |
| Primary ch0 | 0x000 | Secondary ch0 | 0x200 |
| Primary ch1 | 0x010 | Secondary ch1 | 0x210 |
| Primary ch2 | 0x020 | Secondary ch2 | 0x220 |
| Primary ch3 | 0x030 | Secondary ch3 | 0x230 |
| Primary ch4 | 0x040 | Secondary ch4 | 0x240 |
| Primary ch5 | 0x050 | Secondary ch5 | 0x250 |
| Primary ch6 | 0x060 | Secondary ch6 | 0x260 |
| Primary ch7 | 0x070 | Secondary ch7 | 0x270 |
| Primary ch8 | 0x080 | Secondary ch8 | 0x280 |
| Primary ch9 | 0x090 | Secondary ch9 | 0x290 |
| Primary ch10 | 0x0A0 | Secondary ch10 | 0x2A0 |
| Primary ch11 | 0x0B0 | Secondary ch11 | 0x2B0 |
| Primary ch12 | 0x0C0 | Secondary ch12 | 0x2C0 |
| Primary ch13 | 0x0D0 | Secondary ch13 | 0x2D0 |
| Primary ch14 | 0x0E0 | Secondary ch14 | 0x2E0 |
| Primary ch15 | 0x0F0 | Secondary ch15 | 0x2F0 |
| Primary ch16 | 0x100 | Secondary ch16 | 0x300 |
| Primary ch17 | 0x110 | Secondary ch17 | 0x310 |
| Primary ch18 | 0x120 | Secondary ch18 | 0x320 |
| Primary ch19 | 0x130 | Secondary ch19 | 0x330 |
| Primary ch20 | 0x140 | Secondary ch20 | 0x340 |
| Primary ch21 | 0x150 | Secondary ch21 | 0x350 |
| Primary ch22 | 0x160 | Secondary ch22 | 0x360 |
| Primary ch23 | 0x170 | Secondary ch23 | 0x370 |
| Primary ch24 | 0x180 | Secondary ch24 | 0x380 |
| Primary ch25 | 0x190 | Secondary ch25 | 0x390 |
| Primary ch26 | 0x1A0 | Secondary ch26 | 0x3A0 |
| Primary ch27 | 0x1B0 | Secondary ch27 | 0x3B0 |
| Primary ch28 | 0x1C0 | Secondary ch28 | 0x3C0 |
| Primary ch29 | 0x1D0 | Secondary ch29 | 0x3D0 |
| Primary ch30 | 0x1E0 | Secondary ch30 | 0x3E0 |
| Primary ch31 | 0x1F0 | Secondary ch31 | 0x3F0 |

**Figure 3.7    The memory map of a control data table**

Figure3.7 is an example in the case of using primary/secondary data of all 32 channels. The required memory area varies depending on the number of channels available for the product and the channel number.

### 3.2.2. Structure of channel control data

Channel control data contains the following three kinds of data.
- The End address of source data
- The End address of destination data
- Transfer mode setup

Each content is explained below.

### 3.2.2.1. Source data End address (DMASrcEndPtr)

The End address of the data to transmit is set up. Please unite alignment of an address with transmission data size. DMA calculates the start address of a source based on this address.

| Bit | Bit symbol | Function |
|---|---|---|
| [31:0] | src_data_end_ptr | The End address of source data |

### 3.2.2.2. Destination data End address (DMADstEndPtr)

The End address of a destination is set up. Please unite alignment of an address with transmission data size. DMA calculates the start address of a destination based on this address.

| Bit | Bit symbol | Function |
|---|---|---|
| [31:0] | dst_data_end_ptr | The End address of a destination |

### 3.2.2.3. Transfer mode setup (DMAChnlCfg)

A parameter required for DMA transmission is set.

| Bit | Bit symbol | Function |
|---|---|---|
| [31:30] | dst_inc | Increment of a transfer destination address (Note2)<br>00: 1byte<br>01: 2byte<br>10: 4byte<br>11: no increment |
| [29:28] | dst_size | Destination data size (Note1)<br>00: 1byte<br>01: 2byte<br>10: 4byte<br>11: Reserved |
| [27:26] | src_inc | Increment of a source address (Note2)<br>00: 1byte<br>01: 2byte<br>10: 4byte<br>11: no increment |
| [25:24] | src_size | Source data size (Note1)<br>00: 1byte<br>01: 2byte<br>10: 4byte<br>11: Reserved |
| [23:18] | - | Please set up "000000." |
| [17:14] | R_power | The run unit of arbitration<br>0000:  One After time transmission<br>0001:  Two After time transmission<br>0010:  Four After time transmission<br>0011:  Eight After time transmission<br>0100:  16 After time transmission<br>0101:  32 After time transmission<br>0110:  64 After time transmission<br>0111:  128 After time transmission<br>1000:  256 After time transmission<br>1001:  512 After time transmission<br>1010  to 1111:   Arbitration toughness<br>Arbitration is performed for every set-up number of transfer times. |
| [13:4] | n_minus_1 | Number of transfer times<br>0x000:   One Time<br>0x001:   Two Times<br>0x002:   Three Times<br>:<br>0x3FF:   1024 Times   (Note3)<br>The value which subtracted 1 from the total of the data to transmit is set up. |
| [3] | next_useburst | Single transfer setting change   (Note4)<br>0:  The remaining transmission also uses single transmission.<br>1:  The remaining transmission does not use single transmission (burst transmission is used).<br>A single transfer is prohibited at the end of DMA transfer using secondary data in unit chain transfer, Specify whether to continue the transfer or not. |
| [2:0] | cycle_ctrl | Transfer mode<br>000:  Suspend DMA operation.<br>001:  Unit normal transmission<br>010:  Continuation normal transmission<br>011:  Repeat transmission<br>100:  Continuation chain transmission (primary data)<br>101:  Continuation chain transmission (secondary data)<br>110:  Unit chain transmission (primary data)<br>111:  Unit chain transmission (secondary data) |

Note1: <dst_size> should set up the same value as <src_size>.

Note2: By setting <dst_size> and <src_size>, settings of <dst_inc> and <src_inc> are restricted as shown in Table 3.1.

Note3: 1024 times is the upper limit in case of normal transmission.

Note4: When the remaining number of times of transmission is less than $2^R$ time from the last at the time of the 2nd end of $2^R$ times transmission ("R" is set up by <R_power>), single transmission is permitted automatically, but it is setting this bit to "1", and single transmission is carried out to prohibition and burst transmission can be continued.

**Table 3.1   Setup list about transmission**

| <src_inc>/<dst_inc> | <src_size>/<dst_size> | | |
|---|---|---|---|
| | **00**<br>**(1byte)** | **01**<br>**(2byte)** | **10**<br>**(4byte)** |
| 00(1byte) | ✓ | - | - |
| 01(2byte) | ✓ | ✓ | - |
| 10(4byte) | ✓ | ✓ | ✓ |
| no increment | ✓ | ✓ | ✓ |

If the setting is as following <dst_size> ≠ <src_size>, at the time of renewal of unit transmission, the value of <dst_size> is set to <src_size>.

## 3.3. Initialization

The next setup is required to use DMA.

1. Clock supply to DMA

2. Preparation of channel control data

3. Common initialization of a register

### 3.3.1. Clock supply to DMA

When you use DMA, the corresponding clock enable bits should be set to "1" (Clock supply) in fsys supply stop register A (*[CGFSYSENA]*, *[CGFSYSMENA]*), fsys supply stop register B (*[CGFSYSENB]*, *[CGFSYSMENB]*), and fc supply stop register (*[CGFCEN]*). The corresponding registers and the bit locations depend on a product. Some products do not have all registers. For the details, refer to "Clock Control and Operation Mode" in the Reference manual.

### 3.3.2. Preparation of channel control data

It is necessary to prepare the channel control data of the channel to be used. For details, such as a composition of data, and arrangement, please refer to the "3.2. Channel control data".

### 3.3.3. Common initialization of a register

This DMA also has the function to inform of the abnormal termination by a transmission end interrupt. For details of data structure and configuration, please refer to "3.10 Interrupt".
In order to prevent interrupt which is not meant, carry out the next processing to all the units before starting to use DMA.

> *[DMAxCfg]* = 0x00000001;
>
> *[DMAxChnlReqMaskSet]* = 0xFFFFFFFF;
>
> *[DMAxChnlEnableSet]* = 0xFFFFFFFF;

Next, carry out a register setup of the channel control data used at first. Initialization is "primary data." When you change to "primary data" → "secondary data", write "1" into the corresponding channel bit of the *[DMAxChnlPriAltSet]* register. When you change to "secondary data" → "primary data", write "1" into the corresponding channel bit of the *[DMAxChnlPriAltClr]* register.
It is only normal transmission and repeats transmission that "secondary data" can be chosen as channel control data used first. Please choose "primary data" in chain transmission.
A setting value can be checked by reading the *[DMAxChnlPriAltSet]* register. Moreover, in repeat transmission and chain transmission, if the data transfer set up by each channel control data is completed, a setup of "Primary data" ←→ "secondary data" will change automatically.

## 3.4. Priority

A DMA controller performs data transfer according to the priority of each channel. A priority is decided in the following setting combination of Table 3.2.

- Priority setup    (a setup "High priority" and "Normal" is possible, and "High priority" has top priority)
- Channel number (Channel 0 has the highest priority, and priority takes priority in ascending order of numbers)

The default of a priority setup is "Normal." When you change into "High priority" from "Normal", write "1" to the corresponding channel bit of the *[DMAxChnlPrioritySet]* register. When you change into "Normal" from "High priority", write "1" into the corresponding channel bit of *[DMAxChnlPriorityClr]* register.

**Table 3.2    Channel priority**

| Priority setup | Channel number | Priority (descending order) |
|---|---|---|
| High priority | Ch 0 | The channel of the highest priority |
| High priority | Ch 1 | - |
| : | : | - |
| High priority | Ch 31 | - |
| Normal | Ch 0 | - |
| Normal | Ch 1 | - |
| : | : | - |
| Normal | Ch 31 | The channel of the minimum priority |

## 3.5. The kind of transmission request

This DMA supports the burst transmission and the single transmission request. Refer to the "Product Information" of a reference manual for starting factor connection of each peripheral and a transmission request.

- Single transmission:

  It waits for the next transmission, after doing data transfer once.

  Enable or disable single transmission can be set up for every channel.

- Burst transmission:

  Data transfer is done once or, two or more times.

  It can be set up for every channel whether it waits for the next transmission request. For details, refer to the "3.6 Arbitration ".

  The burst transmission is always a permission setup (a prohibition setup cannot be performed).

To enable a single transmission, when you permit the single transfer request, write "1" into the corresponding channel bit of the *[DMAxChnlUseburstSet]* register. For disabled, write "1" into the corresponding channel bit of the *[DMAxChnlUseburstClr]* register.

Burst transmission is usually set as permission. For this reason, the request of burst transmission and single transmission overlaps and it makes it not generate.
(If it generates simultaneously, a burst transmission request has priority and is processed.)
When it is peripheral by which the starting factor is connected to both burst transmission and single transfer.
Carry out a fraction by single transmission after carrying out transmission of a number two or more times by burst transmission. When unit chain transfer mode is used, there is a function changed from burst transmission to single transmission.

## 3.6. Arbitration

When a transmission request is generated, this DMA chooses the channel which carries out transmission processing according to "3.4. Priority" from all the channels which the request has generated. This means the arbitration.
The run unit of arbitration can be set up by *[DMAChnlCfg]* <R_power>. Since the channel concerned occupies DMA if a set value is enlarged, the latency time of other channels increases. Therefore, in order to transmit a high priority channel efficiently, do not set up a High arbitration unit to a low priority channel.
Moreover, in the case of the peripheral corresponding to burst transmission, a Burst size of the arbitration unit of DMAC and the peripheral function is made the same.
In case of chain transmission, make sure to set the arbitration unit of primary data to *[DMAChnlCfg]* <R_power> =0010.

## 3.7. Data size and an address

This DMA is supporting the data size of 1, 2 or 4 bytes. Although the source can set up *[DMAChnlCfg]*<src_size> and a destination by *[DMAChnlCfg]*<dst_size>, respectively, both should set up the same value.
Moreover, the address is supporting 1, 2 or 4 bytes of increment, or fixing. The source can set up *[DMAChnlCfg]*<src_inc> and a destination individually by *[DMAChnlCfg]* <dst_inc>. In the case of increment, set up the increment size to become more than data size. For details, refer to the "3.2.2.3Transfer mode setup (DMAChnlCfg)".

## 3.8. Number of transmissions

A number of transmission sets the numerical value which subtracted 1 from the total number of transfer times as *[DMAChnlCfg]* <n_minus_1>. A value can be set up to 0 to 1023 and it means that this can perform one to 1024 transmission by one channel control data.

A normal transmission is using a one channel control data, therefore a maximum transmission is 1024 times.
A chain transmission is using two channel control data, therefore a maximum transmission is 256x1024 times.
Although a repeat transmission similarly is using two channel control data, a maximum transmission is infinite since infinity can be set up at soft processing.

Moreover, this DMA updates *[DMAChnlCfg]* <n_minus_1>, just before going into arbitration. Thereby, a value shows the remaining number of transmission.

## 3.9. DMA starting

When you use DMA, set mask release (write "1" into the corresponding bit of *[DMAxChnlReqMaskClr]*) of a unit and the channel. However, do not release the same factor simultaneously.
If there is a transmission request from a peripheral, it will perform according to a setup of channel control data.
When using a software start, write "1" into the corresponding bit of *[DMAxChnlSwRequest]*.

## 3.10. Interrupt

This DMA generates two kinds of the interrupt, a transmission end interrupt, and transmission error interrupt.

### 3.10.1. Transmission end interrupt

Completion of the transmission set up by channel control data will generate a transmission end interrupt.
In repeat transmission, it is possible to set up the following channel control data using transmission end interrupt processing.
Also in the following case, it generates in addition to the time of this interrupt and a Normal operation.

- When a corresponding DMA is in a disabled state and a DMA transmission request occurs, a transmission end interrupt occurs as abnormal termination interrupt.

- When channel control data is not set up, Enable a corresponding channel or release a request mask, and also a DMA transmission request is generated, a transmission end interrupt occurs as abnormal termination interrupt.

In normal transmission or chain transmission, the corresponding channel is in the state of invalidity (the corresponding bit of *[DMAxChnlEnableSet]* is "0"), and mask release (the corresponding bit of *[DMAxChnlReqMaskSet]* is "0"). When an interrupt request occurs from a peripheral once again in this state, since the transmission end interrupt which means abnormal termination occurs, cautions are required.
In the data transmitting processing especially by DMA, data transmission is not completed when a transmission end interrupt occurs.
Since a transmitting interrupt occurs after the completion of transmitting or FIFO becomes empty,
Please complete that a corresponding channel is effective (write "1" into the corresponding bit of *[DMAxChnlEnableSet]*), and mask processing (write "1" into the corresponding bit of *[DMAxChnlReqMaskSet]*) by then.

### 3.10.2. Transmission error interrupt

Detection of a bus error and a memory protection error will generate a transmission error interrupt. At this time, DMA makes a corresponding channel invalidity (the corresponding bit of *[DMAxChnlEnableSet]* is "0"), and sets it to *[DMAxErrClr]* =0x00000001.
When the Error interrupt is generated, write "0x00000001" into *[DMAxErrClr]* to clear it.

# 4. Register explanation

## 4.1. Register list

The register and address of DMA are shown below.

| Function name | | A channel/unit | Base Address(Base) | | |
|---|---|---|---|---|---|
| | | | **TYPE1** | **TYPE2** | **TYPE3** |
| DMA controller | **DMAC** | Unit A | 0x4004C000 | 0x400A4000 | 0x40044000 |
| | | Unit B | 0x4004D000 | 0x400A5000 | 0x40045000 |
| | | Unit C | 0x4004E000 | 0x400A6000 | 0x40046000 |
| | | Unit D | 0x4004F000 | 0x400A7000 | 0x40047000 |

Note: The Channel/Unit and Base address type are different by products. Please refer to "Product Information" of the reference manual for the details

| Register name | | Address (Base+) |
|---|---|---|
| DMAC status | *[DMAxStatus]* | 0x000 |
| DMAC configuration | *[DMAxCfg]* | 0x004 |
| Channel control data base pointer | *[DMAxCtrlBasePtr]* | 0x008 |
| Channel alternate control data base pointer | *[DMAxAltCtrlBasePtr]* | 0x00C |
| Channel software request | *[DMAxChnlSwRequest]* | 0x014 |
| Channel useburst set | *[DMAxChnlUseburstSet]* | 0x018 |
| Channel useburst clear | *[DMAxChnlUseburstClr]* | 0x01C |
| Channel request mask set | *[DMAxChnlReqMaskSet]* | 0x020 |
| Channel request mask clear | *[DMAxChnlReqMaskClr]* | 0x024 |
| Channel enable set | *[DMAxChnlEnableSet]* | 0x028 |
| Channel enable clear | *[DMAxChnlEnableClr]* | 0x02C |
| Channel primary-alternate set | *[DMAxChnlPriAltSet]* | 0x030 |
| Channel primary-alternate clear | *[DMAxChnlPriAltClr]* | 0x034 |
| Channel priority set | *[DMAxChnlPrioritySet]* | 0x038 |
| Channel priority clear | *[DMAxChnlPriorityClr]* | 0x03C |
| Bus error clear | *[DMAxErrClr]* | 0x04C |

## 4.2. Register description

### 4.2.1. *[DMAxStatus]* (DMAC Status Register)

| Bit | Bit Symbol | After reset | Type | Function |
|---|---|---|---|---|
| 31:29 | - | 0 | R | Read as "0" |
| 28 | - | 1 | R | Read as "1". |
| 27:21 | - | 0 | R | Read as "0" |
| 20:16 | - | 0x1F | R | Read as "0x1F". |
| 15:8 | - | 0 | R | Read as "0". |
| 7:4 | - | Undefined | R | Read as "Undefined". . |
| 3:1 | - | 0 | R | Read as "0". |
| 0 | Master_enable | 0 | R | DMA operation<br>  0: disable<br>  1: enable |

### 4.2.2. *[DMAxCfg]* (DMAC Configuration Register)

| Bit | Bit Symbol | After reset | Type | Function |
|---|---|---|---|---|
| 31:1 | - | 0 | W | Write as "0" |
| 0 | Master_enable | 0 | W | DMA operation<br>  0: disable<br>  1: enable<br>A DMA Operation State is set up. |

Note: After setting up for all units as following, *[DMAxCfg]* = 0x00000001, *[DMAxChnlReqMaskSet]* = 0xFFFFFFFF, *[DMAxChnlEnableSet]* = 0xFFFFFFFF, set the channel of the unit to be used as mask release (corresponding bit of *[DMAxChnlReqMaskClr]* is set to "1"). However, do not release the same factor simultaneously in each unit.

### 4.2.3. *[DMAxCtrlBasePtr]* (Channel control data base pointer Register)

| Bit | Bit Symbol | After reset | Type | Function |
|---|---|---|---|---|
| 31:10 | Ctrl_base_ptr | 0x000000 | R/W | Primary data base addresses<br>The base address of primary data is specified. |
| 9:0 | - | 0 | R | Read as "0". |

### 4.2.4. *[DMAxAltCtrlBasePtr]* (Channel alternate control data base pointer Register)

| Bit | Bit Symbol | After reset | Type | Function |
|---|---|---|---|---|
| 31:0 | alt_ctrl_base_ptr | 0x00000000 | R | Secondary data base addresses<br>The base address of secondary data can be read.<br>Since the base address of secondary data can acquire information from the set point of primary data, it is not necessary to calculate it by software. |

### 4.2.5. *[DMAxChnlSwRequest]* (Channel software request Register)

| Bit | Bit Symbol | After reset | Type | Function |
|---|---|---|---|---|
| 31:0 | chnl_sw_request | 0x00000000 | W | DMA request<br>　0: Don't carry out a transmission request.<br>　1: Carry out a transmission request.<br>When generating a DMA request by software, write "1" into the corresponding bit of each channel. |

A software DMA request is generated, when a corresponding channel bit is set. In a unit normal transmission, it can be used instead of the transfer request from the peripheral.

### 4.2.6. *[DMAxChnlUseburstSet]* (Channel useburst set Register)

| Bit | Bit Symbol | After reset | Type | Function |
|---|---|---|---|---|
| 31:0 | chnl_useburst_set | 0x00000000 | R | Disabling single transmission<br>　0:　Enable single transmission<br>　1:　Disable single transmission<br>Each bit corresponds to a channel with the specified number.<br>By reading, enabling /disabling state of a single transmission of a corresponding channel can be checked.<br>In the following cases, a bit is operated automatically.<br>- The second from the last $2^R$ transfers ("R" is the control data *[DMAChnlCfg]* set with <R_power>) remaining transfer times at the end When the number is less than $2^R$, this bit is cleared to "0"<br><br>- By unit chain transmission, when *[DMAChnlCfg]* of control data <next_useburst> is set as "1", "1" is set to this bit after termination of DMA transmission by secondary data. |
| | | | W | 　1:　Forbid single transmission.<br><br>Writing "1" prohibits a single transfer of the corresponding channel, and only the burst transfer request becomes valid.<br>　The writing of "0" does not have a meaning. When releasing disable of a single transmission, it carries out by *[DMAxChnlUseburstClr]*. |

Note: When a number of transfer times<n_minus_1> are less than arbitration<R_power>, a DMA request stops occurring.
　Therefore, when a number of transfer times<n_minus_1> are less than arbitration<R_power>, write "0" into the corresponding bit of each channel.

### 4.2.7. *[DMAxChnlUseburstClr]* (Channel useburst clear Register)

| Bit | Bit Symbol | After reset | Type | Function |
|---|---|---|---|---|
| 31:0 | chnl_useburst_clr | 0x00000000 | W | Enable Single transmission<br>　1:　Enable single transmission.<br>Each bit corresponds to a channel with the specified number.<br>By writing "1", a single transfer of the corresponding channel is enabled.<br>Writing "0" has no meaning<br>Disabling single transmission and the Confirmation of a setup are performed by *[DMAxChnlUseburstSet]*. |

### 4.2.8. *[DMAxChnlReqMaskSet]* (Channel request mask set Register)

| Bit | Bit Symbol | After reset | Type | Function |
|---|---|---|---|---|
| 31:0 | chnl_req_mask_set | 0x00000000 | R | Status of DMA request mask<br>　0:　A DMA external request is valid.<br>　1:　A DMA external request is invalid.<br>Each bit corresponds to a channel (00 to 31) with the specified number.<br>In case of reading, the state of DMA external request mask of the corresponding channel can be checked for a valid or invalid. |
| | | | W | DMA request mask<br>　1: mask a DMA request from a peripheral circuit<br><br>The transmission request of the channel which corresponds if "1" is written becomes invalid. The writing of "0" does not have a meaning. When disabling mask, it will be done by *[DMAxChnlReqMaskClr]*. |

Note: After setting up for all units as follows, *[DMAxCfg]* = 0x00000001, *[DMAxChnlReqMaskSet]* = 0xFFFFFFFF, *[DMAxChnlEnableSet]* = 0xFFFFFFFF, set the channel of the unit to be used as mask release (corresponding bit of *[DMAxChnlReqMaskClr]* is set to "1"). However, do not release the same factor simultaneously in each unit.

### 4.2.9. *[DMAxChnlReqMaskClr]* (Channel request mask clear Register

| Bit | Bit Symbol | After reset | Type | Function |
|---|---|---|---|---|
| 31:0 | chnl_req_mask_clr | 0x00000000 | W | Release of a DMA request mask<br>　1:　Cancel the DMA request mask of the corresponding channel.<br><br>Each bit corresponds to a channel (00 to 31) with the specified number.<br>The DMA request mask of the channel corresponding by writing in "1" is invalid. The writing of "0" does not have a meaning.<br>To Confirm an effective setup channel and setup status is checked by *[DMAxChnlReqMaskSet]*. |

### 4.2.10. *[DMAxChnlEnableSet]* (Channel enable set Register)

| Bit | Bit Symbol | After reset | Type | Function |
|---|---|---|---|---|
| 31:0 | chnl_enable_set | 0x00000000 | R | Status of DMA operation<br>　0:　The corresponding channel is invalid.<br>　1:　The corresponding channel is valid.<br>Each bit corresponds to a channel with the specified number.<br>In case of reading, the valid /invalid state of the corresponding channel can be checked.<br>Moreover, in the following cases, it becomes invalid automatically.<br>- Termination of a DMA cycle<br>- When *[DMAChnlCfg]* <cycle_ctrl> reads the control data of "000"<br>- When a bus error occurs |
| | | | W | Setting of DMA operation<br>　1:　the corresponding channel is valid.<br>The channel corresponding by writing "1" is validated.<br>The writing of "0" does not have a meaning.<br>　Use *[DMAxChnlEnableClr]*, to become invalid to the corresponding channel. |

Note: After setting up for all units as following, *[DMAxCfg]* = 0x00000001, *[DMAxChnlReqMaskSet]* = 0xFFFFFFFF, *[DMAxChnlEnableSet]* = 0xFFFFFFFF, set the channel of the unit to be used as mask release (corresponding bit of *[DMAxChnlReqMaskClr]* is set to "1"). However, do not release the same factor simultaneously in each unit.

### 4.2.11. *[DMAxChnlEnableClr]* (Channel enable clear Register)

| Bit | Bit Symbol | After reset | Type | Function |
|---|---|---|---|---|
| 31:0 | chnl_enable_clr | 0x00000000 | W | DMA disabling<br>  1:  the corresponding channel is disable.<br>Each bit corresponds to a channel with the specified number.<br>The channel corresponding by writing "1" is invalid.<br>The writing of "0" does not have a meaning.<br>The Confirmation of an effective setup and setup state is done by *[DMAxChnlEnableSet]*.<br>Moreover, in the following cases, it becomes invalid automatically.<br>- Termination of a DMA cycle<br>- When *[DMAChnlCfg]* <cycle_ctrl> read the control data of "000"<br>- When a bus error occurs |

### 4.2.12. *[DMAxChnlPriAltSet]* (Channel primary-alternate set Register)

| Bit | Bit Symbol | After reset | Type | Function |
|---|---|---|---|---|
| 31:0 | chnl_pri_alt_set | 0x00000000 | R | Status of Primary data / secondary data selection<br>  0:  Primary data<br>  1:  Secondary data<br><br>Each bit corresponds to a channel with the specified number.<br>In case of reading, it can check whether the data of the corresponding channel are primary data or secondary data.<br>Moreover, in the following cases, a setup change automatically.<br><br>- When the data transfer of primary data is completed by repeat transmission, unit chain transmission, or continuation chain transmission.<br>- When the data transfer of secondary data is completed by repeat transmission, unit chain transmission, or continuation chain transmission. |
| | | | W | Setting of Primary data / secondary data selection<br>  1:  Use secondary data.<br><br>The data first used by the channel corresponding by writing 1" is set as the secondary data. The writing of "0" does not have a meaning.<br>The invalid setup is performed by *[DMAxChnlPriAltClr]*.<br>It is the unit normal transmission, continuation normal transmission, and repeat transmission that the second data can be specified as first data. |

### 4.2.13. *[DMAxChnlPriAltClr]* (Channel primary-alternate clear Register)

| Bit | Bit Symbol | After reset | Type | Function |
|---|---|---|---|---|
| 31:0 | chnl_pri_alt_clr | 0x00000000 | W | Release of a secondary data setup<br> 1: Use primary data.<br>Each bit corresponds to a channel with the specified number.<br>The data of the channel corresponding by writing "1" is set as primary.<br>The writing of "0" does not have a meaning.<br><br>To Confirm the secondary setup and a setup state is checked by *[DMAxChnlPriAltSet]*.<br>Moreover, in the following cases, a setup change automatically.<br>- When the data transfer of primary data is completed by unit chain transmission or continuation chain transmission<br>- When the data transfer of primary data is completed by repeat transmission<br>- When the data transfer of secondary data is completed by repeat transmission, unit chain transmission, or continuation chain transmission |

### 4.2.14. *[DMAxChnlPrioritySet]* (Channel priority set Register)

| Bit | Bit Symbol | After reset | Type | Function |
|---|---|---|---|---|
| 31:0 | chnl_priority_set | 0x00000000 | R | Status of Priority setup<br> 0: Normal priority<br> 1: High priority<br>Each bit corresponds to a channel with the specified number.<br>In case of reading, it can check whether the corresponding channel is a high priority or normal priority. |
| | | | W | Priority setup<br> 1: Set to a high priority.<br>The priority of the corresponding channel by writing "1" is set as the high priority.<br>To return to normal priority, use by *[DMAxChnlPriorityClr]*. |

### 4.2.15. *[DMAxChnlPriorityClr]* (Channel priority clear Register)

| Bit | Bit Symbol | After reset | Type | Function |
|---|---|---|---|---|
| 31:0 | chnl_priority_clr | 0x00000000 | W | Release of a high priority setup<br> 1: set to a normal priority.<br>Each bit corresponds to a channel with the specified number.<br>The priority of the channel corresponding by writing "1" is set as the normal priority.<br>The writing of "0" does not have a meaning.<br>The Confirmation of a setup of a high priority and a setup is checked by *[DMAxChnlPrioritySet]*. |

## 4.2.16. *[DMAxErrClr]* (Bus error clear Register)

| Bit | Bit Symbol | After reset | Type | Function |
|---|---|---|---|---|
| 31:1 | - | 0 | R | Read as "0" |
| 0 | err_clr | 0 | R | The generating state of a bus error or a memory protection error<br> 0: No error<br> 1: Error generating<br> It can be checked by reading whether the bus error or the memory protection error has occurred. |
| | | | W | Error release<br> 1: Error release<br><br>The error can be released by writing "1.<br>The writing of "0" does not have a meaning. |

# 5. The usage example

## 5.1. Basic operation

The example of a setting is shown below using the basic operation of DMA.

1. **Use ch0 of UART and DMA.**

   a. Setup on IP side which uses DMA ch0; (Enable DMA request output )

2. **Setup of DMA ch0 for Normal transmission;**

   a. Write "XX (read address of UART)"to <src_data_end_ptr>

   Setup of the read-out address on IP side　;

   b. Write "0x2000_xxxx+40" to <dst_data_end_ptr>

   Setup of the transfer destination address of data　;

   c. Write these values to *[DMAChnlCfg]* for ch0:

   Setup of the control data of ch0　;

   <dst_inc>= 01 (destination halfword address increment)

   <dst_size>= 01 (halfword transfer size)

   <src_inc>= 11 (no address increment for source)

   <src_size>= 01 (halfword transfer size)

   <R_power>= 0000 (arbitrate after each DMA transfer)

   <n_minus_1>= 0x14 (transfer 21 half words)

   <next_useburst>= 0 (not applicable)

   <cycle_ctrl>= 001 (unit normal transmission)

3. **Enable DMA Operation**

   Write master_enable =1 to *[DMAxCfg]*

4. **Disable single transmission request of ch0 (i.e., do not react to data available, wait for buffer full)**

   Write *[DMAxChnlUseburstSet]*[0]=1

5. **Enable transmission buffer full request of ch0**

   Write *[DMAxChnlReqMaskClr]*[0]=1

6. **Primary data structure for ch0**

   Write *[DMAxChnlPriAltClr]*[0]=1

7. **Enable ch0**

   Write *[DMAxChnlEnableSet]*[0]=1

# 6. Revision history

**Table 6.1    Revision history**

| Revision | Date | Description |
|---|---|---|
| 1.0 | 2017-09-07 | First release |
| 2.0 | 2018-04-23 | Revised about Copyright, Date and Revision number.<br>Deleted previous Table1.1 Title<br>Deleted note of 3.3.1<br>Revised Clock Supply section.(3.3.1)<br>Revised 4.1(added TYPE1/2/3 and Note)<br>Revised reading value of 4.2.1<br>Revised reset value of "0" and "-" of Register description (4.2.2, 4.2.7, 4.2.8, 4.2.9, 4.2.11, 4.2.13, 4.2.15, 4.2.16).<br>In 5.1, Corrected of register name to Bold italic type and also channel 0 changed to ch0 |

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