

32-bit RISC Microcontroller

TXZ Family

Reference Manual

Programmable Motor Control Circuit

Plus

(PMD+-A)

Revision 2.1

2019-07

TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

Contents

Preface	5
Related document.....	5
Conventions	6
Terms and Abbreviations	8
1. Outlines	9
2. Configuration.....	11
3. Function and Operation	13
3.1. Clock Supply	13
3.2. Pulse Width Modulation Circuit	14
3.2.1. Setting the PWM period.....	15
3.2.2. Compare function	15
3.2.3. Waveform mode	17
3.2.4. Interrupt processing.....	17
3.3. Conduction Control Circuit.....	18
3.4. Protection Control Circuit.....	21
3.4.1. EMG Protection Circuit.....	21
3.4.2. OVV Protection Circuit.....	23
3.4.3. Protection control when using the debug tool.....	23
3.5. Dead time Control Circuit.....	24
3.6. Synchronous Trigger Generation Circuit	26
4. Registers	29
4.1. List of Registers	29
4.2. Details of Registers.....	30
4.2.1. [PMDxMDEN] (PMD Enable Register)	30
4.2.2. [PMDxPORTMD] (Port Output Mode Register)	30
4.2.3. [PMDxMDCR] (PMD Control Register).....	31
4.2.4. [PMDxCNTSTA] (PWM Counter Status Register)	32
4.2.5. [PMDxMDCNT] (PWM Counter Register).....	33
4.2.6. [PMDxMDPRD] (PWM Period Register).....	33
4.2.7. [PMDxCMPU] (PWM Compare U Register)	34
4.2.8. [PMDxCMPV] (PWM Compare V Register).....	34
4.2.9. [PMDxCMPW] (PWM Compare W Register).....	35
4.2.10. [PMDxMDPOT] (PMD Output Setting Register)	36
4.2.11. [PMDxMDOUT] (PMD Conduction Control Register)	37
4.2.12. [PMDxEMGREL] (EMG Release Register).....	38
4.2.13. [PMDxEMGCR] (EMG Control Register)	39
4.2.14. [PMDxEMGSTA] (EMG Status Register).....	40
4.2.15. [PMDxOVVCR] (OVV Control Register)	40
4.2.16. [PMDxOVVSTA] (OVV Status Register).....	41
4.2.17. [PMDxDTR] (Dead time Register)	42

4.2.18. [PMDxTRGCMP0] (Trigger Compare 0 Register).....	42
4.2.19. [PMDxTRGCMP1] (Trigger Compare 1 Register).....	43
4.2.20. [PMDxTRGCMP2] (Trigger Compare 2 Register).....	43
4.2.21. [PMDxTRGCMP3] (Trigger Compare 3 Register).....	44
4.2.22. [PMDxTRGCR] (Trigger Control Register)	45
4.2.23. [PMDxTRGYNCR] (Trigger Update Timing Setting Register)	46
4.2.24. [PMDxTRGMD] (Trigger Output Mode Setting Register).....	47
4.2.25. [PMDxTRGSEL] (Trigger Output Selection Register).....	48
5. Precautions	49
6. Revision History	50
RESTRICTIONS ON PRODUCT USE.....	52

List of Figures

Figure 1.1	Functions related to Motor Control	10
Figure 2.1	PMD Block diagram	11
Figure 3.1	Pulse Width Modulation Circuit.....	14
Figure 3.2	PWM Waveforms	15
Figure 3.3	Waveforms of PWM triangular wave carrier using fixed edge	16
Figure 3.4	Conduction Control Circuit.....	18
Figure 3.5	Protection Control Circuit.....	21
Figure 3.6	Dead time Control Circuit.....	24
Figure 3.7	Dead time circuit	24
Figure 3.8	Dead time correction.....	25
Figure 3.9	Synchronous Trigger Generation Circuit	26
Figure 3.10	Example of using the PMD trigger at 3-shunt.....	27
Figure 3.11	Example of using the PMD trigger at 1-shunt.....	28

List of Tables

Table 2.1	List of signals	12
Table 3.1	<i>[PMDxMDOUT]</i> buffer Update Timing	19
Table 3.2	Decode circuit outputs according to <i>[PMDxMDOUT]</i> and <i>[PMDxMDCR]<SYNTMD></i> setting	19
Table 4.1	<i>[PMDxMDPRD]</i> , <i>[PMDxCMPU/V/W]</i> buffer Update Timing.....	32
Table 4.2	Port Outputs according to <i>[PMDxMDOUT]</i> and <i>[PMDxMDCR]<SYNTMD></i> settings.....	38
Table 4.3	<i>[PMDxTRGCMPn]</i> buffer Update Timing.....	42
Table 4.4	Trigger Output Patterns	47
Table 6.1	Revision History	50

Preface

Related document

Document name
Input/Output Ports
Exception
Clock Control and Operation Mode
Product Information
12-bit Analog to Digital Converter
Advanced Encoder Input Circuit

Conventions

- Numeric formats follow the rules as shown below:
Hexadecimal: 0xABC
Decimal: 123 or 0d123 – Only when it needs to be explicitly shown that they are decimal numbers.
Binary: 0b111 – It is possible to omit the "0b" when the number of bit can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m: n].
Example: S[3: 0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by [] defines the register.
Example: [ABCD]
- "n" substitutes suffix number of two or more same kind of registers, fields, and bit names.
Example: [XYZ1], [XYZ2], [XYZ3] → [XYZn]
- "x" substitutes suffix number or character of units and channels in the Register List.
In case of unit, "x" means A, B, and C ...
Example: [ADACR0], [ADBCR0], [ADCCR0] → [ADxCR0]
In case of channel, "x" means 0, 1, and 2 ...
Example: [T32A0RUNA], [T32A1RUNA], [T32A2RUNA] → [T32AxRUNA]
- The bit range of a register is written like as [m: n].
Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
Example: [ABCD]<EFG> =0x01 (hexadecimal), [XYZn]<VW> =1 (binary)
- Word and Byte represent the following bit length.
Byte: 8 bits
Half word: 16 bits
Word: 32 bits
Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
R: Read only
W: Write only
R/W: Read and Write are possible
- Unless otherwise specified, register access supports only word access.
- The register defined as reserved must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "—" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, in the cases that default is "—", follow the definition of each register.
- Reserved bits of the Write-only register should be written with their default value.
In the cases that default is "—", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

Arm, Cortex and Thumb are registered trademarks of Arm Limited (or its subsidiaries) in the US
and/or elsewhere. All rights reserved.



The Flash memory uses the Super Flash® technology under license from Silicon Storage Technology, Inc.
Super Flash® is registered trademark of Silicon Storage Technology, Inc.

All other company names, product names, and service names mentioned herein may be trademarks of their
respective companies.

Terms and Abbreviations

Some of abbreviations used in this document are as follows:

ADC	Analog to Digital Converter
A-ENC	Advanced Encoder Input Circuit
PMD	Programmable Motor Control Circuit
PWM	Pulse Width Modulation

1. Outlines

The programmable motor control circuit plus (PMD) can operate as a motor control circuit of 1 channel per unit. The following is a list of functions. The following is a list of functions.

Function Classification	Function	Operation
Output waveform generation	Resolution	The count resolution of PWM carrier: 1/fsys or 4/fsys. Resolution of PWM period and Duty Saw-tooth wave carrier: 1/fsys or 4/fsys Triangular wave carrier: 2/fsys or 8/fsys
	PWM generation	PWM carrier waveform: Saw-tooth wave or Triangular wave 3-phase PWM can be generated with three comparators. 3-phase mode: 3-phase common duty or 3-phase independent duty
	Output waveform (Conduction control)	Each of the U/X, V/Y and W/Z phases can be selected PWM or High/Low output. Upper-phase output or lower-phase output respectively can be set to low-active or high-active. This function has the common PWM carrier waveform and generates independent 3-phase complementary PWM.
Trigger generation	Synchronous trigger generation	It generates a synchronous sampling signal that starts AD conversion at an arbitrary timing synchronized with the PWM carrier.
Buffer function	-	PWM period, Duty, Synchronous trigger timing, and 6 port output setting are double-buffered. These setting can be changed during operation. Update timing can be selected by Asynchronous, Carrier bottom, Carrier peak, Carrier peak/bottom
Protection function	Protection control	This function stop output by protection signal input (OFF output or output disabled) Two types of protection function: EMG and OVV. OVV can be selected monitor function of ADC for protection input.
	Dead time control	The dead time control inserts the dead time for preventing short-circuit at switching between the upper-phase and lower-phase (U/X,V/Y,W/Z). The complementary PWM is output.
Interrupt request	PWM interrupt	PWM interrupt request is generated at a synchronous timing with the PWM period. - Interrupt timing: PWM carrier bottom or PWM carrier peak - Interrupt frequency: Half PWM period, one PWM period, two PWM period, or four PWM period.
	EMG interrupt	This interrupt request is generated by the EMG protection of EMGx_N input
	OVV interrupt	This interrupt request is generated by the OVV protection of OVV input

The PMD can control a 3-phase motor such as vector motors in conjunction with an analog to digital converter (ADC). The synchronous trigger generation circuit can command the ADC to start AD conversion.

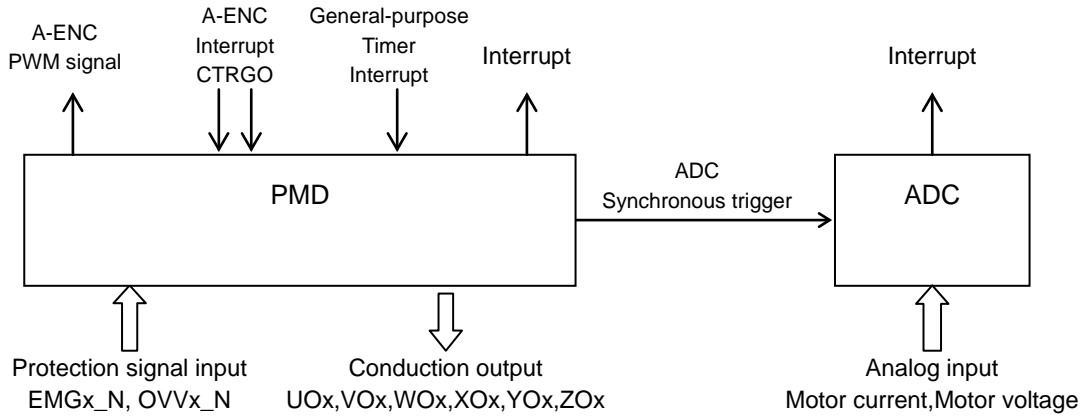


Figure 1.1 Functions related to Motor Control

2. Configuration

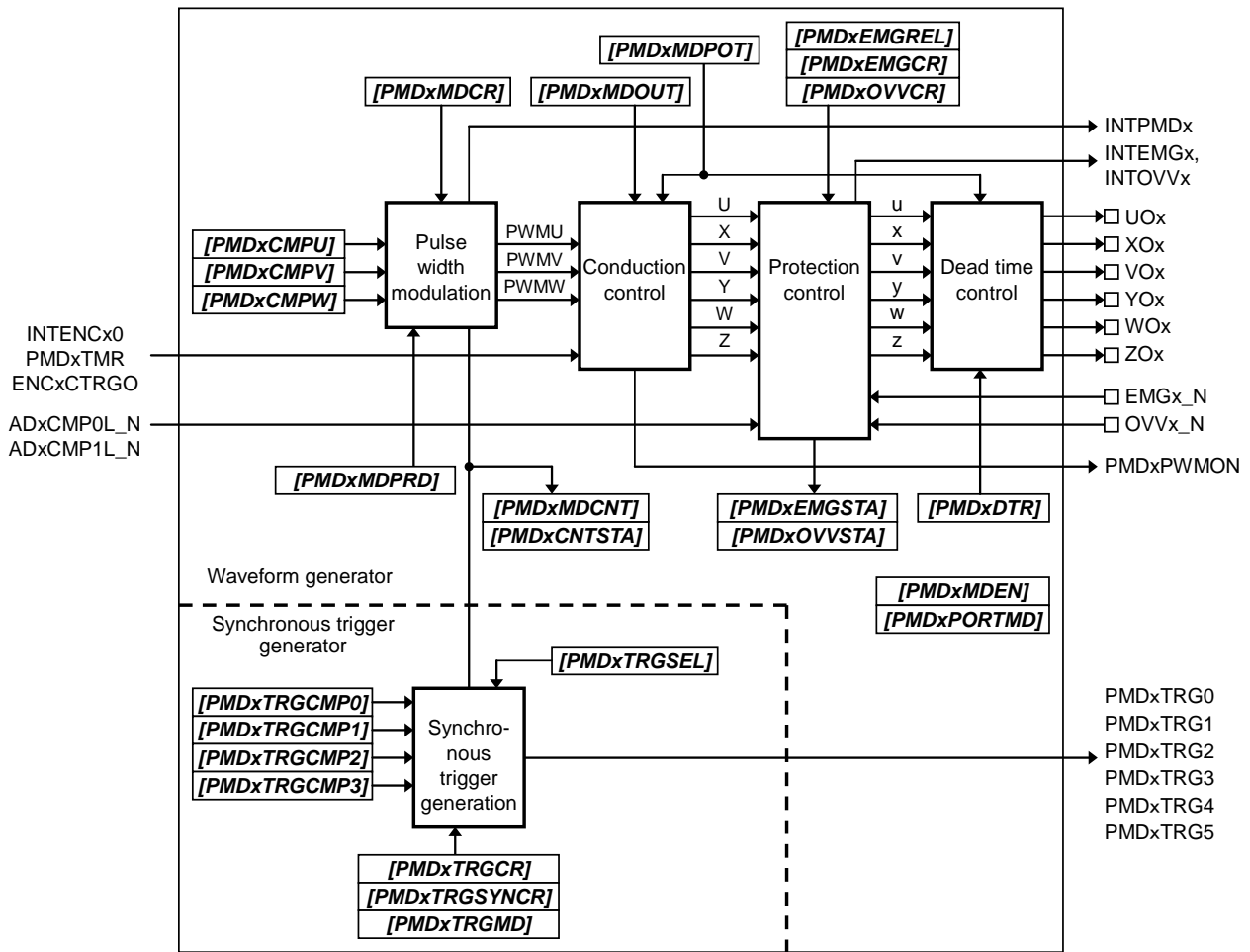


Figure 2.1 PMD Block diagram

Table 2.1 List of signals

No	Signal name		I/O	Related Reference manual
1	UOx	U-phase output pin	Output	Product Information
2	XOx	X-phase output pin	Output	Product Information
3	VOx	V-phase output pin	Output	Product Information
4	YOx	Y-phase output pin	Output	Product Information
5	WOx	W-phase output pin	Output	Product Information
6	ZOx	Z-phase output pin	Output	Product Information
7	EMGx_N	Emergency state detection input pin	Input	Product Information
8	OVVx_N	Over voltage detection input pin	Input	Product Information
9	PMDxPWMON	PWM signal for the encoder input	Output	Product Information
10	INTENCx0	Commutation trigger (A-ENC position detection synchronization)	Input	Product Information
11	PMDxTMR	Commutation trigger (General-purpose timer synchronization)	Input	Product Information
12	ENCxCTRGO	Commutation trigger (A-ENC MCMP completion synchronization)	Input	Product Information
13	ADxCMP0L_N	OVV state signal (AD monitor function 0)	Input	Product Information
14	ADxCMP1L_N	OVV state signal (AD monitor function 1)	Input	Product Information
15	PMDxTRG0	ADC synchronous sampling output 0	Output	Product Information
16	PMDxTRG1	ADC synchronous sampling output 1	Output	Product Information
17	PMDxTRG2	ADC synchronous sampling output 2	Output	Product Information
18	PMDxTRG3	ADC synchronous sampling output 3	Output	Product Information
19	PMDxTRG4	ADC synchronous sampling output 4	Output	Product Information
20	PMDxTRG5	ADC synchronous sampling output 5	Output	Product Information
21	INTPMDx	PWM interrupt	Output	Exception, Product Information
22	INTEMGx	EMG interrupt	Output	Exception
23	INTOVVx	OVV interrupt	Output	Exception

3. Function and Operation

The PMD circuit consists of two blocks of a wave generation circuit and a synchronous trigger generation circuit. The wave generation circuit includes a pulse width modulation circuit, a conduction control circuit, a protection control circuit, and a dead time control circuit.

- The pulse width modulation circuit has the common PWM carrier waveform and generates independent 3-phase PWM waveforms.
- The conduction control circuit determines the output pattern for each of the upper and lower sides of the U-, V-, and W-phases.
- The protection control circuit controls emergency output stop by EMG input and OVV input.
- The dead time control circuit prevents a short circuit which may occur when the upper side and lower side are switched.
- The synchronous trigger generation circuit generates synchronous trigger signals to the ADC for starting AD conversion..

3.1. Clock Supply

When using PMD, set an applicable clock enable bit to "1" (clock supply) in Clock supply and stop register A for fsys (*[CGFSYSENA]*, *[CGFSYSMENA]*), Clock supply and stop register B for fsys (*[CGFSYSENB]*, *[CGFSYSMENB]*), and Clock supply and stop register for fc (*[CGFCEN]*). An applicable register and the bit position vary according to a product. Therefore, the register may not exist with the product. Please refer to "Clock Control and Operation Mode" of the reference manual for the details.

3.2. Pulse Width Modulation Circuit

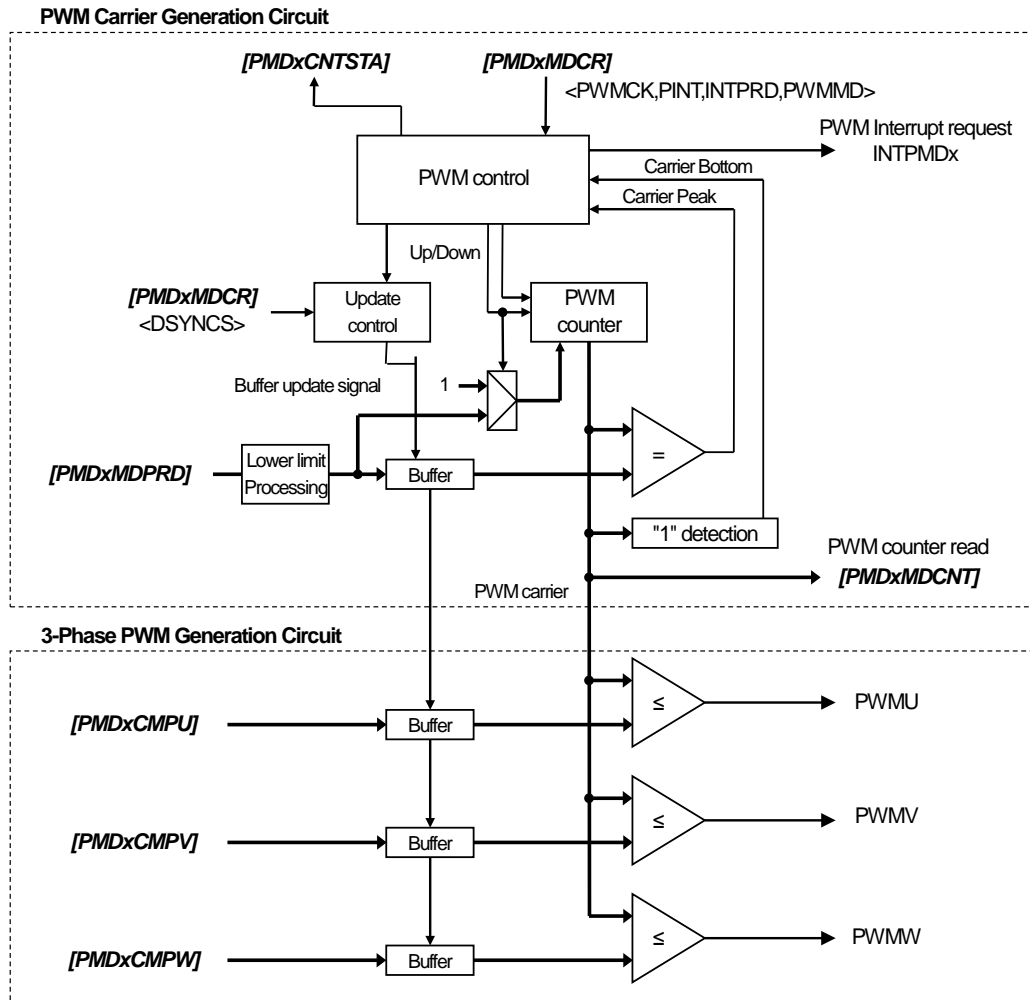


Figure 3.1 Pulse Width Modulation Circuit

The pulse width modulation circuit has a 16-bit PWM up/down-counter and generates PWM carrier waveforms with a resolution of $1/f_{sys}$. The PWM period extension mode ($[PMDxMDCR]\langle PWMCK \rangle = 1$) is also available. When this mode is selected, the PWM counter generates PWM carrier waveforms with a resolution of $4/f_{sys}$.

The PWM carrier waveform mode can be selected from mode 0 (edge-aligned PWM, saw-tooth waveform) and mode 1 (center-aligned PWM, triangular waveform). (Refer to "Figure 3.2 PWM Waveforms".)

3.2.1. Setting the PWM period

The PWM period is determined by the $[PMDxMDPRD]$ register. This register is double-buffered.

The subsequent stage buffer is updated at every PWM period. It is also possible to update at every half PWM period. (Refer to "Table 4.1 $[PMDxMDPRD],[PMDxCMPU/V/W]$ buffer Update Timing".)

$$\begin{aligned} \text{Sawtooth wave PWM} & : \quad [PMDxMDPRD] \text{ value} = \frac{\text{System clock } f_{\text{sys}} [\text{Hz}]}{\text{PWM frequency} [\text{Hz}]} \\ \text{Triangular wave PWM} & : \quad [PMDxMDPRD] \text{ value} = \frac{\text{System clock } f_{\text{sys}} [\text{Hz}]}{\text{PWM frequency} [\text{Hz}] \times 2} \end{aligned}$$

Note: When setting "4 × period", set a value of 1/4 to $[PMDxMDPRD]$.

3.2.2. Compare function

The pulse width modulation circuit generates PWM waveforms of the desired duty by comparing the magnitude of the 3-phase PWM compare registers ($[PMDxCMPU]$, $[PMDxCMPV]$, $[PMDxCMPW]$) and the PWM carrier which is generated by the PWM counter ($[PMDxMDCNT]$).

The PWM compare register of each phase has a double-buffered register. The PWM compare register value is loaded into the subsequent stage buffer at every PWM period. It is also possible to update at every half a PWM period. (Refer to "Table 4.1 $[PMDxMDPRD],[PMDxCMPU/V/W]$ buffer Update Timing".)

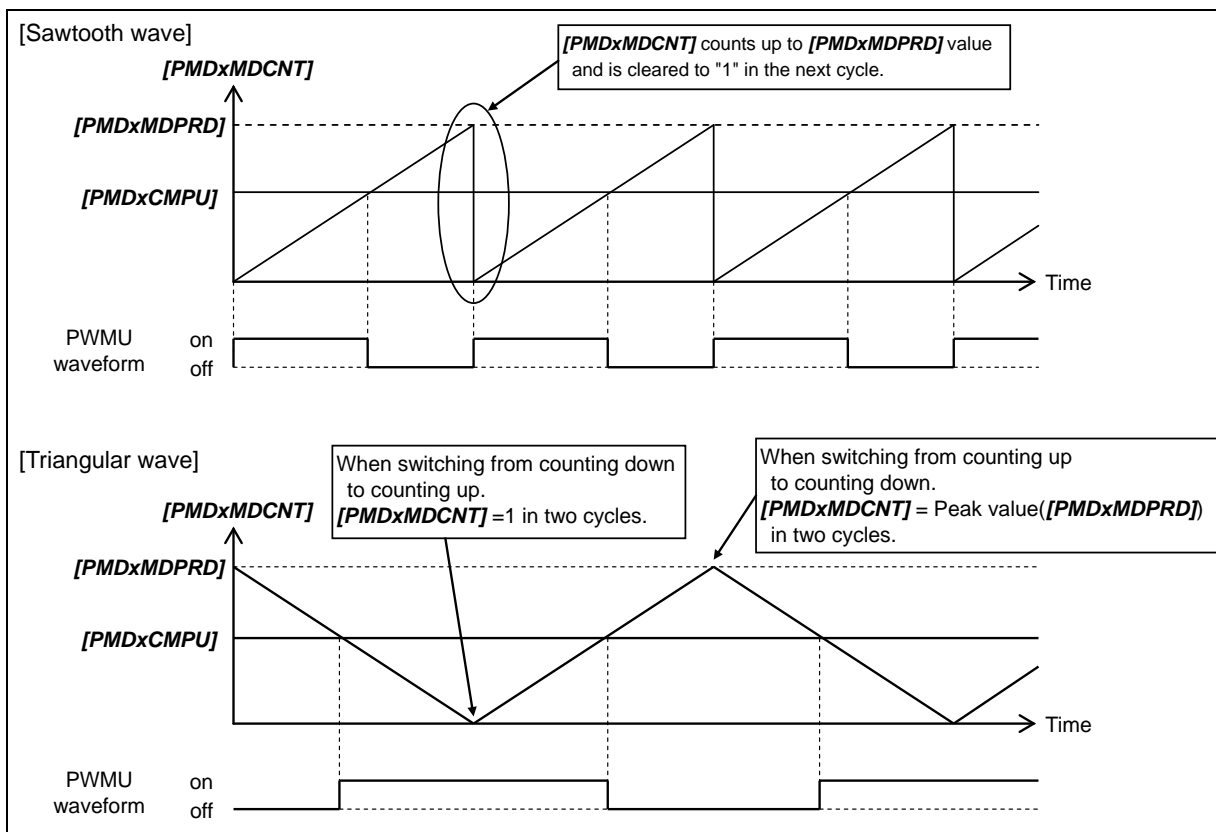


Figure 3.2 PWM Waveforms

When triangular wave carrier, the PWM waveform of each phase is selected from the center-aligned PWM, the falling edge fixed PWM and the rising edge fixed PWM by $[PMDxMDCR] \langle nPWMES \rangle$ ($n = U, V, W$) setting. (Refer to "Figure 3.3 Waveforms of PWM triangular wave carrier using fixed edge").

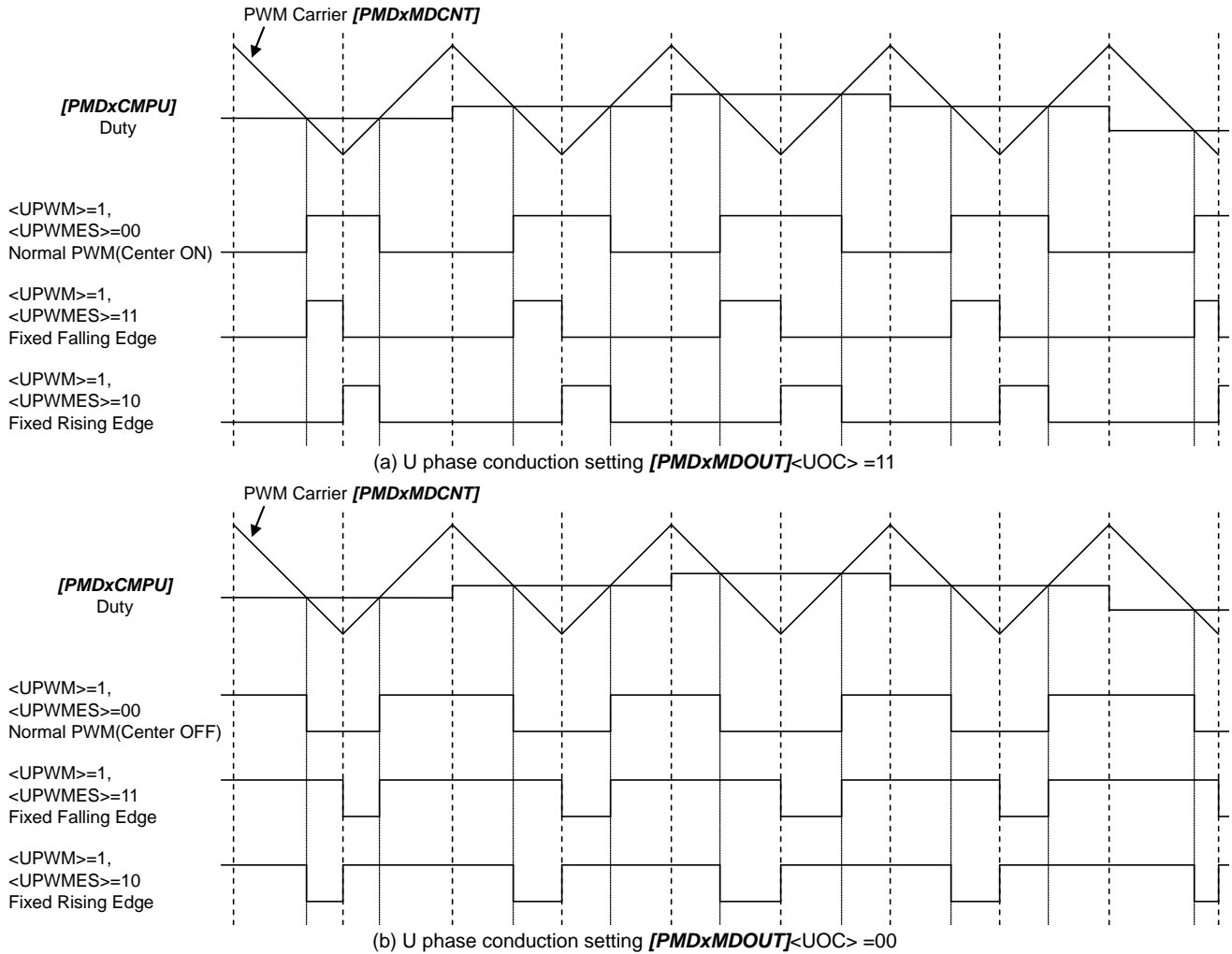


Figure 3.3 Waveforms of PWM triangular wave carrier using fixed edge

Also, PWM output of each phase of 3 phase PWM, can be switched between the center-on PWM and the center-off PWM with combination of $[PMDxMDOUT] \langle nOC \rangle$, $\langle nPWM \rangle$ ($n=U, V, W$), and $[PMDxMDCR] \langle SYNTMD \rangle$ (Refer to "3.3 Conduction Control Circuit").

3.2.3. Waveform mode

3-phase PWM waveforms can be generated in the following two modes by $[PMDxMDCR]<DTYMD>$ setting:

- 3-phase independent mode:

Each of the PWM compare registers for the three phases is set independently to generate independent PWM waveforms for each phase. This mode is used to generate drive waveforms such as sinusoidal waves.

- 3-phase common mode:

Only the U-phase PWM compare register is set to generate identical PWM waveforms for all the three phases. This mode is used for rectangular wave drive of brushless DC motors.

3.2.4. Interrupt processing

The pulse width modulation circuit generates PWM interrupt requests in synchronization with PWM waveforms. Interrupt request timing can be selected either at PWM carrier peak or at PWM carrier bottom.

The frequency of PWM interrupt can be set to half a PWM period, one PWM period, two PWM periods or four PWM periods.

3.3. Conduction Control Circuit

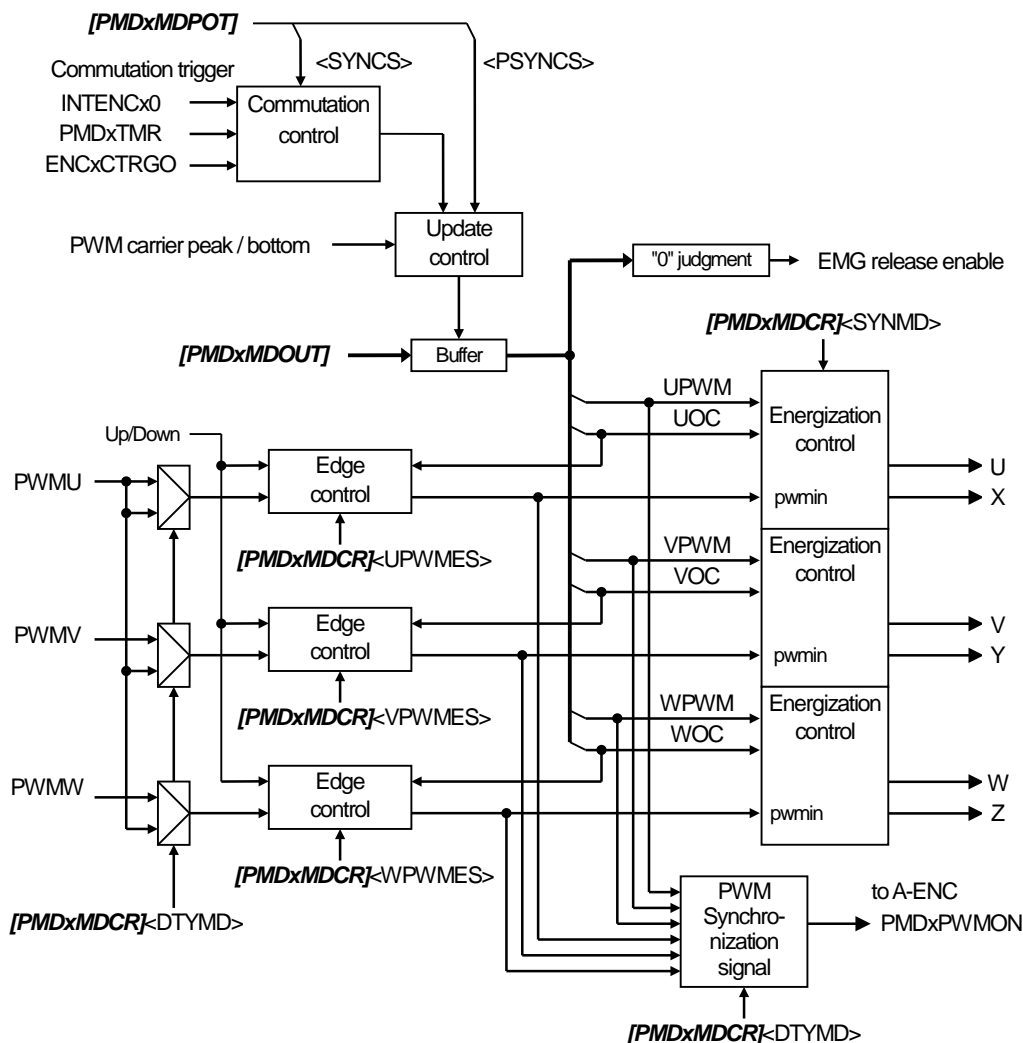


Figure 3.4 Conduction Control Circuit

The conduction control circuit performs the six phase outputs (U/X, V/Y, W/Z) control according to the settings made in the output control register $[PMDxMDOUT]$ and the output setting register $[PMDxMDPOT]$. $[PMDxMDOUT]$ register is double-buffered and update timing can be select as synchronous or asynchronous to PWM. Update timing synchronizing with trigger input from another peripheral function can also be selected. (For details of update timing, refer to "Table 3.1 $[PMDxMDOUT]$ buffer Update Timing".)

$\langle UPWM \rangle$, $\langle VPWM \rangle$, $\langle WPWM \rangle$ of the $[PMDxMDOUT]$ register selects PWM or High/Low output for each of the U/X, V/Y and W/Z phases. When PWM output is selected, PWM waveforms are output. When High/Low output is selected, output is fixed to either a High level or Low level. Each output is set to "High" or "Low" by $\langle UOC \rangle$, $\langle VOC \rangle$, $\langle WOC \rangle$ of the register $[PMDxMDOUT]$.

Refer to "Table 3.2 Decode circuit outputs according to $[PMDxMDOUT]$ and $[PMDxMDCR]$ $\langle SYNTMD \rangle$ setting" for six phase outputs control with the output control setting ($[PMDxMDOUT]$ and $[PMDxMDPOT]$), and the port output setting ($[PMDxMDCR]$ $\langle SYNTMD \rangle$).

In addition, using $[PMDxMDPOT]$ $\langle POLH \rangle$, $\langle POLL \rangle$, six output ports can be set to low-active or high-active on

upper-phase outputs (UOx,VOx,WOx) or lower-phase outputs (XOx,YOx,ZOx) respectively.

The conduction control circuit outputs a PWM signal (PWMON) to the encoder input circuit (A-ENC). The external input signal in the A-ENC is sampled synchronously with the PWMON.

Table 3.1 [PMDxMDOUT] buffer Update Timing

		[PMDxMDPOT]<PSYNCS> setting			
		00	01	10	11
[PMDxMDPOT] <SYNCS> setting	00	Constant update	PWM carrier bottom	PWM carrier peak	PWM carrier peak and PWM carrier bottom
	01	When INTENCx0 (Note2) is arisen	The first PWM carrier bottom every time when INTENCx0 (Note2) is arisen.	The first PWM carrier peak every time when INTENCx0 (Note2) is arisen.	Either the first PWM carrier peak or the first carrier bottom every time when INTENCx0(Note2) is arisen.
	10	When PMDxTMR (Note2) is arisen.	The first PWM carrier bottom every time when PMDxTMR (Note2) is arisen.	The first PWM carrier peak every time when PMDxTMR (Note2) is arisen.	Either the first PWM carrier peak or the first carrier bottom every time when PMDxTMR(Note2) is arisen.
	11	When ENCxCTRGO (Note2) is arisen.	The first PWM carrier bottom every time when ENCxCTRGO (Note2) is arisen.	The first PWM carrier peak every time when ENCxCTRGO (Note2) is arisen.	Either the first PWM carrier peak or the first carrier bottom every time when ENCxCTRGO (Note2) is arisen.

Note1: If PMD is disabled ([PMDxMDEN]<PWMEEN>=0), the retained trigger condition is cleared.

Note2: The connection destination depend on the product. For details, refer to "Product Information" of the reference manual.

Table 3.2 Decode circuit outputs according to [PMDxMDOUT] and [PMDxMDCR]<SYNTMD> setting

[PMDxMDCR]<SYNTMD>=0

		PWM output setting [PMDxMDOUT]<nPWM>			
		0: H/L output		1: PWM output	
		Upper-phase	Lower-phase	Upper-phase	Lower-phase
Conduction setting [PMDxMDOUT] <nOC>	00	Low	Low	PWM_N	PWM
	01	Low	High	Low	PWM
	10	High	Low	PWM	Low
	11	High	High	PWM	PWM_N

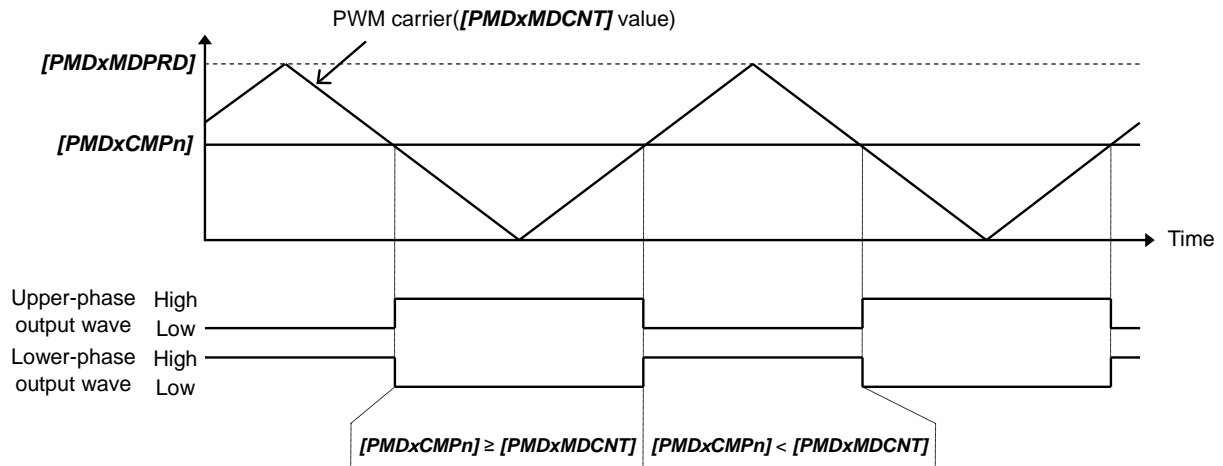
[PMDxMDCR]<SYNTMD>=1

		PWM output setting [PMDxMDOUT]<nPWM>			
		0: H/L output		1: PWM output	
		Upper-phase	Lower-phase	Upper-phase	Lower-phase
Conduction setting [PMDxMDOUT] <nOC>	00	Low	Low	PWM_N	PWM
	01	Low	High	Low	PWM_N
	10	High	Low	PWM	Low
	11	High	High	PWM	PWM_N

Note: n = U, V, W

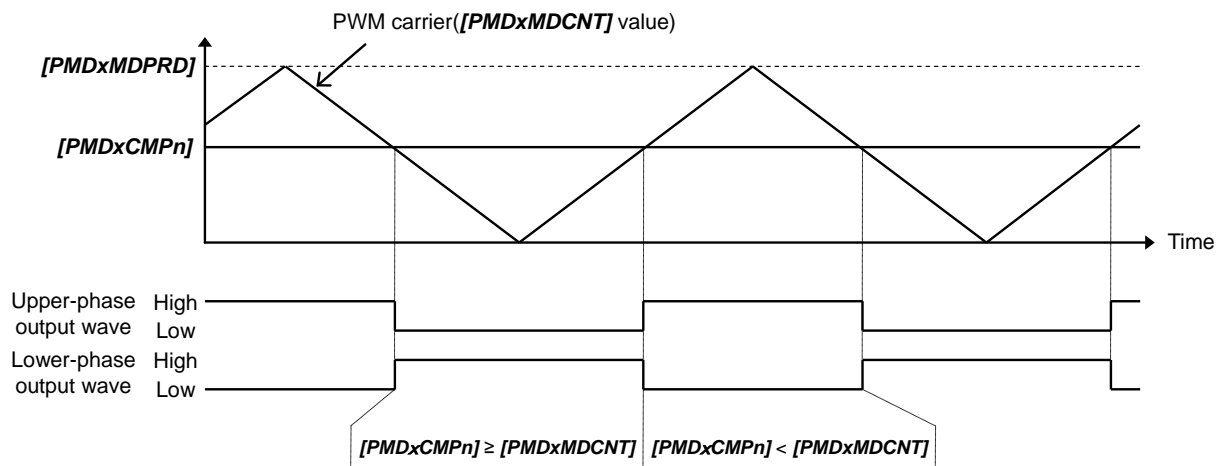
- Center-ON PWM

$[PMDxMDCR] < PWMMD > = 1$
 $[PMDxMDOUT] < nPWM > = 1$
 $[PMDxMDOUT] < nOC > = 11$



- Center-OFF PWM

$[PMDxMDCR] < PWMMD > = 1$
 $[PMDxMDOUT] < nPWM > = 1$
 $[PMDxMDOUT] < nOC > = 00$



3.4. Protection Control Circuit

The protection control circuit consists of a protection control unit and a protect output control unit.
 The protection control unit consists of the EMG protection control circuit and the OVV protection control circuit.

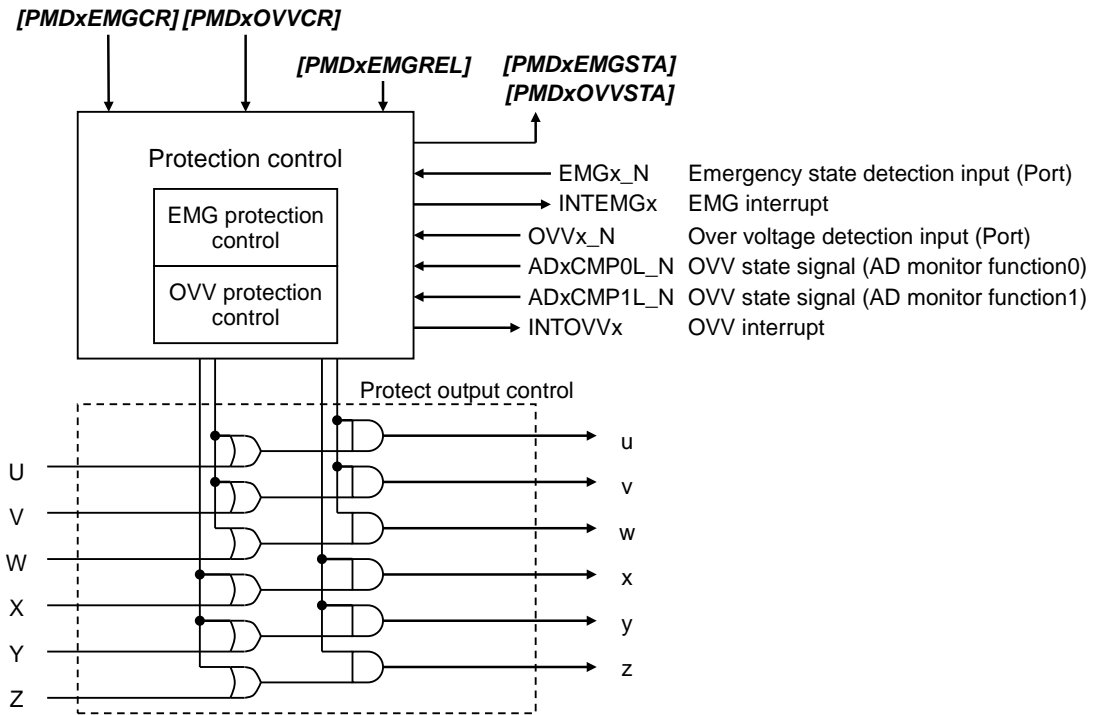


Figure 3.5 Protection Control Circuit

3.4.1. EMG Protection Circuit

The EMG protection circuit is a protection circuit for emergency stop . This circuit is activated when the EMGx_N input becomes "Low". EMG protection is set through the EMG Control Register (*[PMDxEMGCR]*).

Note: After reset, the EMG protection circuit is enabled.

- EMG input

The noise filter is inserted in the EMGx_N input. The noise detection time is selected with the EMG input detection time setting (*[PMDxEMGCR]*<EMGCNT>).

- EMG protection operation

The EMG protection circuit offers an emergency stop mechanism: when the EMGx_N input is asserted (H→L), all six port outputs are immediately disabled (depending on the *[PMDxEMGCR]*<EMGMD> setting) and an EMG interrupt (INTEMGx) is generated. <EMGMD> can be set to output a control signal that sets external output ports to High-impedance in case of an emergency. A read value of "1" in *[PMDxEMGSTA]*<EMGST> indicates that the EMG protection circuit is active.

- Release of the EMG protection

In the EMG protection state, it can be released by setting all the port output lines inactive (Set "0" to $[PMDxMDOUT]<UPWM>, <VPWM>, <WPWM>, <UOC>, <VOC>, <WOC>$.) (Note1) and then setting either $[PMDxEMGCR]<EMGRS>$ to "1". While the EMGx_N input is "Low", any attempt to release the EMG protection state is ignored. The EMG protection state can release after that confirming the status flag of $[PMDxEMGSTA]<EMGI>$ is "1".

Note1: The data of $[PMDxMDOUT]$ is necessary to be reflected in the subsequent stage buffer.

Note2: EMG release procedure after the reset deassertion.

After reset, the EMG function is enabled but EMGx_N pin is configured as a normal port. Therefore, as the EMG protection might be valid, release the EMG protection by the following procedure at the initial sequence.

- (1) Selects EMG function by the Port function register($[PxFRn]$).
- (2) Reads $[PMDxEMGSTA]<EMGI>$ to confirm it as "1".
- (3) Sets $[PMDxMDOUT]<UPWM>, <VPWM>, <WPWM>, <UOC>, <VOC>, <WOC>$ to "0" to make all ports in-active.
- (4) Releases EMG protection by setting $[PMDxEMGCR]<EMGRS>$ to "1".

- Disable of the EMG protection function

To disable the EMG protection function, write "0x5A" and "0xA5" in this order to the EMG release register ($[PMDxEMGREL]$) and then clear $[PMDxEMGCR]<EMGEN>$ to "0". These 3 instructions must be executed consecutively to prevent the EMG protection function from being inadvertently disabled.

3.4.2. OVV Protection Circuit

The OVV protection circuit is activated when the OVV input becomes "Low". This protection control is set by OVV control register (*[PMDxOVVCR]*).

- OVV input

The OVV input can be selected from the OVV_x_N pin and the OVV status signal (AD_xCMP0L_N, AD_xCMP1L_N) of the AD monitor function by *[PMDxOVVCR]* <OVVISEL>, <ADIN0EN>, and <ADIN1EN>.

The noise filter is inserted in the OVV input. The noise detection time is selected with the OVV input detection time setting (*[PMDxOVVCR]*<OVVCNT>). The noise filter is valid only when the OVV_x_N pin is selected (<OVVISEL> = 0).

- OVV protection operation

OVV protection circuit fixes 6 port outputs in the port output disable unit to High level or Low level, when OVV input is active continuously for a predetermined interval time (set by <OVVCNT>). And OVV interrupt (INTOVV_x) is generated. *[PMDxOVVCR]*<OVVMD> setting selects from among Lower-phases OFF/Upper-phases ON, Upper-phases OFF/Lower-phases ON, and all phases OFF.

A read value of "1" in *[PMDxOVVSTA]*<OVVST> indicates that the OVV protection circuit is active.

- Release of the OVV protection

The release of the OVV protection state is enabled by setting *[PMDxOVVCR]*<OVVRS> to "1". And after the OVV input becomes inactive, the OVV protection is automatically released at a predetermined timing. (While the OVV input is "Low", any attempt to release the OVV protection state is ignored. The state of the OVV input can be checked by reading *[PMDxOVVSTA]*<OVVVI>)

The OVV protection state is released in synchronization with the PWM period (at the timing when PWM count (*[PMDxMDCNT]*) matches *[PMDxMDPRD]*). However if an interrupt on a half period of PWM is set, the protection state is released when PWM count is "0x0001" or matches *[PMDxMDPRD]*).

- Disable of the OVV protection function

In order to disable OVV function, EMG release register *[PMDxEMGREL]* should be set to "0x5A" and next, "0xA5". Then *[PMDxOVVCR]*<OVVEN> should be set to "0". These 3 instructions should be executed continuously to prevent the OVV protection function from being inadvertently disabled.

3.4.3. Protection control when using the debug tool

When using the debug tool, PMD output ports can be disabled when CPU is stopped by the debug halt.

In the debug halt, whether the port output becomes High-impedance or PMD output is selected by *[PMDxPORTMD]*<PORTMD> setting.

3.5. Dead time Control Circuit

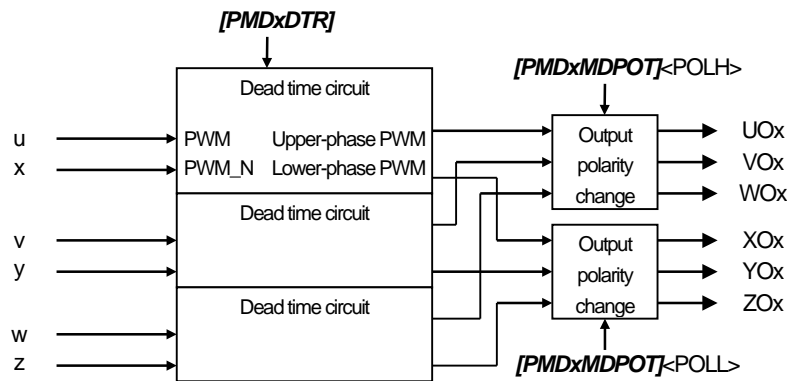


Figure 3.6 Dead time Control Circuit

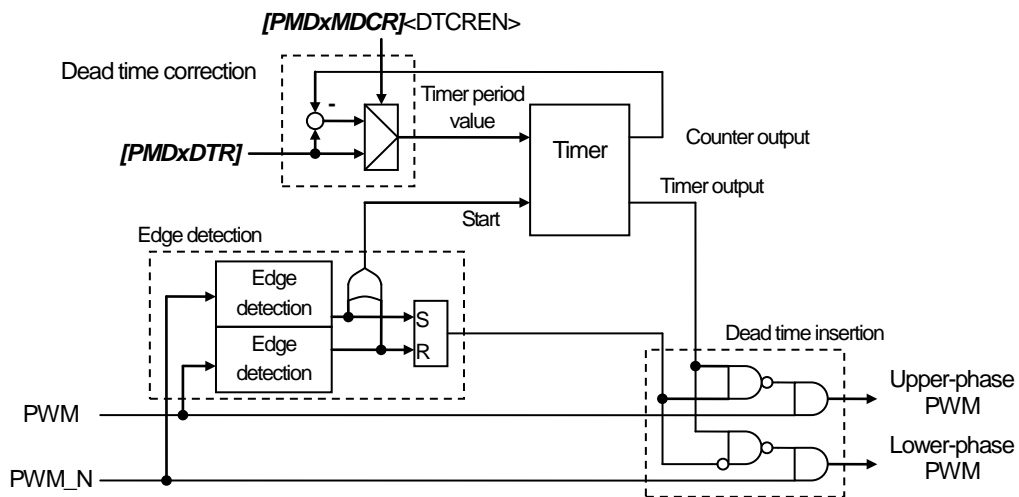


Figure 3.7 Dead time circuit

The dead time control circuit consists of a dead time circuit and an output polarity switching circuit. The dead time unit consists of the edge detection block, timer block, dead time insert block, and dead time correction block. (Refer to "Figure 3.7 Dead time circuit")

For each of the U-, V-, and W-phases, the dead-time units delay the ON-timing of each phase when the upper-phase and lower-phase are switched to prevent a short circuit. The dead time is set to the Dead time Register (*[PMDxDTR]*) as an 8-bit value with a resolution of $8/f_{sys}$ can be set.

The output polarity switching circuit allows the polarity (active high or active low) of the upper-output (UOx, VOx, WOx) and lower-output (XOx, YOx, ZOx) phases to be independently set through PMD output setting register *[PMDxMDPOT]<POLH>* and *<POLL>*.

In the dead time correction block, when one of the on-period of the upper PWM or the lower PWM is 0 width, if *[PMDxMDCR]<DTCREN>* is set to "1", the other PWM delay time is corrected to be shortened. If the PWM signal is OFF during the dead time period, the delay time of the counter phase is shortened in the rest of dead time (dead time register setting time - ON time). When the upper PWM becomes OFF during the dead time period, the delay time of the lower PWM should be corrected to be shortened. When the lower PWM becomes OFF during the dead time period, the delay time of the upper PWM should be corrected to be shortened. Figure 3.8 shows

dead time correction. A delay time is corrected in the vicinity of duty of 100% of the upper PWM and it also is corrected in the vicinity of duty of 0%.

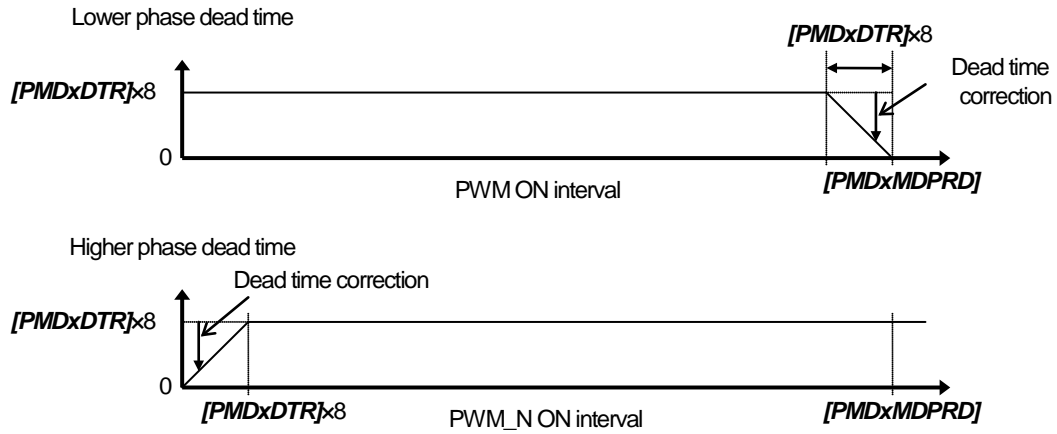


Figure 3.8 Dead time correction

3.6. Synchronous Trigger Generation Circuit

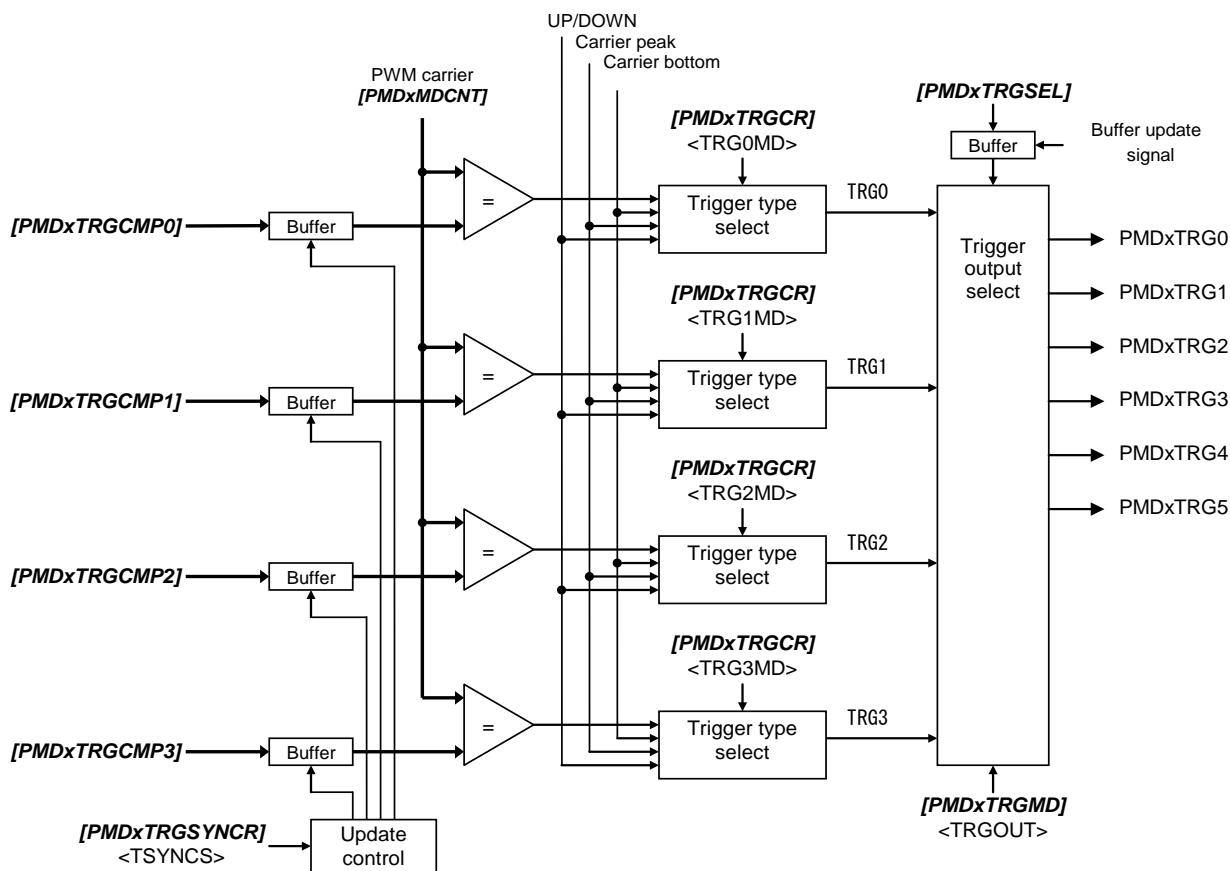


Figure 3.9 Synchronous Trigger Generation Circuit

The synchronous trigger generation circuit generates four trigger signals (TRG0 to TRG3) for starting ADC sampling in synchronization with PWM.

The trigger timing can be selected following 6 types.

- (1) At up count operation compare-match (Note1)(Note2)
- (2) At down count operation compare-match (Note1)(Note3)
- (3) At up/down count operation compare-match (Note1)(Note3)(Note4)
- (4) PWM carrier peak
- (5) PWM carrier bottom(Note3)
- (6) PWM carrier peak and PWM carrier bottom(Note3)

Note1: The compare-match is a match between $[PMDxMDCNT]$ and $[PMDxTRGCMPn]$ ($n=0$ to 3).

Note2: If PWM is started ($\langle PWMMEN \rangle = 1$) while $[PMDxTRGCMPn]$ ($n=0$ to 3) is set to "0x0001" with saw-tooth wave carrier ($\langle PWMMMD \rangle = 0$), there is no trigger output in the first PWM cycle.

Note3: When saw-tooth wave carrier ($\langle PWMMMD \rangle = 0$) is selected, it cannot be selected.

Note4: When trigger output at up/down-count match, $[PMDxTRGCMPn]$ ($n=0$ to 3) = 0x0001 and triangular wave ($\langle PWMMMD \rangle = 1$), one trigger output is made per period.

In the trigger selection output mode $[PMDxTRGMD]\langle TRGOUT \rangle = 1$, the TRG0 signal is output from ADC synchronous sampling output ($[PMDxTRG0]$ to $[PMDxTRG5]$) selected by the trigger output selection register $[PMDxTRGSEL]$. The TRG0 setting is set by $[PMDxTRGCMP0]$ and $[PMDxTRGCR]\langle TRG0MD \rangle$. (Refer to "Table 4.4 Trigger Output Patterns".)

When $[PMDxTRGMD]\langle EMGTGE \rangle = 1$, this circuit outputs trigger signals in EMG protection state.

An example of using the synchronization trigger generation circuit is shown below.

- In the case of 3-shunt

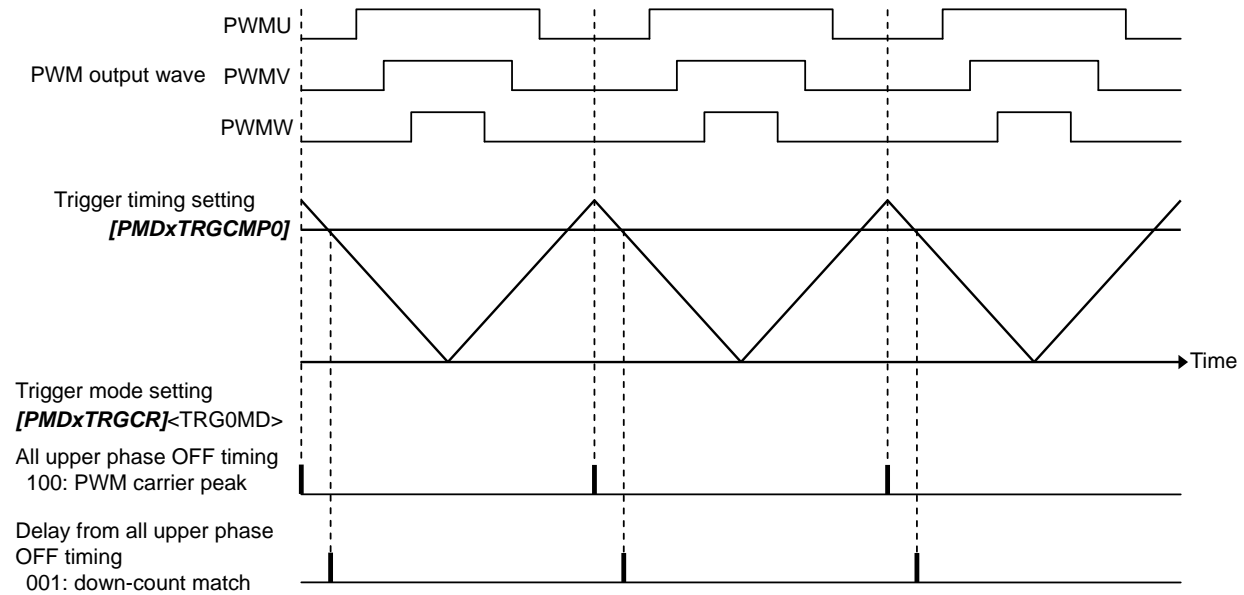


Figure 3.10 Example of using the PMD trigger at 3-shunt

Trigger output mode setting ($[PMDxTRGMD]\langle TRGOUT \rangle$) is set to "1" (Trigger selection output).

Trigger mode setting 0 ($[PMDxTRGCR]\langle TRG0MD \rangle$) is set to "100" (Trigger output at PWM carrier peak), when trigger is generated at the timing of all upper-phases OFF. Trigger mode setting 1 ($[PMDxTRGCR]\langle TRG1MD \rangle$) is set to "001" (Trigger output at down-count match) and $[PMDxTRGCMP0]$ is set to delay timing, when delayed trigger is generated at the timing of all upper-phases OFF.

By setting trigger output selection register ($[PMDxTRGSEL]\langle TRGSEL \rangle$) according to the position (sector) of the motor, it is possible to generate six kinds of triggers for each sector.

- In the case of 1-shunt

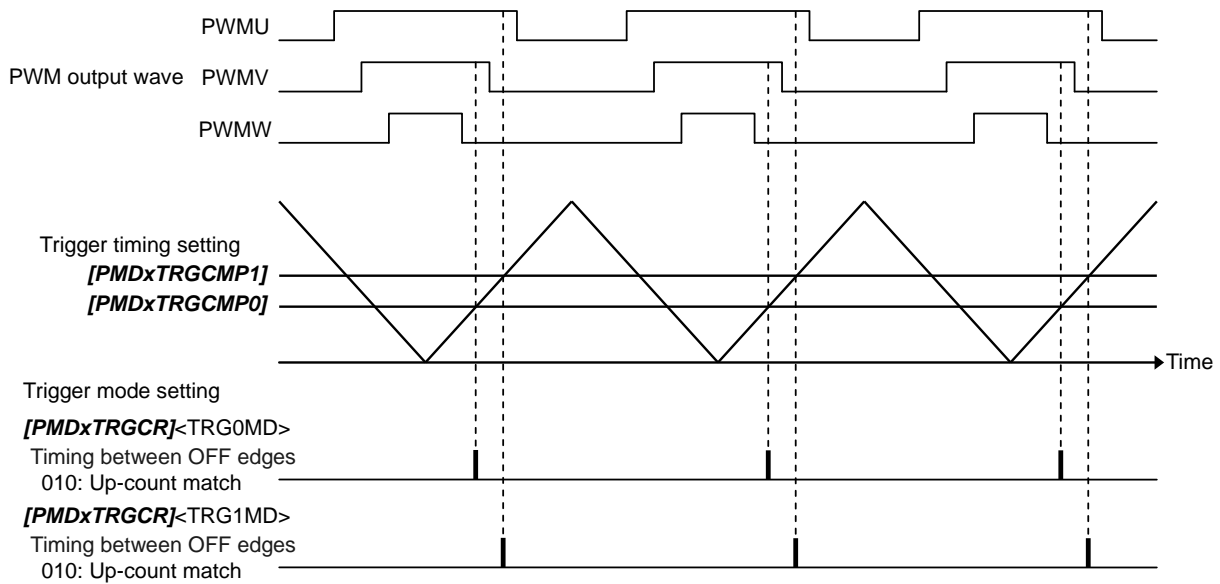


Figure 3.11 Example of using the PMD trigger at 1-shunt

Trigger output mode setting ($[PMDxTRGMD]<TRGOUT>$) is set to "0"(Trigger fixed output).

Trigger mode setting 0 and 1($[PMDxTRGCR]<TRG0MD>,<TRG1MD>$) is set to "010"(Trigger output at up-count match), when trigger is generated at the timing between OFF edges. Or trigger mode setting 0 and 1($<TRG0MD>,<TRG1MD>$) is set to "001"(Trigger output at down-count match), when trigger is generated at the timing between ON edges.

The previous trigger is set to $[PMDxTRGCMP0]$, and the subsequent trigger is set to $[PMDxTRGCMP1]$.

4. Registers

4.1. List of Registers

The following table lists the control registers and their addresses:

Peripheral Function Name		Channel/Unit	Base Address		
			TYPE1	TYPE2	TYPE3
Programmable Motor Control Circuit Plus	PMD+	ch0	0x400F6000	0x400E9000	0x40089000
		ch1	0x400F6100	0x400E9400	0x40089400
		ch2	0x400F6200	0x400E9800	0x40089800
		ch3	-	0x400E9C00	0x40089C00

Note: The Channel/Unit and Base address type are different by products. Please refer to "Product Information" of the reference manual for the details.

Register Name		Address(Base+)
PMD Enable Register	[PMDxMDEN]	0x0000
Port Output Mode Register	[PMDxPORTMD]	0x0004
PMD Control Register	[PMDxMDCR]	0x0008
PWM Counter Status Register	[PMDxCNTSTA]	0x000C
PWM Counter Register	[PMDxMDCNT]	0x0010
PWM Period Register	[PMDxMDPRD]	0x0014
PMD Compare U Register	[PMDxCMPU]	0x0018
PMD Compare V Register	[PMDxCMPV]	0x001C
PMD Compare W Register	[PMDxCMPW]	0x0020
Reserved	-	0x0024
PMD Conduction Control Register	[PMDxMDOUT]	0x0028
PMD Output Setting Register	[PMDxMDPOT]	0x002C
EMG Release Register	[PMDxEMGREL]	0x0030
EMG Control Register	[PMDxEMGCR]	0x0034
EMG Status Register	[PMDxEMGSTA]	0x0038
OVV Control Register	[PMDxOVVCR]	0x003C
OVV Status Register	[PMDxOVVSTA]	0x0040
Dead time Register	[PMDxDTR]	0x0044
Trigger Compare 0 Register	[PMDxTRGCMP0]	0x0048
Trigger Compare 1 Register	[PMDxTRGCMP1]	0x004C
Trigger Compare 2 Register	[PMDxTRGCMP2]	0x0050
Trigger Compare 3 Register	[PMDxTRGCMP3]	0x0054
Trigger Control Register	[PMDxTRGCR]	0x0058
Trigger Output Mode Setting Register	[PMDxTRGMD]	0x005C
Trigger Output Selection Register	[PMDxTRGSEL]	0x0060
Trigger Update Timing Setting Register	[PMDxTRGSYNCR]	0x0064

4.2. Details of Registers

4.2.1. [PMDxMDEN] (PMD Enable Register)

Bit	Bit Symbol	After reset	Type	Function
31:1	-	0	R	Read as "0".
0	PWMEN	0	R/W	Enables or disables waveform synthesis. (Note1) (Note2) 0: Disable 1: Enable

Note1: When the port is set to a function output (PMD output), the port disables output (High-impedance) by setting <PWMEN>=0. For details of a port setting, refer to "Input/Output Ports" of the reference manual.

Note2: <PWMEN>=1 should be set after initial settings other than <PWMEN> like an output polarity are set.

4.2.2. [PMDxPORTMD] (Port Output Mode Register)

Bit	Bit Symbol	After reset	Type	Function
31:2	-	0	R	Read as "0".
1:0	PORTMD[1:0]	00	R/W	Port control setting when a debug halt occurs (Note1) (Note2) (Note3) 00: Upper-phases High-impedance / lower-phases High-impedance 01: Upper-phases High-impedance / lower-phases PMD output 10: Upper-phases PMD output / lower-phases High-impedance 11: Upper-phases PMD output / lower-phases PMD output Sets the port output for both upper-phases (UOx/VOx/WOx) and the lower-phases (XOx/YOx/ZOx) when a debug halt occurs in the use of ports for function output (PMD output). When a debug halt occurs while High-impedance is selected, the ports are disabled to output (High-impedance). In other cases, external port outputs depend on PMD outputs. (Note3)

Note1: When <PWMEN>=0, output ports are disabled to output (High-impedance) regardless of the <PORTMD[1:0]> setting.

Note2: Depending on the setting of [PMDxEMGCR]<EMGMD[1: 0]>, port output control is also performed during EMG protection.

Note3: For details of a port setting, refer to "Input/Output Ports" of the reference manual..

4.2.3. [PMDxMDCR] (PMD Control Register)

Bit	Bit Symbol	After reset	Type	Function
31:16	-	0	R	Read as "0".
15:14	WPWMES[1:0]	00	R/W	W-phase edge setting (Note1) 00: Edge unfixed (center-aligned PWM) 01: Reserved 10: PWM rising-edge fixed (to the PWM carrier bottom) 11: PWM falling-edge fixed (to the PWM carrier bottom)
13:12	VPWMES[1:0]	00	R/W	V-phase edge setting (Note1) 00: Edge unfixed (center-aligned PWM) 01: Reserved 10: PWM rising-edge fixed (to the PWM carrier bottom) 11: PWM falling-edge fixed (to the PWM carrier bottom)
11:10	UPWMES[1:0]	00	R/W	U-phase edge setting (Note1) 00: Edge unfixed (center-aligned PWM) 01: Reserved 10: PWM rising-edge fixed (to the PWM carrier bottom) 11: PWM falling-edge fixed (to the PWM carrier bottom)
9:8	DSYNCS[1:0]	00	R/W	Double-buffer update timing for the PWM compare register and PWM period register. (Note2)(Note3) 00: Depends on interrupt period setting (refer to the Table 4.1) Updates at the carrier peak and carrier bottom when 0.5 PWM period is selected (<INTPRD>=00). Otherwise, updates at the carrier peak. 01: Updates at PWM carrier bottom 10: Updates at PWM carrier peak 11: Updates at both PWM carrier peak and bottom
7	DTCREN	0	R/W	Set a dead time correction. 0: Disable 1: Enable
6	PWMCK	0	R/W	PWM period extension mode 0: Normal period 1: 4 x period Sets the counting period of the PWM counter. Normal period setting: Saw-tooth wave 1/fsys / Triangular wave 2/fsys 4 x period setting: Saw-tooth wave 4/fsys / Triangular wave 8/fsys
5	SYNTMD	0	R/W	Port output mode setting Port outputs are controlled by a combination of [PMDxMDOUT] <nOC>, <nPWM>, [PMDxMDPOT] <POLH>, <POLL> and <SYNTMD> (refer to Table 4.2).
4	DTYMD	0	R/W	Duty mode selection 0: 3-phase common mode 1: 3-phase independent mode This bit selects whether to make duty setting independently for each phase or to use the [PMDxCMPU] register as 3-phase common.

Bit	Bit Symbol	After reset	Type	Function
3	PINT	0	R/W	PWM interrupt request timing selection (Note4)(Note5) 0: Interrupt request occurs at PWM carrier bottom ($[PMDxMDCNT]=0x0001$). 1: Interrupt request occurs at PWM carrier peak ($[PMDxMDCNT] = [PMDxMDPRD]$).
2:1	INTPRD[1:0]	00	R/W	PWM interrupt request period selection 00: Interrupt request at every 0.5 PWM period (Note6)(Note7) 01: Interrupt request at every PWM period 10: Interrupt request at every two PWM periods 11: Interrupt request at every four PWM periods This field selects the PWM interrupt request period from 0.5 PWM period, one PWM period, two PWM periods and four PWM periods.
0	PWMMD	0	R/W	PWM carrier waveform selection 0: PWM mode 0 (edge-aligned PWM and saw-tooth wave) 1: PWM mode 1(center-aligned PWM and triangular wave)

Note1: Valid when triangular carrier PWM is selected ($\langle PWMMD \rangle = 1$).

Note2: Updates at carrier peak when saw-tooth wave carrier is selected ($\langle PWMMD \rangle = 0$) regardless of the setting.

Note3: When $[PMDxMDEN] \langle PWMEN \rangle = 0$, updates asynchronously regardless of setting.

Note4: Interrupt request occurs at carrier peak when the PWM carrier is saw-tooth wave ($\langle PWMMD \rangle = 0$).

Note5: Interrupt request occurs both at carrier peak and carrier bottom when the interrupt period is 0.5 period ($\langle INTPRD \rangle = 00$).

Note6: PWM interrupt request period can be configured only when the PWM carrier is triangular wave ($\langle PWMMD \rangle = 1$)

Note7: The subsequent stage of the double-buffer of the compare registers ($[PMDxCMPU/V/W]$) and the period register ($[PMDxMDPRD]$) are updated by peak and bottom of the PWM carrier.

Table 4.1 $[PMDxMDPRD]$, $[PMDxCMPU/V/W]$ buffer Update Timing

Settings		Update Timing
$\langle DSYNCS \rangle$	$\langle INTPRD \rangle$	
00	1x	Updates at PWM carrier peak
	x1	Updates at PWM carrier peak
	00	Updates at PWM carrier peak and PWM carrier bottom
01	xx	Updates at PWM carrier bottom
10	xx	Updates at PWM carrier peak
11	xx	Updates at PWM carrier peak and PWM carrier bottom

Note: x: Don't care

4.2.4. $[PMDxCNTSTA]$ (PWM Counter Status Register)

Bit	Bit Symbol	After reset	Type	Function
31:1	-	0	R	Read as "0".
0	UPDWN	0	R	PWM counter flag (Note) 0: Up-counting 1: Down-counting This bit indicates whether the PWM counter is up-counting or down-counting.

Note: The PWM carrier is a saw-tooth wave ($[PMDxMDCR] \langle PWMMD \rangle = 0$), a zero is always read.

4.2.7. [PMDxCMPU] (PWM Compare U Register)

Bit	Bit Symbol	After reset	Type	Function
31:16	-	0	R	Read as "0".
15:0	CMPU[15:0]	0x0000	R/W	<p>PWM pulse width of U Phase (Note1) 0x0000 through 0xFFFF</p> <p><CMPU> are compare registers for determining the output pulse width of the U-phase. These registers are double-buffered. Pulse width is determined by comparing the subsequent stage buffer and the PWM counter to evaluate which is small or large.</p> <p>By the combination of the PWM period extension mode ([PMDxMDCR]<PWMCK>) and the PWM carrier waveform ([PMDxMDCR]<PWMMMD>), the pulse width can be calculated as follows:</p> <p>When <PWMCK>=0, <PWMMMD>=0: $[PMDxCMPU] \times 1/fsys$ <PWMMMD>=1: $[PMDxCMPU] \times 2/fsys$</p> <p>When <PWMCK>=1, <PWMMMD>=0: $[PMDxCMPU] \times 4/fsys$ <PWMMMD>=1: $[PMDxCMPU] \times 8/fsys$</p>

Note1: When $[PMDxCMPU] > [PMDxMDPRD]$, the duty is 100%.

Note2: Do not write to this register in byte unit. If the upper 8 bits [15:8] and the lower 8 bits [7:0] are written separately, operation cannot be guaranteed.

Note3: Since the [PMDxCMPU] register is double-buffered, the PWM pulse width can be changed during the operation of the PWM counter.

Note4: For detailed update timing of the subsequent stage buffer, refer to the "Table 4.1 [PMDxMDPRD],[PMDxCMPU/V/W] buffer Update Timing".

Note5: Read value is the first buffer value (the latest data set via a bus).

4.2.8. [PMDxCMPV] (PWM Compare V Register)

Bit	Bit Symbol	After reset	Type	Function
31:16	-	0	R	Read as "0".
15:0	CMPV[15:0]	0x0000	R/W	<p>PWM pulse width of V Phase (Note1) 0x0000 through 0xFFFF</p> <p><CMPV> are compare registers for determining the output pulse width of the V-phase. These registers are double-buffered. Pulse width is determined by comparing the subsequent stage buffer and the PWM counter to evaluate which is small or large.</p> <p>By the combination of the PWM period extension mode ([PMDxMDCR]<PWMCK>) and the PWM carrier waveform ([PMDxMDCR]<PWMMMD>), the pulse width can be calculated as follows:</p> <p>When <PWMCK>=0, <PWMMMD>=0: $[PMDxCMPV] \times 1/fsys$ <PWMMMD>=1: $[PMDxCMPV] \times 2/fsys$</p> <p>When <PWMCK>=1, <PWMMMD>=0: $[PMDxCMPV] \times 4/fsys$ <PWMMMD>=1: $[PMDxCMPV] \times 8/fsys$</p>

Note1: When $[PMDxCMPV] > [PMDxMDPRD]$, the duty is 100%.

Note2: Do not write to this register in byte unit. If the upper 8 bits [15:8] and the lower 8 bits [7:0] are written separately, operation cannot be guaranteed.

Note3: Since the [PMDxCMPV] register is double-buffered, the PWM pulse width can be changed during the operation of the PWM counter.

Note4: For detailed update timing of the subsequent stage buffer, refer to the "Table 4.1 [PMDxMDPRD],[PMDxCMPU/V/W] buffer Update Timing".

Note5: Read value is the first buffer value (the latest data set via a bus).

4.2.9. [PMDxCMPW] (PWM Compare W Register)

Bit	Bit Symbol	After reset	Type	Function
31:16	-	0	R	Read as "0".
15:0	CMPW[15:0]	0x0000	R/W	<p>PWM pulse width of W Phase (Note1) 0x0000 through 0xFFFF</p> <p><CMPW> are compare registers for determining the output pulse width of the W-phase. These registers are double-buffered. Pulse width is determined by comparing the subsequent stage buffer and the PWM counter to evaluate which is small or large.</p> <p>By the combination of the PWM period extension mode ([PMDxMDCR]<PWMCK>) and the PWM carrier waveform ([PMDxMDCR]<PWMMMD>), the pulse width can be calculated as follows:</p> <p>When <PWMCK>=0, <PWMMMD>=0: $[PMDxCMPW] \times 1/f_{sys}$ <PWMMMD>=1: $[PMDxCMPW] \times 2/f_{sys}$</p> <p>When <PWMCK>=1, <PWMMMD>=0: $[PMDxCMPW] \times 4/f_{sys}$ <PWMMMD>=1: $[PMDxCMPW] \times 8/f_{sys}$</p>

Note1: When $[PMDxCMPW] > [PMDxMDPRD]$, the duty is 100%.

Note2: Do not write to this register in byte unit. If the upper 8 bits [15:8] and the lower 8 bits [7:0] are written separately, operation cannot be guaranteed.

Note3: Since the [PMDxCMPW] register is double-buffered, the PWM pulse width can be changed during the operation of the PWM counter.

Note4: For detailed update timing of the subsequent stage buffer, refer to the "Table 4.1 [PMDxMDPRD],[PMDxCMPU/V/W] buffer Update Timing".

Note5: Read value is the first buffer value (the latest data set via a bus).

4.2.10. [PMDxMDPOT] (PMD Output Setting Register)

Bit	Bit Symbol	After reset	Type	Function
31:10	-	0	R	Read as "0".
9:8	SYNCS[1:0]	00	R/W	Selects [PMDxMDOUT] transfer timing (trigger synchronous setting). (Note2)(Note3) 00: asynchronous(Note4) 01: when INTENCx0 (A-ENCx interrupt request)(Note6) occurs 10: when PMDxTMR (Timer interrupt request)(Note6) occurs 11: when ENCxCTRGO (A-ENCx MCMP completed)(Note6) occurs Selects the subsequent stage buffer update timing of the conduction control register.
7:4	-	0	R	Read as "0".
3	POLH	0	R/W	Selects the output polarity of the upper-phase outputs (UOx, VOx, WOx). 0: Active low 1: Active high
2	POLL	0	R/W	Selects the output polarity of the lower-phase outputs (XOx, YOx, ZOx). 0: Active low 1: Active high
1:0	PSYNCS[1:0]	00	R/W	Selects [PMDxMDOUT] transfer timing (PWM synchronous setting). (Note2)(Note3)(Note5) 00: asynchronous to PWM (Note4) 01: Carrier bottom (when [PMDxMDCNT] = 0x0001) 10: Carrier peak ([PMDxMDCNT] = [PMDxMDPRD]) 11: Carrier peak and carrier bottom Selects the subsequent stage buffer update timing of the conduction control register.

Note1: This register must be set while [PMDxMDEN]<PWMEN>=0.

Note2: By the combination of the settings for <PSYNCS> and <SYNCS>, the buffer update timing can be determined (refer to the "Table 3.1 [PMDxMDOUT] buffer Update Timing").

Note3: When PMD is disabled ([PMDxMDEN]<PWMEN>=0), the timing is asynchronous regardless of settings.

Note4: When <SYNCS> and <PSYNCS> are set to "0", the setting is applied to the port output at the same time that the [PMDxMDOUT] registers.

Note5: When the PWM carrier is saw-tooth wave, the buffer update timing is the carrier peak, except <PSYNCS>=00

Note6: The connection destination depend on the product. For details, refer to "Product Information" of the reference manual.

4.2.11. [PMDxMDOUT] (PMD Conduction Control Register)

Bit	Bit Symbol	After reset	Type	Function
31:11	-	0	R	Read as "0".
10	WPWM	0	R/W	W-phase PWM output setting 0: High/Low Output 1: PWM Output Port output is controlled by the combination of <WOC>, <WPWM>, [PMDxMDPOT]<POLH>, <POLL> and [PMDxMDCR] <SYNTMD> (refer to the Table 4.2).
9	VPWM	0	R/W	V-phase PWM output setting 0: High/Low Output 1: PWM Output Port output is controlled by the combination of <VOC>, <VPWM>, [PMDxMDPOT]<POLH>, <POLL> and [PMDxMDCR] <SYNTMD> (refer to the Table 4.2).
8	UPWM	0	R/W	U-phase PWM output setting 0: High/Low Output 1: PWM Output Port output is controlled by the combination of <UOC>, <UPWM>, [PMDxMDPOT]<POLH>, <POLL> and [PMDxMDCR] <SYNTMD> (refer to the Table 4.2).
7:6	-	0	R	Read as "0".
5:4	WOC[1:0]	00	R/W	W-phase conduction control setting Port output is controlled by the combination of <WOC>, <WPWM>, [PMDxMDPOT]<POLH>, <POLL> and [PMDxMDCR] <SYNTMD> (refer to the Table 4.2).
3:2	VOC[1:0]	00	R/W	V-phase conduction control setting Port output is controlled by the combination of <VOC>, <VPWM>, [PMDxMDPOT]<POLH>, <POLL> and [PMDxMDCR] <SYNTMD> (refer to the Table 4.2).
1:0	UOC[1:0]	00	R/W	U-phase conduction control setting Port output is controlled by the combination of <UOC>, <UPWM>, [PMDxMDPOT]<POLH>, <POLL> and [PMDxMDCR] <SYNTMD> (refer to the Table 4.2).

Note1: Do not write to this register in byte unit. If the upper 8 bits [15:8] and the lower 8 bits [7:0] are written separately, operation cannot be guaranteed.

Note2: Since the conduction control register is double-buffered, the setting value can be changed during the operation of the PWM counter.

Note3: For detailed update timing of the subsequent stage buffer, refer to the "Table 3.1 [PMDxMDOUT] buffer Update Timing".

Note4: Read value is the first buffer value (the latest data set via a bus).

Table 4.2 Port Outputs according to [PMDxMDOUT] and [PMDxMDCR]<SYNTMD> settings

[PMDxMDCR]<SYNTMD>=0

Polarity: Active high ([PMDxMDPOT]<POLH><POLL>=11)

		PWM output setting [PMDxMDOUT]<nPWM>			
		0: H/L output		1: PWM output	
		Upper phase	Lower phase	Upper phase	Lower phase
Conduction control setting [PMDxMDOUT] <nOC>	00	L	L	/PWMn	PWMn
	01	L	H	L	PWMn
	10	H	L	PWMn	L
	11	H	H	PWMn	/PWMn

[PMDxMDCR]<SYNTMD>=0

Polarity: Active low ([PMDxMDPOT]<POLH><POLL>=00)

		PWM output setting [PMDxMDOUT]<nPWM>			
		0: H/L output		1: PWM output	
		Upper phase	Lower phase	Upper phase	Lower phase
Conduction control setting [PMDxMDOUT] <nOC>	00	H	H	PWMn	/PWMn
	01	H	L	H	/PWMn
	10	L	H	/PWMn	H
	11	L	L	/PWMn	PWMn

[PMDxMDCR]<SYNTMD>=1

Polarity: Active high ([PMDxMDPOT]<POLH><POLL>=11)

		PWM output setting [PMDxMDOUT]<nPWM>			
		0: H/L output		1: PWM output	
		Upper phase	Lower phase	Upper phase	Lower phase
Conduction control setting [PMDxMDOUT] <nOC>	00	L	L	/PWMn	PWMn
	01	L	H	L	/PWMn
	10	H	L	PWMn	L
	11	H	H	PWMn	/PWMn

[PMDxMDCR]<SYNTMD>=1

Polarity: Active low ([PMDxMDPOT]<POLH><POLL>=00)

		PWM output setting [PMDxMDOUT]<nPWM>			
		0: H/L output		1: PWM output	
		Upper phase	Lower phase	Upper phase	Lower phase
Conduction control setting [PMDxMDOUT] <nOC>	00	H	H	PWMn	/PWMn
	01	H	L	H	PWMn
	10	L	H	/PWMn	H
	11	L	L	/PWMn	PWMn

Note1: n = U, V, W

Note2: PWMn: PWM signal of PWM compare setting /PWMn: Inversion signal of PWMn

4.2.12. [PMDxEMGREL] (EMG Release Register)

Bit	Bit Symbol	After reset	Type	Function
31:8	-	0	R	Read as "0".
7:0	EMGREL[7:0]	0x00	W	EMG/OVV disable code 0x5A, 0xA5: Disable code. Except 0x5A, 0xA5: Don't care. The EMG and OVV protection functions can be disabled by setting "0x5A" and "0xA5" in this order to register. After writing disable code, set immediately [PMDxEMGCR]<EMGEN>=0 or [PMDxOVVCR]<OVVEN>=0.

Note: Write a disable code each at disabling EMG and OVV.

4.2.13. [PMDxEMGCR] (EMG Control Register)

Bit	Bit Symbol	After reset	Type	Function
31:12	-	0	R	Read as "0".
11:8	EMGCNT[3:0]	0x0	R/W	EMG _x _N input detection time 0x0 to 0xF (When <EMGCNT>=0x0, the noise filter is bypassed.) The noise filtering length of anomaly detection input set to these bits. And this value can be calculated by following formula. <EMGCNT> × 16/fsys Please set it while EMG protection is prohibited (<EMGEN>=0). (Note1)
7:6	-	0	R	Read as "0".
5	INHEN	1	R/W	Debug halt enable/disable 0: Disable 1: Enable (Enabled in the initial status) This bit selects whether or not to stop the PMD when the debug halt signal is input.
4:3	EMGMD[1:0]	11	R/W	EMG protection mode select (Note2) 00: All phases High-impedance 01: All upper-phases ON / all lower-phases High-impedance 10: All upper-phases High-impedance / all lower-phases ON 11: All phases High-impedance ON indicates that PWM output continues. Sets the port output both the upper (UOx, VOx, WOx) and the lower (XOx, YOx, ZOx) for the case when EMG occurs.
2	-	0	R/W	Always write "0".
1	EMGRS	0	W	EMG protection release 0: Don't care 1: Release protection After setting "0x000" in the [PMDxMDOUT] register (Note3), confirm that [PMDxEMGSTA]<EMGI> becomes "1", then set "1" to <EMGRS>. It releases from the EMG protection state. Always reads as "0".
0	EMGEN	1	R/W	EMG protection circuit enable/disable 0: Disable 1: Enable (Enabled in the initial status) To disable the function, write "0x5A" and then write "0xA5" to the EMG release register ([PMDxEMGREL]). Then, set "0" to <EMGEN> (These three instructions must be executed consecutively.).

Note1: If <EMGCNT> is changed while EMG protection circuit is enabled, it may become the protection state. Therefore, when <EMGCNT> is changed, please release the protection state by the following procedure:

- (1) [PMDxEMGSTA]<EMGI> should be read to confirm its value is "1".
- (2) [PMDxMDOUT]<UPWM>, <VPWM>, <WPWM>, <UOC>, <VOC>, and <WOC> should be set to "0" to set all port outputs to inactive state.
- (3) [PMDxEMGCR]<EMGRS> should be set to "1" to exit EMG protection state.

Note2: <EMGMD> protection mode setting is prioritized when OVV and EMG occur at the same time.

Note3: EMG protection cannot be released if the subsequent stage buffer of [PMDxMDOUT] is not updated to "0x000".

4.2.14. [PMDxEMGSTA] (EMG Status Register)

Bit	Bit Symbol	After reset	Type	Function
31:2	-	0	R	Read as "0".
1	EMGI	Undefined	R	EMGx_N input state 0: Active input. 1: Inactive input. EMGx_N input status can be checked by reading this bit.
0	EMGST	0	R	EMG protection state 0: Normal operation 1: Protected EMG protection status can be checked by reading this bit.

4.2.15. [PMDxOVVCR] (OVV Control Register)

Bit	Bit Symbol	After reset	Type	Function
31:12	-	0	R	Read as "0".
11:8	OVVCNT[3:0]	0x0	R/W	OVV input detection time 0x1 to 0xF (If 0x0 is set, it is handled as 0x1.) The noise filtering length of OVV input set to these bits. And this value can be calculated by following formula. $\langle \text{OVVCNT} \rangle \times 16 / \text{fsys}$ Please set it while OVV protection is prohibited ($\langle \text{OVVEN} \rangle = 0$).
7	-	0	R	Read as "0".
6	ADIN1EN	0	R/W	AD monitor function 1 input enable (Note1) 0: Disable input 1: Enable input Selects enable/disable signals from AD monitor function 1 of the ADC. If you enable it and select AD monitor function signal for input ($\langle \text{OVVISEL} \rangle = 1$), the results of the AD monitor function 1 as OVV inputs (if OVV protection is enabled).
5	ADIN0EN	0	R/W	AD monitoring function 0 input enable (Note1) 0: Disable input 1: Enable input Selects enable/disable signals from AD monitor function 0 of the ADC. If you enable it and select AD monitor function signal for input ($\langle \text{OVVISEL} \rangle = 1$), the results of the AD monitor function 0 as OVV inputs (if OVV protection is enabled).
4:3	OVVMD[1:0]	00	R/W	Selects OVV protection mode (Note2) 00: No output control 01: All upper-phases ON, all lower-phases OFF 10: All upper-phases OFF, all lower-phases ON 11: All phases OFF This field controls the outputs of the upper (UOx, VOx, WOx) and lower (XOx, YOx, ZOx) phases when an OVV condition occurs. ON indicates that it's fixed to active output. OFF indicates that it's fixed inactive output. Active and inactive are depends on the settings of $\langle \text{POLL} \rangle$ and $\langle \text{POLH} \rangle$.

Bit	Bit Symbol	After reset	Type	Function
2	OVVISEL	0	R/W	<p>Selects OVV input 0: OVVx_N pin input 1: AD monitor function signal</p> <p>This bit selects whether to use port input or the monitor signal from the ADC as the OVV signal to be input to the protection circuit.</p> <p>When the AD monitor function signal is selected, the setting of OVV input detection time <OVVCNT> becomes invalid.(Direct input)</p>
1	OVVRS	0	R/W	<p>Selects OVV protection state release 0: Disable automatic release of OVV protection state 1: Enable automatic release of OVV protection state</p> <p>If automatic release of OVV protection is enabled, when the state changes to OVV protection after detecting anomaly (OVV input makes a high-to-low transition), the OVV protection state can be automatically released when updating the buffer of PWM period register [<i>PMDxMDPRD</i>] after the OVV input transition to high. (Refer to the "Table 4.1 [<i>PMDxMDPRD</i>],[<i>PMDxCMPU/V/W</i>] buffer Update Timing".)</p>
0	OVVEN	0	R/W	<p>OVV protection circuit enable/disable 0: Disable 1: Enable</p> <p>To disable the function, write "0x5A" and then write "0xA5" to the EMG release register (<i>[PMDxEMGREL]</i>). Then, set "0" to <OVVEN>. (These three instructions must be executed consecutively.)</p>

Note1: Refer to the chapter "AD Monitor Function" in the Reference Manual of "12-bit Analog to Digital Converter" for detailed information about AD monitor function.

Note2: If OVV and EMG conditions occur simultaneously, the protection mode settings in the bits of <EMGMD> become effective.

4.2.16. [*PMDxOVVSTA*] (OVV Status Register)

Bit	Bit Symbol	After reset	Type	Function
31:2	-	0	R	Read as "0".
1	OVVI	Undefined	R	<p>OVVI input state 0: Active input. 1: Inactive input.</p> <p>OVV input status (Input selected by [<i>PMDxOVVCR</i>]<OVVISEL>) can be checked by reading this bit.</p>
0	OVVST	0	R	<p>OVV protection state 0: Normal operation 1: In protected</p> <p>OVV protection status can be checked by reading this bit.</p>

4.2.17. [PMDxDTR] (Dead time Register)

Bit	Bit Symbol	After reset	Type	Function
31:8	-	0	R	Read as "0".
7:0	DTR[7:0]	0x00	R/W	Sets dead time 0x00 to 0xFF The dead time value can be calculated by following formula. <DTR> × 8/fsys

Note: Do not change [PMDxDTR] register while [PMDxMDEN]<PWMEN>=1.

4.2.18. [PMDxTRGCMP0] (Trigger Compare 0 Register)

Bit	Bit Symbol	After reset	Type	Function
31:16	-	0	R	Read as "0".
15:0	TRGCMP0[15:0]	0x0000	R/W	Trigger output compare register <TRGCMP0> should be set in a range of 0x0001 to [PMDxMDPRD] value - 1]. When the PWM counter value [PMDxMDCNT] matches the value set in [PMDxTRGCMP0]. TRG0 is output. Note: It is prohibited to set [PMDxTRGCMP0] to "0x0000" and [PMDxTRGCMP0] ≥ [PMDxMDPRD].

Note1: Do not write to this register in byte unit. If the upper 8 bits [15:8] and the lower 8 bits [7:0] are written separately, operation cannot be guaranteed.

Note2: Since the trigger compare register is double-buffered, this register can be changed during the operation of the PWM counter.

Note3: For detailed update timing of the subsequent stage buffer, refer to the "Table 4.3 [PMDxTRGCMPn] buffer Update Timing".

Note4: Read value is the first buffer value (the latest data set via a bus).

Note5: When PWM is started (<PWMEN>=1) while [PMDxTRGCMPn] (n=0 to 3) is set to "0x0001" with saw-tooth wave carrier (<PWMMD>=0), there is no trigger output in the first PWM cycle.

Table 4.3 [PMDxTRGCMPn] buffer Update Timing

[PMDxTRGSYNCR] <TSYNCS>setting	[PMDxTRGCR] <TRGnMD>setting	[PMDxTRGCMPn] Buffer update timing
00	000	Updates immediately
	001	Update when PWM carrier peak
	010	Update when PWM carrier bottom
	011	Update when PWM carrier peak or PWM carrier bottom (Note1)
	1xx	Updates immediately
01	xxx	Update when PWM carrier bottom
10	xxx	Update when PWM carrier peak
11	xxx	Update when PWM carrier peak or PWM carrier bottom (Note1)

Note1: Updates at carrier peak when saw-tooth wave carrier is selected ([PMDxMDCR]<PWMMD>=0).

Note2: x: Don't care

Note3: Asynchronous update [PMDxMDEN]<PWMEN>=0 regardless of setting.

4.2.19. [PMDxTRGCMP1] (Trigger Compare 1 Register)

Bit	Bit Symbol	After reset	Type	Function
31:16	-	0	R	Read as "0".
15:0	TRGCMP1[15:0]	0x0000	R/W	Trigger output compare register <TRGCMP1> should be set in a range of 0x0001 to [[PMDxMDPRD] value - 1]. When the PWM counter value [PMDxMDCNT] matches the value set in [PMDxTRGCMP1], TRG1 is output. Note: It is prohibited to set [PMDxTRGCMP1] to "0x0000" and [PMDxTRGCMP1] ≥ [PMDxMDPRD].

- Note1: Do not write to this register in byte unit. If the upper 8 bits [15:8] and the lower 8 bits [7:0] are written separately, operation cannot be guaranteed.
- Note2: Since the trigger compare register is double-buffered, this register can be changed during the operation of the PWM counter.
- Note3: For detailed update timing of the subsequent stage buffer, refer to the "Table 4.3 [PMDxTRGCMPn] buffer Update Timing".
- Note4: Read value is the first buffer value (the latest data set via a bus).
- Note5: When PWM is started (<PWMEN>=1) while [PMDxTRGCMPn] (n=0 to 3) is set to "0x0001" with saw-tooth wave carrier (<PWMMD>=0), there is no trigger output in the first PWM cycle.

4.2.20. [PMDxTRGCMP2] (Trigger Compare 2 Register)

Bit	Bit Symbol	After reset	Type	Function
31:16	-	0	R	Read as "0".
15:0	TRGCMP2[15:0]	0x0000	R/W	Trigger output compare register <TRGCMP2> should be set in a range of 0x0001 to [[PMDxMDPRD] value - 1]. When the PWM counter value [PMDxMDCNT] matches the value set in [PMDxTRGCMP2], TRG2 is output. Note: It is prohibited to set [PMDxTRGCMP2] to "0x0000" and [PMDxTRGCMP2] ≥ [PMDxMDPRD].

- Note1: Do not write to this register in byte unit. If the upper 8 bits [15:8] and the lower 8 bits [7:0] are written separately, operation cannot be guaranteed.
- Note2: Since the trigger compare register is double-buffered, this register can be changed during the operation of the PWM counter.
- Note3: For detailed update timing of the subsequent stage buffer, refer to the "Table 4.3 [PMDxTRGCMPn] buffer Update Timing".
- Note4: Read value is the first buffer value (the latest data set via a bus).
- Note5: When PWM is started (<PWMEN>=1) while [PMDxTRGCMPn] (n=0 to 3) is set to "0x0001" with saw-tooth wave carrier (<PWMMD>=0), there is no trigger output in the first PWM cycle.

4.2.21. [PMDxTRGCMP3] (Trigger Compare 3 Register)

Bit	Bit Symbol	After reset	Type	Function
31:16	-	0	R	Read as "0".
15:0	TRGCMP3[15:0]	0x0000	R/W	Trigger output compare register <TRGCMP3> should be set in a range of 0x0001 to [[PMDxMDPRD] value- 1]. When the PWM counter value [PMDxMDCNT] matches the value set in [PMDxTRGCMP3]. TRG3 is output. Note: It is prohibited to set [PMDxTRGCMP3] to "0x0000" and [PMDxTRGCMP3] ≥ [PMDxMDPRD].

- Note1: Do not write to this register in byte unit. If the upper 8 bits [15:8] and the lower 8 bits [7:0] are written separately, operation cannot be guaranteed.
- Note2: Since the trigger compare register is double-buffered, this register can be changed during the operation of the PWM counter.
- Note3: For detailed update timing of the subsequent stage buffer, refer to the "Table 4.3 [PMDxTRGCMPn] buffer Update Timing".
- Note4: Read value is the first buffer value (the latest data set via a bus).
- Note5: When PWM is started (<PWMEN>=1) while [PMDxTRGCMPn] (n=0 to 3) is set to "0x0001" with saw-tooth wave carrier (<PWMMD>=0), there is no trigger output in the first PWM cycle.

4.2.22. [PMDxTRGCR] (Trigger Control Register)

Bit	Bit Symbol	After reset	Type	Function
31:16	-	0	R	Read as "0".
15	TRG3BE	0	R/W	Asynchronous update of the [PMDxTRGCMP3] buffer This bit enables asynchronous updating to the subsequent stage buffer from [PMDxTRGCMP3] . (Note1) (Note2) 0: Synchronous update 1: Asynchronous update (The value written to [PMDxTRGCMP3] is immediately reflected.)
14:12	TRG3MD[2:0]	000	R/W	[PMDxTRGCMP3] mode setting This register selects a match-mode of trigger output (TRG3). 000: Trigger output disabled 001: Trigger output at down-count match (Note3) 010: Trigger output at up-count match (Note4) 011: Trigger output at up/down-count match (Note3) (Note5) 100: Trigger output at PWM carrier peak 101: Trigger output at PWM carrier bottom (Note3) 110: Trigger output at PWM carrier peak/bottom (Note3) 111: Trigger output disabled
11	TRG2BE	0	R/W	Asynchronous update of the [PMDxTRGCMP2] buffer This bit enables asynchronous updating to the subsequent stage buffer from [PMDxTRGCMP2] . (Note1) (Note2) 0: Synchronous update 1: Asynchronous update (The value written to [PMDxTRGCMP2] is immediately reflected.)
10:8	TRG2MD[2:0]	000	R/W	[PMDxTRGCMP2] mode setting This register selects a match-mode of trigger output (TRG2). 000: Trigger output disabled 001: Trigger output at down-count match (Note3) 010: Trigger output at up-count match (Note4) 011: Trigger output at up/down-count match (Note3) (Note5) 100: Trigger output at PWM carrier peak 101: Trigger output at PWM carrier bottom (Note3) 110: Trigger output at PWM carrier peak/bottom (Note3) 111: Trigger output disabled
7	TRG1BE	0	R/W	Asynchronous update of the [PMDxTRGCMP1] buffer This bit enables asynchronous updating to the subsequent stage buffer from [PMDxTRGCMP1] . (Note1) (Note2) 0: Synchronous update 1: Asynchronous update (The value written to [PMDxTRGCMP1] is immediately reflected.)
6:4	TRG1MD[2:0]	000	R/W	[PMDxTRGCMP1] mode setting This register selects a match-mode of trigger output (TRG1). 000: Trigger output disabled 001: Trigger output at down-count match (Note3) 010: Trigger output at up-count match (Note4) 011: Trigger output at up/down-count match (Note3) (Note5) 100: Trigger output at PWM carrier peak 101: Trigger output at PWM carrier bottom (Note3) 110: Trigger output at PWM carrier peak/bottom (Note3) 111: Trigger output disabled

Bit	Bit Symbol	After reset	Type	Function
3	TRG0BE	0	R/W	Asynchronous update of the [PMDxTRGCMP0] buffer This bit enables asynchronous updating to the subsequent stage buffer from [PMDxTRGCMP0] . (Note1)(Note2) 0: Synchronous update 1: Asynchronous update (The value written to [PMDxTRGCMP0] is immediately reflected.)
2:0	TRG0MD[2:0]	000	R/W	[PMDxTRGCMP0] mode setting This register selects a match-mode of trigger output (TRG0). 000: Trigger output disabled 001: Trigger output at down-count match (Note3) 010: Trigger output at up-count match (Note4) 011: Trigger output at up/down-count match (Note3) (Note5) 100: Trigger output at PWM carrier peak 101: Trigger output at PWM carrier bottom (Note3) 110: Trigger output at PWM carrier peak/bottom (Note3) 111: Trigger output disabled

Note1: When **[PMDxMDEN]<PWMEN>=0**, updates asynchronously regardless of setting.

Note2: For detailed update timing, refer to the "Table 4.3 **[PMDxTRGCMPn]** buffer Update Timing".

Note3: When a "0" is set to **[PMDxMDCR]<PWMMD>** (Saw-tooth wave), please do not select.

Note4: When PWM is started (**<PWMEN>=1**) while **[PMDxTRGCMPn]** (n=0 to 3) is set to "0x0001" with saw-tooth wave carrier (**<PWMMD>=0**), there is no trigger output in the first PWM cycle.

Note5: When **[PMDxTRGCMPn]=0x0001** (n=0 to 3) and **[PMDxMDCR]<PWMMD>=1** (triangular wave), one trigger output is made per period.

4.2.23. **[PMDxTRGSYNCR]** (Trigger Update Timing Setting Register)

Bit	Bit Symbol	After reset	Type	Function
31:2	-	0	R	Read as "0".
1:0	TSYNCS[1:0]	00	R/W	Update timing setting for the buffer of the trigger compare register. 00: PWM carrier bottom or PWM carrier peak is set for each trigger by setting [PMDxTRGCR]<TRGnMD> (n=0 to 3). 01: PWM carrier bottom 10: PWM carrier peak 11: PWM carrier peak and PWM carrier bottom

Note1: Asynchronous update **[PMDxMDEN]<PWMEN>=0** regardless of setting.

Note2: Refer to the "Table 4.3 **[PMDxTRGCMPn]** buffer Update Timing".

4.2.24. [PMDxTRGMD] (Trigger Output Mode Setting Register)

Bit	Bit Symbol	After reset	Type	Function
31:2	-	0	R	Read as "0".
1	TRGOUT	0	R/W	<p>Trigger output mode 0: Trigger fixed output 1: Trigger selection output</p> <p>When trigger fixed output is selected, trigger outputs from PMDxTRG0 to PMDxTRG3 output the trigger signals generated by a match with [PMDxTRGCMP0] to [PMDxTRGCMP3] respectively. A PMDxTRG4 and a PMDxTRG5 are not output the trigger signals.</p> <p>When trigger selection output is selected, output signals of the [PMDxTRGCMP0] are output to one of trigger output from PMDxTRG0 to PMDxTRG5. The trigger output signal is selected by trigger output selection register.(Note)</p>
0	EMGTGE	0	R/W	<p>Output enable in EMG protection state 0: Disable trigger output in the protection state 1: Enable trigger output in the protection state</p> <p>This bit enables or disables trigger output in the EMG protection state.</p>

Note: Refer to the "Table 4.4 Trigger Output Patterns" when trigger selection output is selected (<TRGOUT>=1).

Table 4.4 Trigger Output Patterns

<TRGOUT> Setting	Compare Register	<TRGSEL> Setting	Trigger Output
<TRGOUT>=0	[PMDxTRGCMP0]	N/A	PMDxTRG0
	[PMDxTRGCMP1]		PMDxTRG1
	[PMDxTRGCMP2]		PMDxTRG2
	[PMDxTRGCMP3]		PMDxTRG3
<TRGOUT>=1	[PMDxTRGCMP0]	0	PMDxTRG0
		1	PMDxTRG1
		2	PMDxTRG2
		3	PMDxTRG3
		4	PMDxTRG4
		5	PMDxTRG5
	[PMDxTRGCMP1]	N/A	No trigger output
	[PMDxTRGCMP2]	N/A	No trigger output
[PMDxTRGCMP3]	N/A	No trigger output	

4.2.25. [PMDxTRGSEL] (Trigger Output Selection Register)

Bit	Bit Symbol	After reset	Type	Function
31:3	-	0	R	Read as "0".
2:0	TRGSEL[2:0]	000	R/W	Trigger output select 000: Output from PMDxTRG0 001: Output from PMDxTRG1 010: Output from PMDxTRG2 011: Output from PMDxTRG3 100: Output from PMDxTRG4 101: Output from PMDxTRG5 110: No trigger output 111: No trigger output This field is effective when the trigger selection output mode is selected ([PMDxTRGMD]<TRGOUT>=1). And an output trigger can be selected by setting the [PMDxTRGCMPO] register. (Refer to the "Table 4.4 Trigger Output Patterns".)

- Note1: Since the trigger output selection register is double-buffered, this register can be changed during the operation of the PWM counter.
- Note2: The update timing of the subsequent stage buffer is as the same as the compare register ([PMDxCMPU/V/W]).
- Note3: When PMD is disabled ([PMDxMDEN]<PWMEN>=0), updates asynchronously.

5. Precautions

- When PMD cooperate with a ADC, please refer to the reference manual "12-bit Analog to Digital Converter".
- The byte write of registers is disabled regardless of whether PWM is operating or stopped.
- *[PMDxMDCNT]* value has changed during PWM operation. Therefore, the byte read of *[PMDxMDCNT]* should not be done. Read should be done with Word or Half-word unit.
- The following registers have the double-buffer structure. The data written to these registers is transferred to the subsequent stage buffer at each update timing (depending on the setting).
 - *[PMDxCMPU]*, *[PMDxCMPV]*, *[PMDxCMPW]*
 - *[PMDxMDOUT]*
 - *[PMDxMDPRD]*
 - *[PMDxTRGCMP0]* to *[PMDxTRGCMP3]*
 - *[PMDxTRGSEL]*
- Even in the setting of *[PMDxMDCR]*<PWMMD>=1(Triangular wave carrier) and *[PMDxTRGCR]* <TRGnMD> =011(Trigger output at up/down-count match), When *[PMDxTRGCMPn]* (n=0 to 3) setting is "0x0001", TRGn is generated only once in the PWM period.
- The PWM carrier is set to the saw-tooth wave, and *[PMDxTRGCMPn]* (n=0 to 3) is set to "0x0001". Then, if *[PMDxMDEN]*<PWMEN> is changed to enable, the TRGn is not generated in the first PWM period.
- Be sure to release processing from the EMG protection state before using the PMD (After setting PORT).
- The EMG protection function is enabled after reset. If it is not used, prohibit it with the following procedure.
 - (1) *[PMDxEMGREL]* should be set to "0x5A".
 - (2) *[PMDxEMGREL]* should be set to "0xA5".
 - (3) *[PMDxEMGCR]*<EMGEN> should be set to "0".

Note: These 3 instructions must be executed consecutively.

- When attempting to stop supplying the clock, make sure to check whether the PMD is stopping. Note that when the MCU shift STOP1/STOP2 mode, make sure to check whether the PMD is stopping as well.

6. Revision History

Table 6.1 Revision History

Revision	Date	Description
1.0	2017-09-08	First release
2.0	2018-04-02	<ul style="list-style-type: none"> - The entire document dead-time → dead time - Page2 Table of Contents → Contents - Related document Added: Advanced Encoder Input Circuit - Terms and Abbreviations Modified: Programmable Motor Driver → Programmable Motor Control Circuit - 1.Outlines Table PWM interrupt/ Operation terms: Added prefix - Figure 2.1 Modified description - 3. Function and Operation 5th term: Modified - 3.1.Clock Supply Modified text - Modified description Figure 3.1, Figure 3.4 to Figure 3.9 - 3.6. Synchronous Trigger Generation Circuit Page 27 1st stage Added: (Refer to "Table 4.4 Trigger Output Patterns".) - 4.1.List of Registers Upper table: Added TYPE, ch2, ch3 Added Note under table - 5. Precautions Added 9th term
2.1	2019-07-23	<ul style="list-style-type: none"> - Overall Modified "Variable trigger output" to "Trigger selection output" Modified "Fixed trigger output" to "Trigger fixed output" Modified "trigger output select register" to "trigger output selection register" - Conventions - 1.Outlines Table Trigger generation / Operation: Modified explanation Buffer function / Operation: Modified explanation of Update timing - 2.Configuration Table 2.1 Signal name Modified "Protection signal input(EMG)" to "Emergency state detection input pin" Modified "Protection signal input(OVV)" to "Over voltage detection input pin" - 3.2.1.Setting the PWM period Added Note - 3.2.2. Compare function Modified "PWM compare registers" to "3-phase PWM compare registers" Added "When triangular wave carrier, " above Figure 3.3 Modified "each phase" to "each phase of 3 phase PWM" under Figure 3.3 Modified "<nPWM>" to "<nPWM> (n=U,V,W)" under Figure 3.3 - 3.2.4.Interrupt processing Modified "PWM interrupt period" to "frequency of PWM interrupt" - 3.3.Conduction Control Circuit Figure 3.4 Modified "Comutation trigger" to "Commutation trigger" Modified "EMG return enable" to "EMG release enable" - 3.4.Protection Control Circuit Figure 3.5 Modified "EMG detection input" to "Emergency state detection input" Modified "OVV detection input (Port)" to "Over voltage detection input (Port)" Modified "OVV detection input (AD)" to "OVV status signal (AD)" - 3.4.1.EMG Protection Circuit Text: Modified the description of the EMG protection circuit Release of the EMG protection: Modified Note2 Disable of the EMG protection function: Modified "[PMDxEMGREL] register" to "EMG release register([PMDxEMGREL])" - 3.4.2.OVV Protection Circuit OVV input: Added "The noise filter is valid only when the OVVx_N pin is selected (<OVVISEL> = 0)." OVV protection operation, Release of the OVV protection: Modified "OVV signal input", "OVV protection input", and "port" to "OVV input" - 3.4.3.Protection control when using the debug tool Modified "when PMD is stopped" to "when CPU is stopped" - 3.5.Dead time Control Circuit Modified "dead time unit" to "dead time circuit" Modified "output polarity switching unit" to "output polarity switching circuit" - 3.6.Synchronous Trigger Generation Circuit Note1 to Note4: Modified expression

		<p>Text: Modified the description of trigger selection output mode</p> <ul style="list-style-type: none"> - 4.2.1. Added "(Note1) (Note2)" in Function - 4.2.2. Added "(Note1) (Note2) (Note3)" in Function Note1 and Note2: Modified expression - 4.2.3. Bit5 / Function: Added "setting" Corrected "Table 4.1" to "Table 4.2" Bit 4 to 0 / Function: Added "selection" - 4.2.4. Function: Added "(Note)" - 4.2.11. Table 4.2 and Table 4.3: Corrected "Active high ($[PMDxMDPOT]<POLH><POLL>=00$)" to "Active low ($[PMDxMDPOT]<POLH><POLL>=00$)" - 4.2.13. Bit 1 / Function: Modified "return from the EMG" to "release from the EMG" - 4.2.14. Bit 1 / Function: Modified the description of EMGI - 4.2.16. Bit 1 / Function: Modified the description of OVVI - 4.2.18. 4.2.21. Function and Note: Modified expression - 4.2.22. Function: Added "(TRGn)" Note: Modified expression - 4.2.25. Note: Modified "trigger output selecting register" to "trigger output selection register" - 5.Precautions 5th term: Modified expression 6th term: Modified "permission" to "enable" 7th term: Added "(After setting PORT)" 9th term: Modified "enters" to "shift" - RESTRICTIONS ON PRODUCT USE Updated
--	--	---

RESTRICTIONS ON PRODUCT USE

Toshiba Corporation and its subsidiaries and affiliates are collectively referred to as "TOSHIBA". Hardware, software and systems described in this document are collectively referred to as "Product".

- TOSHIBA reserves the right to make changes to the information in this document and related Product without notice.
- This document and any information herein may not be reproduced without prior written permission from TOSHIBA. Even with TOSHIBA's written permission, reproduction is permissible only if reproduction is without alteration/omission.
- Though TOSHIBA works continually to improve Product's quality and reliability, Product can malfunction or fail. Customers are responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of Product could cause loss of human life, bodily injury or damage to property, including data loss or corruption. Before customers use the Product, create designs including the Product, or incorporate the Product into their own applications, customers must also refer to and comply with (a) the latest versions of all relevant TOSHIBA information, including without limitation, this document, the specifications, the data sheets and application notes for Product and the precautions and conditions set forth in the "TOSHIBA Semiconductor Reliability Handbook" and (b) the instructions for the application with which the Product will be used with or for. Customers are solely responsible for all aspects of their own product design or applications, including but not limited to (a) determining the appropriateness of the use of this Product in such design or applications; (b) evaluating and determining the applicability of any information contained in this document, or in charts, diagrams, programs, algorithms, sample application circuits, or any other referenced documents; and (c) validating all operating parameters for such designs and applications. **TOSHIBA ASSUMES NO LIABILITY FOR CUSTOMERS' PRODUCT DESIGN OR APPLICATIONS.**
- **PRODUCT IS NEITHER INTENDED NOR WARRANTED FOR USE IN EQUIPMENTS OR SYSTEMS THAT REQUIRE EXTRAORDINARILY HIGH LEVELS OF QUALITY AND/OR RELIABILITY, AND/OR A MALFUNCTION OR FAILURE OF WHICH MAY CAUSE LOSS OF HUMAN LIFE, BODILY INJURY, SERIOUS PROPERTY DAMAGE AND/OR SERIOUS PUBLIC IMPACT ("UNINTENDED USE").** Except for specific applications as expressly stated in this document, Unintended Use includes, without limitation, equipment used in nuclear facilities, equipment used in the aerospace industry, lifesaving and/or life supporting medical equipment, equipment used for automobiles, trains, ships and other transportation, traffic signaling equipment, equipment used to control combustions or explosions, safety devices, elevators and escalators, and devices related to power plant. **IF YOU USE PRODUCT FOR UNINTENDED USE, TOSHIBA ASSUMES NO LIABILITY FOR PRODUCT.** For details, please contact your TOSHIBA sales representative or contact us via our website.
- Do not disassemble, analyze, reverse-engineer, alter, modify, translate or copy Product, whether in whole or in part.
- Product shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable laws or regulations.
- The information contained herein is presented only as guidance for Product use. No responsibility is assumed by TOSHIBA for any infringement of patents or any other intellectual property rights of third parties that may result from the use of Product. No license to any intellectual property right is granted by this document, whether express or implied, by estoppel or otherwise.
- **ABSENT A WRITTEN SIGNED AGREEMENT, EXCEPT AS PROVIDED IN THE RELEVANT TERMS AND CONDITIONS OF SALE FOR PRODUCT, AND TO THE MAXIMUM EXTENT ALLOWABLE BY LAW, TOSHIBA (1) ASSUMES NO LIABILITY WHATSOEVER, INCLUDING WITHOUT LIMITATION, INDIRECT, CONSEQUENTIAL, SPECIAL, OR INCIDENTAL DAMAGES OR LOSS, INCLUDING WITHOUT LIMITATION, LOSS OF PROFITS, LOSS OF OPPORTUNITIES, BUSINESS INTERRUPTION AND LOSS OF DATA, AND (2) DISCLAIMS ANY AND ALL EXPRESS OR IMPLIED WARRANTIES AND CONDITIONS RELATED TO SALE, USE OF PRODUCT, OR INFORMATION, INCLUDING WARRANTIES OR CONDITIONS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ACCURACY OF INFORMATION, OR NONINFRINGEMENT.**
- Do not use or otherwise make available Product or related software or technology for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). Product and related software and technology may be controlled under the applicable export laws and regulations including, without limitation, the Japanese Foreign Exchange and Foreign Trade Law and the U.S. Export Administration Regulations. Export and re-export of Product or related software or technology are strictly prohibited except in compliance with all applicable export laws and regulations.
- Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product. Please use Product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. **TOSHIBA ASSUMES NO LIABILITY FOR DAMAGES OR LOSSES OCCURRING AS A RESULT OF NONCOMPLIANCE WITH APPLICABLE LAWS AND REGULATIONS.**